

DESCRIPTION

The HYM536220A is a 2M x 36-bit Fast page mode CMOS DRAM module consisting of four HY5118160B in 42/42 pin SOJ and eight HY531000A in 20/26 pin SOJ on a 72 pin glass-epoxy printed circuit board. 0.22 μ F decoupling capacitor is mounted for each DRAM.

The HYM536220AW/LW are Tin-Lead plated and HYM536220AWG/LWG are Gold plated socket type Single In-line Memory Modules suitable for easy interchange and addition of 8M byte memory.

FEATURES

- Low power dissipation
 Max. battery back-up 30.8mW (L-part)
 Max. CMOS standby 17.6mW (L-part)
 66.0mW
 Max. TTL standby 132.0mW
 Max. operating

Speed	Power
60	3.70W
70	3.37W
80	3.04W

- Single power supply of 5V \pm 10%
- TTL compatible inputs and outputs
- Fast access time

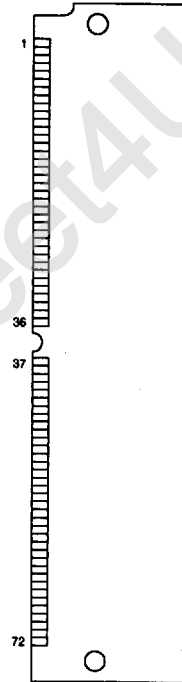
Speed	tRAC	tCAC	tPC
60	60ns	15ns	40ns
70	70ns	20ns	45ns
80	80ns	20ns	50ns

- Fast page mode operation
- CAS-before-RAS, RAS-only, Hidden refresh
- 1024 refresh cycles / 256ms (L-part)
 1024 refresh cycles / 16ms

PIN DESCRIPTION

RAS0-RAS3	Row Address Strobe
CAS0-CAS3	Column Address Strobe
WE	Write Enable
A0-A9	Address Input
DQ0-DQ35	Data Input/Output
PD1-PD4	Presence Detect
Vcc	Power (+ 5V)
Vss	Ground

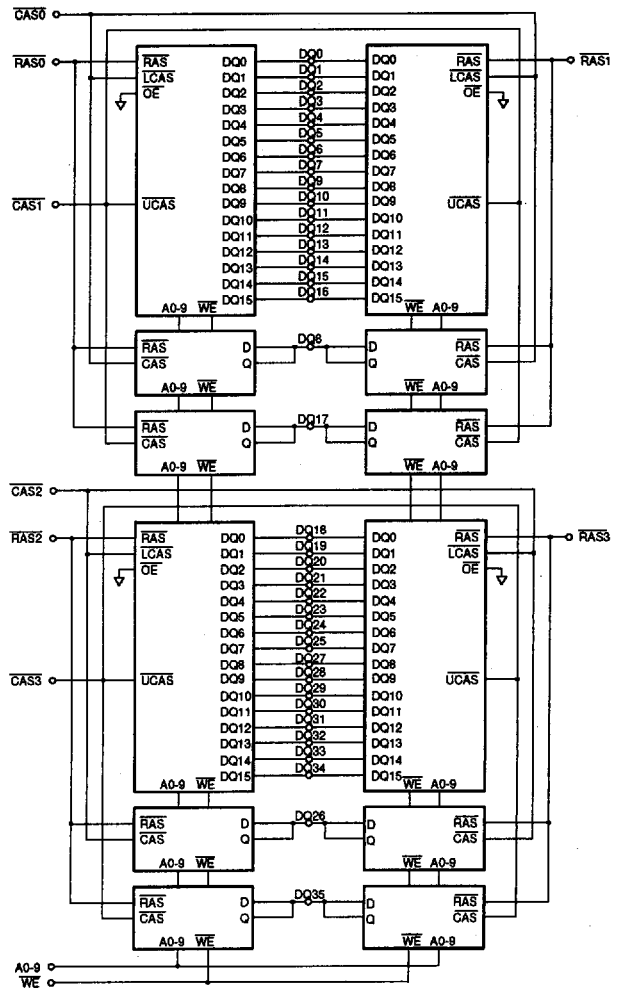
PIN CONNECTION



PIN NAME

#	NAME	#	NAME
1	Vss	37	DQ17
2	DQ0	38	DQ35
3	DQ18	39	Vss
4	DQ1	40	CAS0
5	DQ19	41	CAS2
6	DQ2	42	CAS3
7	DQ20	43	CAS1
8	DQ3	44	RAS0
9	DQ21	45	RAST
10	Vcc	46	NC
11	NC	47	WE
12	A0	48	NC
13	A1	49	DQ9
14	A2	50	DQ27
15	A3	51	DQ10
16	A4	52	DQ28
17	A5	53	DQ11
18	A6	54	DQ29
19	NC	55	DQ12
20	DQ4	56	DQ30
21	DQ22	57	DQ13
22	DQ5	58	DQ31
23	DQ23	59	Vcc
24	DQ6	60	DQ32
25	DQ24	61	DQ14
26	DQ7	62	DQ33
27	DQ25	63	DQ15
28	A7	64	DQ34
29	NC	65	DQ16
30	Vcc	66	NC
31	A8	67	PD1
32	A9	68	PD2
33	RAS3	69	PD3
34	RAS2	70	PD4
35	DQ26	71	NC
36	DQ8	72	Vss

BLOCK DIAGRAM



PRESENCE DETECT PINS

PIN	-60	-70	-80
PD1	NC	NC	NC
PD2	NC	NC	NC
PD3	NC	Vss	NC
PD4	NC	NC	Vss

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
TA	Ambient Temperature	0 to 70	°C
TSTG	Storage Temperature	-55 to 150	°C
VIN, VOUT	Voltage on Any Pin Relative to Vss	-1.0 to 7.0	V
VCC	Voltage on VCC Relative to Vss	-1.0 to 7.0	V
Ios	Short Circuit Output Current	50	mA
Pd	Power Dissipation	9.2	W

NOTE : Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(TA= 0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Vcc	Supply Voltage	4.5	5.0	5.5	V
VIH	Input High Voltage	2.4	-	Vcc+ 1.0	V
VIL	Input Low Voltage	-1.0	-	0.8	V

NOTE : All voltages are referenced to Vss.

DC CHARACTERISTICS

(TA= 0°C to 70°C, VCC= 5V± 10%, VSS= 0V, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED/ POWER	MIN.	MAX.	UNIT	NOTE
I _{LI}	Input Leakage Current (Any Input Pin)	V _{SS} ≤ V _{IN} ≤ V _{CC} + 1.0, All other pins not under test= V _{SS}		-120	120	μA	
I _{LO}	Output Leakage Current (High Impedance State)	V _{SS} ≤ V _{OUT} ≤ V _{CC} , RAS & CAS at V _{IH}		-20	20	μA	
I _{CC1}	V _{CC} Supply Current, Operating	t _{RC} = t _{RC} (min.)	60 70 80	-	672 612 552	mA	1,2,3
I _{CC2}	V _{CC} Supply Current, TTL Standby	RAS & CAS at V _{IH} , other inputs ≥ V _{SS}		-	24	mA	
I _{CC3}	V _{CC} Supply Current, RAS-only refresh	t _{RC} = t _{RC} (min.)	60 70 80	-	672 612 552	mA	1,3
I _{CC4}	V _{CC} Supply Current, Fast Page mode	t _{PC} = t _{PC} (min.)	60 70 80	-	512 432 372	mA	1,2,3
I _{CC5}	V _{CC} Supply Current, CMOS Standby	RAS & CAS ≥ V _{CC} -0.2V	L-part	-	12 2.8	mA	5
I _{CC6}	V _{CC} Supply Current, CAS-before-RAS refresh	t _{RC} = t _{RC} (min.)	60 70 80	-	672 612 552	mA	1,3
I _{CC7}	V _{CC} Supply Current, Battery Back Up (L-part only)	t _{RC} = 250μs, CAS= CBR cycling or 0.2V WE= V _{CC} -0.2V A0-A9= V _{CC} -0.2V or 0.2V DQ0-DQ35= V _{CC} -0.2V, 0.2V, or open	t _{RAS} ≤ 300ns t _{RAS} ≤ 1μs	-	3.8 5.0	mA	1,4,5
V _{OL}	Output Low Voltage	I _{OL} = 4.2mA		-	0.4	V	
V _{OH}	Output High Voltage	I _{OH} = -5mA		2.4	-	V	

NOTE :

- I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} and I_{CC7} depend on cycle rate.
- I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on output loading. Specified values are obtained with the output open.
- I_{CC} is specified as average current. for I_{CC1}, I_{CC3} and I_{CC6}, address can be changed maximum two times while RAS= V_{IL} for I_{CC4}, address can be changed maximum once while CAS= V_{IH}.
- Only t_{RAS}(max.)= 1μs is applied to refresh of battery backup but t_{RAS}(max.)= 10μs is applied to normal functional operation.
- I_{CC5}(max.)= 3.2mA and I_{CC7} are applied to L-part only (HYM536220ALW/LWG).

AC CHARACTERISTICS

(TA= 0°C to 70°C, Vcc= 5V± 10%, Vss= 0V, unless otherwise noted.) NOTE : 1, 2, 3

#	SYMBOL	PARAMETER	HYM536220AW/WG						UNIT	NOTE
			-60		-70		-80			
			MIN	MAX	MIN.	MAX.	MIN.	MAX.		
1	tRC	Random Read or Write Cycle Time	110		130	-	150	-	ns	
2	tRPC	RAS to CAS Precharge Time	5		5	-	5	-	ns	
3	tPC	Fast Page Mode Cycle Time	40		40	-	50	-	ns	
4	tRHCP	RAS Hold Time from CAS Precharge	40		40	-	50	-	ns	
5	tRAC	Access Time from RAS		60	-	70	-	80	ns	5,10,11
6	tCAC	Access Time from CAS		15	-	20	-	20	ns	5,10
7	tAA	Access Time from Column Address		30	-	35	-	40	ns	5,11
8	tCPA	Access Time from CAS Precharge		30	-	35	-	45	ns	5
9	tCLZ	CAS to Output Low Impedance	0		0	-	0	-	ns	5
10	tOFF	Output Buffer Turn-off Delay	0	15	0	15	0	15	ns	6
11	tT	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	4
12	tRP	RAS Precharge Time	40		50	-	60	-	ns	
13	tRAS	RAS Pulse Width	60	10K	70	10K	80	10K	ns	
14	tRASP	RAS Pulse Width (Fast Page Mode)	60	100K	70	100K	80	100K	ns	
15	tRSH	RAS Hold Time	15		20	-	20	-	ns	
16	tCSH	CAS Hold Time	40		50	-	60	-	ns	
17	tCAS	CAS Pulse Width	15	10K	15	10K	15	10K	ns	
18	tRCD	RAS to CAS Delay	15	45	20	50	20	60	ns	10
19	tRAD	RAS to Column Address Delay Time	15	30	15	35	15	40	ns	11
20	tCRP	CAS to RAS Precharge Time	5		5	-	5	-	ns	
21	tCP	CAS Precharge Time	10		10	-	10	-	ns	
22	tASR	Row Address Set-up Time	0		0	-	0	-	ns	
23	tRAH	Row Address Hold Time	10		10	-	10	-	ns	
24	tASC	Column Address Set-up Time	0		0	-	0	-	ns	
25	tCAH	Column Address Hold Time	10		15	-	15	-	ns	
26	tAR	Column Address Hold Time from RAS	50		55	-	60	-	ns	
27	tRAL	Column Address to RAS Lead Time	30		35	-	40	-	ns	
28	tRCS	Read Command Set-up Time	0		0	-	0	-	ns	
29	tRCH	Read Command Hold Time Referenced to CAS	0		0	-	0	-	ns	7
30	tRRH	Read Command Hold Time Referenced to RAS	0		0	-	0	-	ns	7
31	tWCH	Write Command Hold Time	15		15	-	15	-	ns	
32	tWCR	Write Command Hold Time from RAS	50		55	-	60	-	ns	
33	tWP	Write Command Pulse Width	10		10	-	10	-	ns	
34	tRWL	Write Command to RAS Lead Time	20		20	-	20	-	ns	
35	tCWL	Write Command to CAS Lead Time	20		20	-	20	-	ns	
36	tDS	Data-In Set-up Time	0		0	-	0	-	ns	8
37	tDH	Data-In Hold Time	15		15	-	15	-	ns	8
38	tDHR	Data-In Hold Time Referenced to RAS	50		55	-	60	-	ns	
39	tREF	Refresh Period (1024 cycles)	16		16	-	16	ms		
		SL-PART		256		256		256		12
40	tWCS	Write Command Set-up Time			0	-	0	-	ns	9

AC CHARACTERISTICS

(continued)

#	SYMBOL	PARAMETER	HYM536220W/WG						UNIT	NOTE
			-60		-70		-80			
			MIN	MAX	MIN.	MAX.	MIN.	MAX.		
41	tCSR	CAS Set-up Time (CBR Cycle)	5		5	-	5	-	ns	
42	tCHR	CAS Hold Time (CBR Cycle)	10		10	-	10	-	ns	
43	tCPT	CAS Precharge Time (CBR Counter Test)	35		35	-	40	-	ns	
44	tWRP	WE to RAS Precharge Time (CBR Cycle)	10		10	-	10	-	ns	
45	tWRH	WE to RAS Hold Time (CBR Cycle)	10		10	-	10	-	ns	
46	trASS	RAS Pulse Width (Self Refresh Cycle)	100		100	-	100	-	μs	
47	trPS	RAS Precharge Time (Self Refresh Cycle)	130		150	-	180	-	ns	
48	tCHS	CAS Hold Time (Self Refresh Cycle)	-50		-50	-	-50	-	ns	

NOTE :

1. An initial pause of 200 μ s is required after power-up followed by 8 RAS cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 CAS-before-RAS initialization cycles instead of 8 RAS-only refresh cycles are required. The device should be carefully initialized to be prevented from being entered into multi bit test mode.
2. If RAS= Vss during power-up, the HYM536220A could begin an active cycle. This condition results in higher power-up current than necessary demands from the power-up. It is recommended that RAS and CAS track with Vcc during power-up or be held at a valid VIH in order to minimize the power-up current.
3. VIH(min.) and VIL(max.) are reference levels for measuring timing of input signals. Transition time is measured between VIH and VIL and assumed to be 5ns for all inputs.
4. Refer to the HY531000A and HY5118160B data sheet for detailed information.
5. Measured with a load equivalent to 2 TTL loads and 100pF.
6. tOFF(max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. Either tRCH or tRRH must be satisfied for a read cycle.
8. These parameters are referenced to CAS leading edge in early write cycles.
9. twCS is not a restrictive operating parameter. It is included in the data sheet as electrical characteristics only. If twCS \geq twCS(min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle.
10. Operation within the tRCD(max.) limit insures that tRAC(max.) can be met. tRCD(max.) is specified as a reference point only. If tRCD is greater than the specified tRCD(max.) limit, then access time is controlled by tCAC.
11. Operation within the tRAD(max.) limit insures that tRAC(max.) can be met. tRAD(max.) is specified as a reference point only. If tRAD is greater than the specified tRAD(max.) limit, then access time is controlled by tAA.
12. tREF(max.)= 256ms is applied to L-part only (HYM536220ALW and HYM536220ALWG).

CAPACITANCE

(TA= 25°C, VCC= 5V \pm 10%, VSS= 0V, f= 1MHz, unless otherwise noted.)

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
CIN1	Input Capacitance (A0-A9)	-	80	pF
CIN2	Input Capacitance (WE)	-	95	pF
CIN3	Input Capacitance (RAS0-RAS3)	-	38	pF
CIN4	Input Capacitance (CAS0-CAS3)	-	38	pF
CDQ	Data Input/Output Capacitance (DQ0-DQ35)	-	35	pF

ORDERING INFORMATION

PART NUMBER	SPEED	POWER	PACKAGE	PLATING
HYM536220AW	70/80		SIMM	Tin-Lead
HYM536220ALW	70/80	L-part	SIMM	Tin-Lead
HYM536220AWG	70/80		SIMM	Gold
HYM536220ALWG	70/80	L-part	SIMM	Gold

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