

DESCRIPTION

The HYM540A410 is a 4M x 40-bit Fast page mode CMOS DRAM module consisting of ten HY5117400 in 24/28 pin SOJ or TSOP-II on a 72 pin glass-epoxy printed circuit board. 0.22 μ F decoupling capacitor is mounted for each DRAM.

The HYM540A410M/LM/TM/LTM are Tin-Lead plated and HYM540A410MG/LMG/TMG/LTMG are Gold plated socket type Single In-line Memory Modules suitable for easy interchange and addition of 16M byte memory.

FEATURES

- Low power dissipation

Max. battery back-up 27.5mW (L-part)

Max. CMOS standby 22.0mW (L-part)
55.0mW

Max. TTL standby 110.0mW

Max. operating

Speed	Power
60	7.15W
70	6.33W
80	5.50W

- Single power supply of 5V $\pm$ 10%

- TTL compatible inputs and outputs

- Fast access time

Speed	tRAC	tCAC	tPC
60	60ns	15ns	40ns
70	70ns	18ns	45ns
80	80ns	20ns	50ns

- Fast page mode operation

- CAS-before-RAS, RAS-only, Hidden refresh

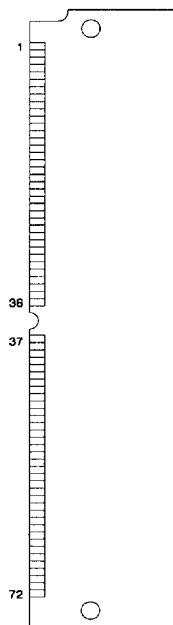
- 2048 refresh cycles / 256ms (L-part)

2048 refresh cycles / 32ms

PIN DESCRIPTION

RAS	Row Address Strobe
CAS	Column Address Strobe
WE	Write Enable
OE	Out Enable
A0-A10	Address Input
DQ0-DQ39	Data Input/Output
PD1-PD4	Presence Detect
Vcc	Power (+5V)
Vss	Ground

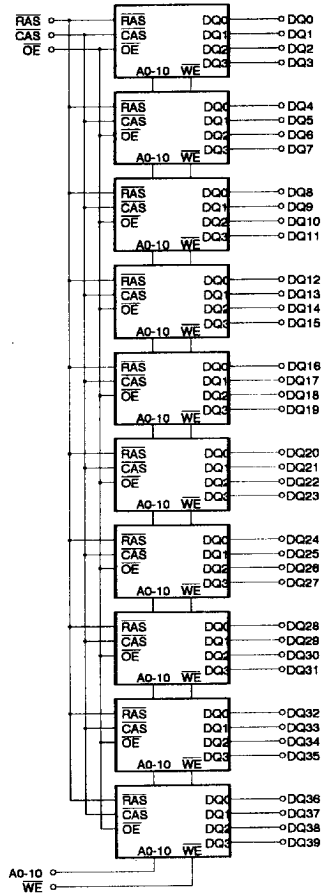
PIN CONNECTION



PIN NAME

#	NAME	#	NAME
1	VSS	37	DQ19
2	DQ0	38	DQ20
3	DQ1	39	VSS
4	DQ2	40	CAS
5	DQ3	41	A10
6	DQ4	42	NC
7	DQ5	43	NC
8	DQ6	44	RAS
9	DQ7	45	NC
10	VCC	46	DQ21
11	NC	47	WE
12	A0	48	VSS
13	A1	49	DQ22
14	A2	50	DQ23
15	A3	51	DQ24
16	A4	52	DQ25
17	A5	53	DQ26
18	A6	54	DQ27
19	OE	55	DQ28
20	DQ8	56	DQ29
21	DQ9	57	DQ30
22	DQ10	58	DQ31
23	DQ11	59	VCC
24	DQ12	60	DQ32
25	DQ13	61	DQ33
26	DQ14	62	DQ34
27	DQ15	63	DQ35
28	A7	64	DQ36
29	DQ16	65	DQ37
30	VCC	66	DQ38
31	A8	67	PD1
32	A9	68	PD2
33	NC	69	PD3
34	NC	70	PD4
35	DQ17	71	DQ39
36	DQ18	72	VSS

BLOCK DIAGRAM



PRESENCE DETECT PINS

PIN	-60	-70	-80
PD1	VSS	VSS	VSS
PD2	NC	NC	NC
PD3	NC	VSS	NC
PD4	NC	NC	VSS

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
TA	Ambient Temperature	0 to 70	°C
TSTG	Storage Temperature	-55 to 150	°C
VIN, VOUT	Voltage on Any Pin Relative to VSS	-1.0 to 7.0	V
VCC	Voltage on VCC Relative to VSS	-1.0 to 7.0	V
IOS	Short Circuit Output Current	50	mA
PD	Power Dissipation	7.0	W

NOTE : Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(TA = 0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
VCC	Supply Voltage	4.5	5.0	5.5	V
VIH	Input High Voltage	2.4	-	VCC + 1.0	V
VIL	Input Low Voltage	-1.0	-	0.8	V

NOTE : All voltages are referenced to VSS.

DC CHARACTERISTICS

(TA = 0°C to 70°C, VCC = 5V ± 10%, VSS = 0V, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED/ POWER	MIN.	MAX.	UNIT	NOTE
ILI	Input Leakage Current (Any Input Pin)	VSS ≤ VIN ≤ VCC + 1.0, All other pins not under test = VSS		-100	100	μA	
ILO	Output Leakage Current (High Impedance State)	VSS ≤ VOUT ≤ VCC, RAS & CAS at VIH		-10	10	μA	
ICC1	VCC Supply Current, Operating	trc = trc (min.)	60 70 80	-	1300 1150 1000	mA	1,2,3
ICC2	VCC Supply Current, TTL Standby	RAS & CAS at VIH, other inputs ≥ VSS		-	20	mA	
ICC3	VCC Supply Current, RAS-only refresh	trc = trc (min.)	60 70 80	-	1300 1150 1000	mA	1,3
ICC4	VCC Supply Current, Fast Page mode	tpc = tpc (min.)	60 70 80	-	700 650 600	mA	1,2,3
ICC5	VCC Supply Current, CMOS Standby	RAS & CAS ≥ VCC-0.2V	L-part	-	10 4	mA	5
ICC6	VCC Supply Current, CAS-before-RAS refresh	trc = trc (min.)	60 70 80	-	1300 1150 1000	mA	1,3
ICC7	VCC Supply Current, Battery Back Up (L-part only)	trc = 125μs, CAS = CBR cycling or 0.2V OE & WE = VCC-0.2V A0-A10 = VCC-0.2V or 0.2V DQ0-DQ39 = VCC-0.2V, 0.2V, or open	trc ≤ 300ns trc ≤ 1μs	-	3 5	mA	1,4,5
VOL	Output Low Voltage	IOL = 4.2mA		-	0.4	V	
VOH	Output High Voltage	IOH = -5mA		2.4	-	V	

NOTE :

1. ICC1, ICC3, ICC4, ICC6 and ICC7 depend on cycle rate.
2. ICC1 and ICC4 depend on output loading. Specified values are obtained with the output open.
3. It depends on user whether column address is changed or not at least once while RAS = VIH and CAS = VIH.
4. Only trc(max.) = 1μs is applied to refresh of battery backup but trc(max.) = 10μs is applied to normal functional operation.
5. ICC5(max.) = 4mA and ICC7 are applied to L-part only (HYM540A410LM, HYM540A410LTM, HYM540A410LMG and HYM540A410LTMG).

AC CHARACTERISTICS

(TA = 0°C to 70°C, VCC = 5V ± 10%, VSS = 0V, unless otherwise noted.) NOTE : 1, 2, 3

#	SYMBOL	PARAMETER	HYM540A410M/TM/MG/LMG/TMG/LTMG						UNIT	NOTE
			-60		-70		-80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	tRC	Random Read or Write Cycle Time	110	-	130	-	150	-	ns	
2	tRWC	Read-Modify-Write Cycle Time	155	-	180	-	200	-	ns	
3	tPC	Fast Page Mode Cycle Time	40	-	45	-	50	-	ns	
4	tPRWC	Fast Page Mode Read-Modify-Write Cycle Time	85	-	95	-	100	-	ns	
5	tRAC	Access Time from RAS	-	60	-	70	-	80	ns	4,9,10
6	tCAC	Access Time from CAS	-	15	-	18	-	20	ns	4,9
7	tAA	Access Time from Column Address	-	30	-	35	-	40	ns	4,9,10
8	tCPA	Access Time from CAS Precharge	-	35	-	40	-	45	ns	4
9	tCLZ	CAS to Output Low Impedance	0	-	0	-	0	-	ns	4
10	tOFF	Output Buffer Turn-off Delay	0	15	0	18	0	20	ns	5
11	tT	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	3
12	tRP	RAS Precharge Time	40	-	50	-	60	-	ns	
13	tRAS	RAS Pulse Width	60	10K	70	10K	80	10K	ns	
14	tRASP	RAS Pulse Width (Fast Page Mode)	60	400K	70	400K	80	400K	ns	
15	tRSH	RAS Hold Time	15	-	18	-	20	-	ns	
16	tCSH	CAS Hold Time	60	-	70	-	80	-	ns	
17	tCAS	CAS Pulse Width	15	10K	18	10K	20	10K	ns	
18	tRCD	RAS to CAS Delay	20	45	20	52	20	60	ns	9
19	tRAD	RAS to Column Address Delay Time	15	30	15	35	15	40	ns	10
20	tCRP	CAS to RAS Precharge Time	5	-	5	-	5	-	ns	
21	tCP	CAS Precharge Time	10	-	10	-	10	-	ns	
22	tASR	Row Address Set-up Time	0	-	0	-	0	-	ns	
23	tRAH	Row Address Hold Time	10	-	10	-	10	-	ns	
24	tASC	Column Address Set-up Time	0	-	0	-	0	-	ns	
25	tCAH	Column Address Hold Time	10	-	15	-	15	-	ns	
26	tAR	Column Address Hold Time from RAS	50	-	55	-	60	-	ns	
27	tRAL	Column Address to RAS Lead Time	30	-	35	-	40	-	ns	
28	tRCS	Read Command Set-up Time	0	-	0	-	0	-	ns	
29	tRCH	Read Command Hold Time Referenced to CAS	0	-	0	-	0	-	ns	6
30	tRRH	Read Command Hold Time Referenced to RAS	0	-	0	-	0	-	ns	6
31	tWCH	Write Command Hold Time	10	-	15	-	15	-	ns	
32	tWCR	Write Command Hold Time from RAS	45	-	55	-	60	-	ns	
33	tWP	Write Command Pulse Width	10	-	15	-	15	-	ns	
34	tRWL	Write Command to RAS Lead Time	15	-	18	-	20	-	ns	
35	tCWL	Write Command to CAS Lead Time	15	-	18	-	20	-	ns	
36	tDS	Data-In Set-up Time	0	-	0	-	0	-	ns	7
37	tDH	Data-In Hold Time	10	-	15	-	15	-	ns	7
38	tDHR	Data-In Hold Time Referenced to RAS	50	-	55	-	60	-	ns	
39	tREF	Refresh Period (2048 cycles)	-	32	-	32	-	32	ms	
		L-part	-	256	-	256	-	256	ms	11
40	tWCS	Write Command Set-up Time	0	-	0	-	0	-	ns	8

AC CHARACTERISTICS

(continued)

continued)

#	SYMBOL	PARAMETER	HYM540A410M/TM/MG/LMG/TMG/LTM						UNIT	NOTE
			-60		-70		-80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
41	tCWD	CAS to WE Delay Time	40	-	45	-	45	-	ns	8
42	tRWD	RAS to WE Delay Time	85	-	95	-	105	-	ns	8
43	tAWD	Column Address to WE Delay Time	55	-	60	-	65	-	ns	8
44	tCSR	CAS Set-up Time (CBR Cycle)	10	-	10	-	10	-	ns	
45	tCHR	CAS Hold Time (CBR Cycle)	10	-	15	-	15	-	ns	
46	tRPC	RAS to CAS Precharge Time	5	-	5	-	5	-	ns	
47	tCPT	CAS Precharge Time (CBR Counter Test)	20	-	25	-	25	-	ns	
48	tROH	RAS Hold Time Reference to OE	10	-	15	-	15	-	ns	
49	tOEA	OE Access Time	0	15	0	18	0	20	ns	
50	tOED	OE to Data Delay	15	-	15	-	15	-	ns	
51	tOEZ	Output Buffer Turn Off Delay Time from OE	0	15	0	15	0	15	ns	
52	tOEH	OE Command Hold Time	15	-	15	-	15	-	ns	
53	tCPWD	WE Delay Time from CAS Precharge	60	-	65	-	70	-	ns	8
54	tRHCP	RAS Hold Time from CAS Precharge	35	-	40	-	45	-	ns	
55	tWRP	WE to RAS Precharge Time (CBR Cycle)	10	-	10	-	10	-	ns	
56	tWRH	WE to RAS Hold Time (CBR Cycle)	10	-	10	-	10	-	ns	

NOTE :

1. An initial pause of 200 μ s is required after power-up followed by 8 $\overline{\text{RAS}}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ initialization cycles instead of 8 $\overline{\text{RAS}}$ -only refresh cycles are required. The device should be carefully initialized to be prevented from being entered into multi bit test mode.
2. $V_{IH}(\text{min.})$ and $V_{IL}(\text{max.})$ are reference levels for measuring timing of input signals. Transition time is measured between V_{IH} and V_{IL} and assumed to be 5ns for all inputs.
3. Refer to the HY5117400 data sheet for detailed information.
4. Measured with a load equivalent to 2 TTL loads and 100pF.
5. $t_{OFF}(\text{max.})$ defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
7. These parameters are referenced to $\overline{\text{CAS}}$ leading edge in early write cycles.
8. t_{WCS} is not a restrictive operating parameter. It is included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}(\text{min.})$, the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle.
9. Operation within the $t_{RCD}(\text{max.})$ limit insures that $t_{RAC}(\text{max.})$ can be met. $t_{RCD}(\text{max.})$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD}(\text{max.})$ limit, then access time is controlled by t_{CAC} .
10. Operation within the $t_{RAD}(\text{max.})$ limit insures that $t_{RAC}(\text{max.})$ can be met. $t_{RAD}(\text{max.})$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD}(\text{max.})$ limit, then access time is controlled by t_{AA} .
11. $t_{REF}(\text{max.}) = 256\text{ms}$ is applied to L-part only (HYM540A410LM, HYM540A410LTM, HYM540A410LMG and HYM540A410LTMG).

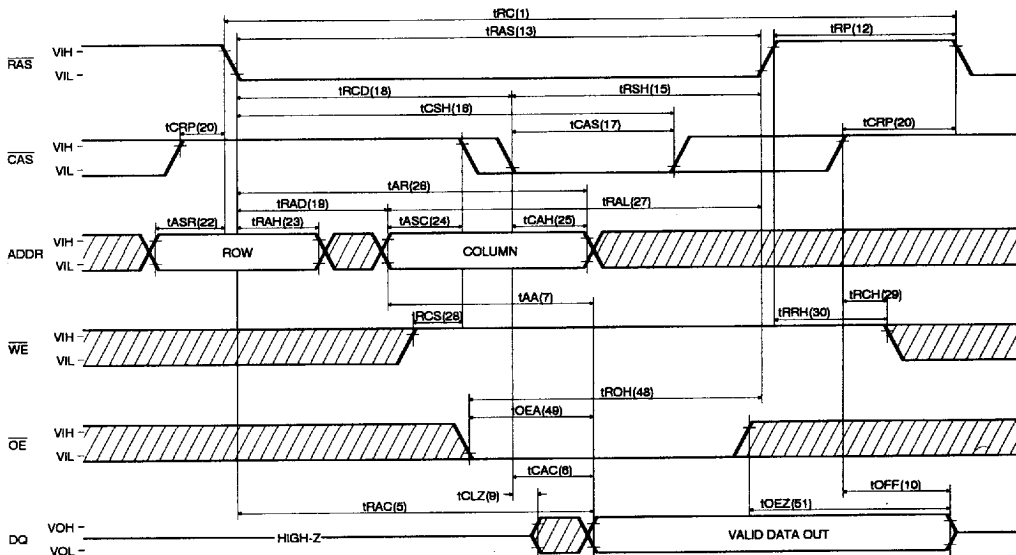
CAPACITANCE

($T_A = 25^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 10\%$, $V_{SS} = 0\text{V}$, $f = 1\text{MHz}$, unless otherwise noted.)

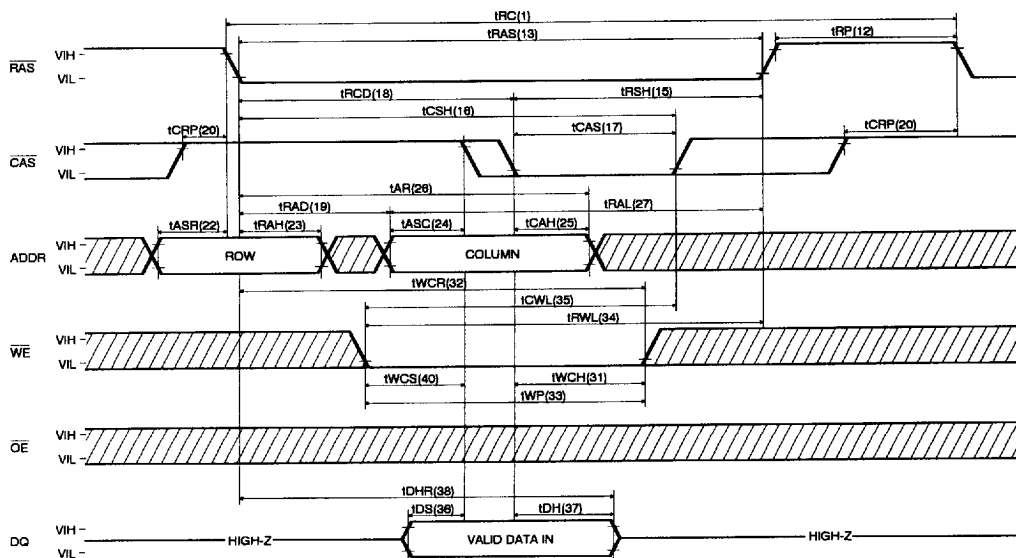
SYMBOL	PARAMETER	TYP.	MAX.	UNIT
C_{IN1}	Input Capacitance (A0-A10)	-	70	pF
C_{IN2}	Input Capacitance ($\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$)	-	80	pF
C_{DQ}	Data Input/Output Capacitance (DQ0-DQ39)	-	17	pF

TIMING DIAGRAM

READ CYCLE



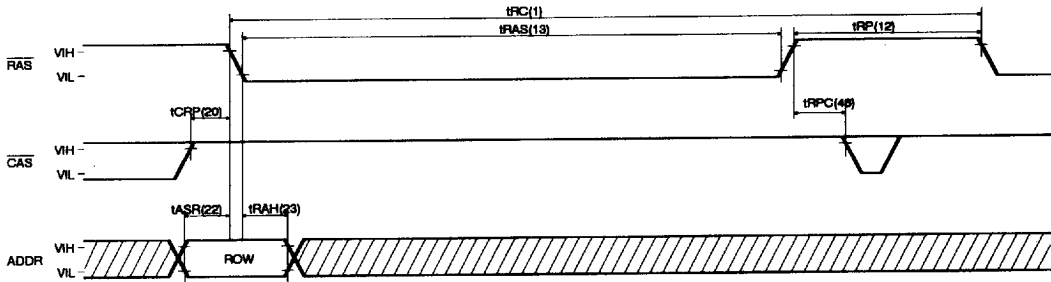
EARLY WRITE CYCLE



The timing diagram illustrates the relationship between the RAS, CAS, ADDR, WE, OE, and DQ signals. Key timing parameters are defined as follows:

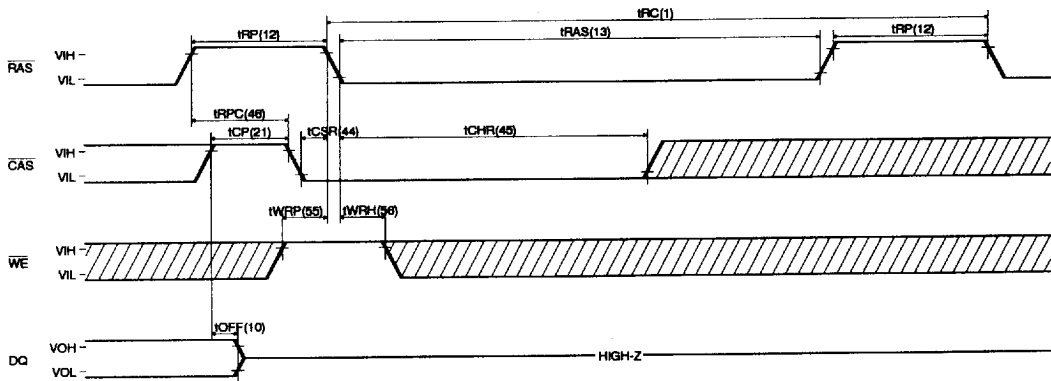
- RAS:** $t_{RASP}(14)$ (RAS pulse width), $t_{CRP}(20)$ (RAS to CAS setup), $t_{CASH}(16)$ (RAS to CAS hold), $t_{RHP}(54)$ (RAS to RAS hold), $t_{RSH}(15)$ (RAS to RAS setup), $t_{CAS}(17)$ (RAS to CAS delay).
- CAS:** $t_{CRP}(20)$ (CAS to RAS setup), $t_{CASH}(16)$ (CAS to RAS hold), $t_{CSP}(21)$ (CAS to RAS setup), $t_{CAS}(17)$ (CAS to RAS delay).
- ADDR:** $t_{ASR}(22)$ (ADDR to RAS setup), $t_{ASR}(22)$ (ADDR to RAS hold), $t_{ASR}(22)$ (ADDR to RAS setup), $t_{ASR}(22)$ (ADDR to RAS hold), $t_{ASR}(22)$ (ADDR to RAS setup), $t_{ASR}(22)$ (ADDR to RAS hold), $t_{ASR}(22)$ (ADDR to RAS setup), $t_{ASR}(22)$ (ADDR to RAS hold).
- WE:** $t_{WCR}(32)$ (WE to RAS setup), $t_{WCR}(32)$ (WE to RAS hold), $t_{WCR}(32)$ (WE to RAS setup), $t_{WCR}(32)$ (WE to RAS hold), $t_{WCR}(32)$ (WE to RAS setup), $t_{WCR}(32)$ (WE to RAS hold), $t_{WCR}(32)$ (WE to RAS setup), $t_{WCR}(32)$ (WE to RAS hold).
- OE:** $t_{OEH}(52)$ (OE to RAS setup), $t_{OEH}(52)$ (OE to RAS hold), $t_{OEH}(52)$ (OE to RAS setup), $t_{OEH}(52)$ (OE to RAS hold), $t_{OEH}(52)$ (OE to RAS setup), $t_{OEH}(52)$ (OE to RAS hold), $t_{OEH}(52)$ (OE to RAS setup), $t_{OEH}(52)$ (OE to RAS hold).
- DQ:** $t_{DS}(36)$ (DQ to RAS setup), $t_{DS}(36)$ (DQ to RAS hold), $t_{DS}(36)$ (DQ to RAS setup), $t_{DS}(36)$ (DQ to RAS hold), $t_{DS}(36)$ (DQ to RAS setup), $t_{DS}(36)$ (DQ to RAS hold), $t_{DS}(36)$ (DQ to RAS setup), $t_{DS}(36)$ (DQ to RAS hold).

RAS-ONLY REFRESH CYCLE



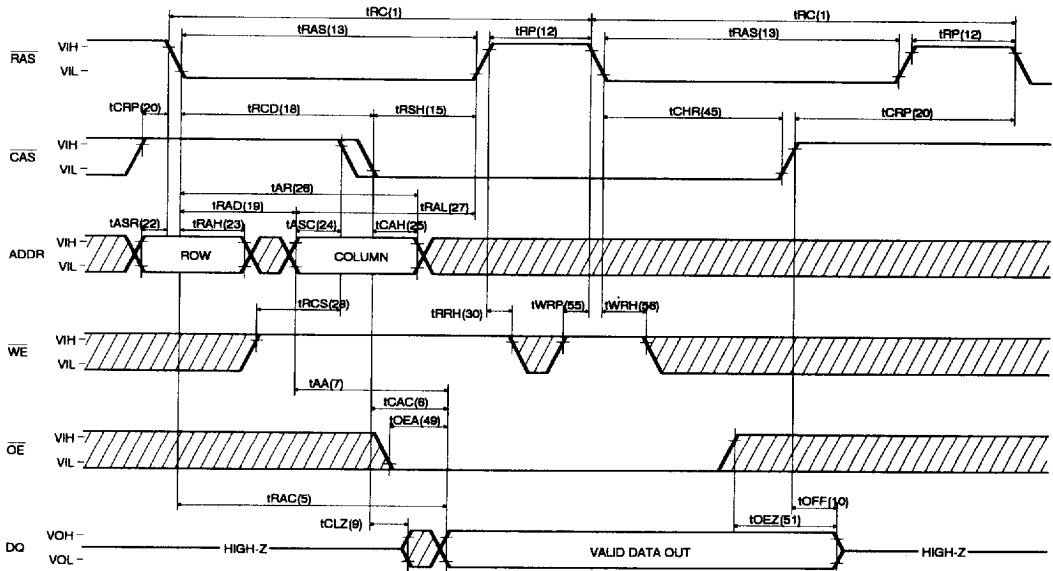
NOTE : WE and OE = "H" or "L"

CAS-BEFORE-RAS REFRESH CYCLE

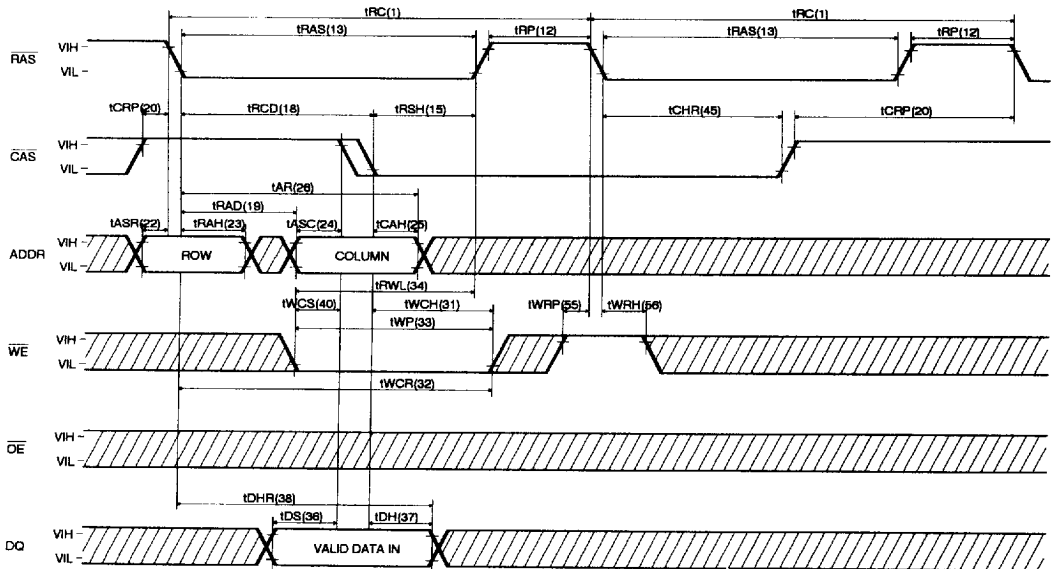


NOTE : ADDR and OE = "H" or "L"

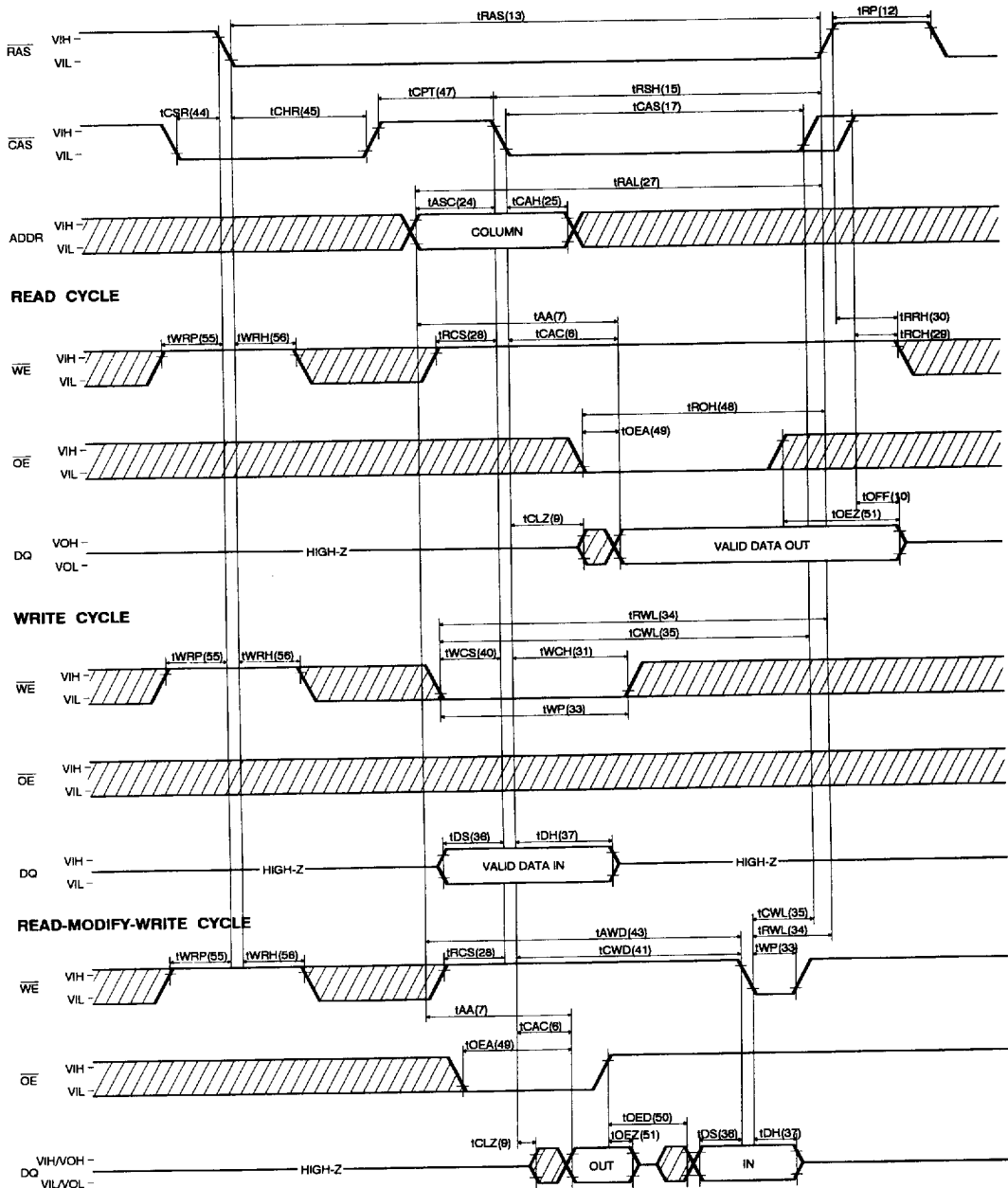
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE

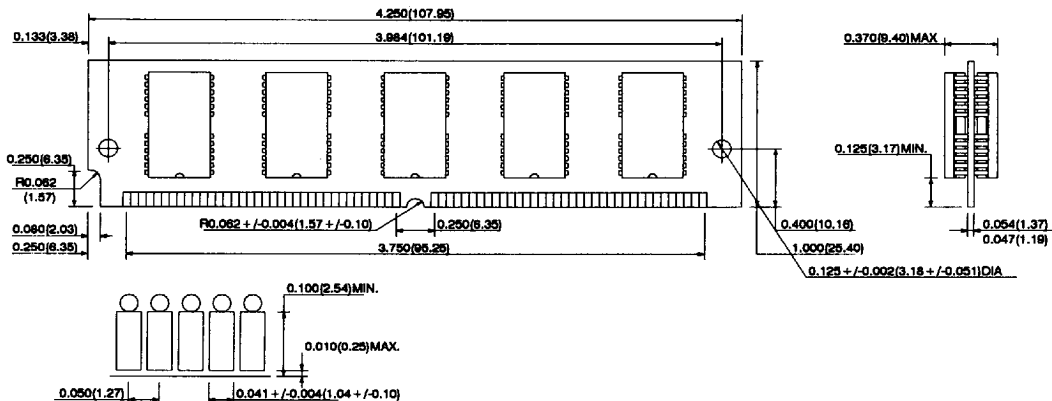


PACKAGE INFORMATION

72 pin Single In-line Memory Module (M ; Tin-Lead platedM, MG ; Gold plated)

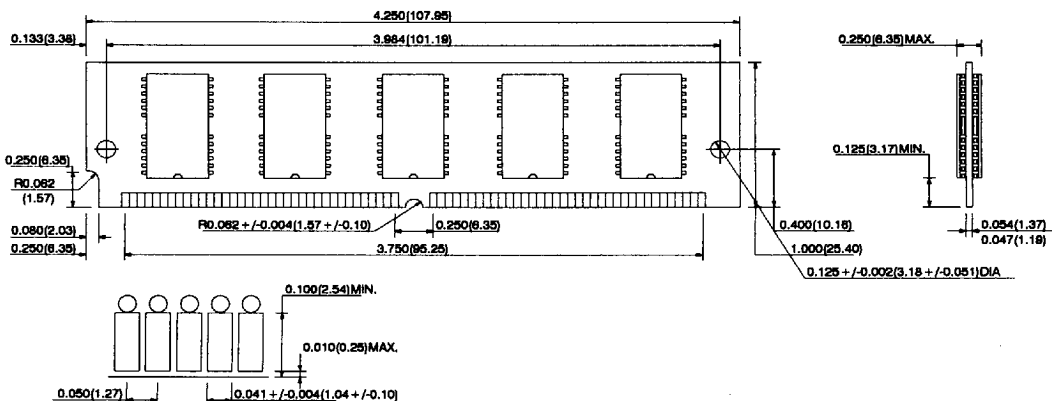
HYM540410M/LM (SOJ mounted)

UNIT : INCH(mm)
TOLERANCE : +/-0.005(0.13)



HYM540410TM/LTM (TSOP-II mounted)

UNIT : INCH(mm)
TOLERANCE : +/-0.005(0.13)



ORDERING INFORMATION

PART NUMBER	SPEED	POWER	PACKAGE	PLATING
HYM540A410M	60/70/80		SIMM	Tin-Lead
HYM540A410LM	60/70/80	L-part	SIMM	Tin-Lead
HYM540A410TM	60/70/80		SIMM	Tin-Lead
HYM540A410LTM	60/70/80	L-part	SIMM	Tin-Lead
HYM540A410MG	60/70/80		SIMM	Gold
HYM540A410LMG	60/70/80	L-part	SIMM	Gold
HYM540A410TMG	60/70/80		SIMM	Gold
HYM540A410LTMG	60/70/80	L-part	SIMM	Gold