

DESCRIPTION

The HYM536810 is a 8M x 36-bit Fast page mode CMOS DRAM module consisting of sixteen HY5117400 in 24/28 pin SOJ or TSOP and eight HY514100A in 20/26 pin SOJ or TSOP II on a 72 pin glass-epoxy printed circuit board. 0.22 μ F decoupling capacitor is mounted for each DRAM.

The HYM536810M/LM/TM/LTM are Tin-Lead plated and HYM536810MG/LMG/TMG/LTMG are Gold plated socket type Single In-line Memory Modules suitable for easy interchange and addition of 32M byte memory.

FEATURES

- Low power dissipation

Max. battery back-up 61.6mW (L-part)

Max. CMOS standby 44.0mW (L-part)
132.0mW

Max. TTL standby 264.0mW

Max. operating

Speed	Power
60	8.27W
70	7.28W

- Single power supply of 5V $\pm$ 10%

- TTL compatible inputs and outputs

- Fast access time

Speed	tRAC	tCAC	tPC
60	60ns	15ns	40ns
70	70ns	20ns	45ns

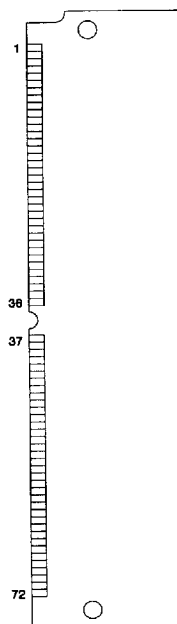
- Fast page mode operation

- CAS-before-RAS, RAS-only, Hidden refresh

- 2048 refresh cycles / 256ms (L-part)

2048 refresh cycles / 32ms

PIN CONNECTION



PIN DESCRIPTION

RAS0-RAS3	Row Address Strobe
CAS0-CAS3	Column Address Strobe
WE	Write Enable
A0-A10	Address Input
DQ0-DQ35	Data Input/Output
PD1-PD4	Presence Detect
VCC	Power (+ 5V)
VSS	Ground

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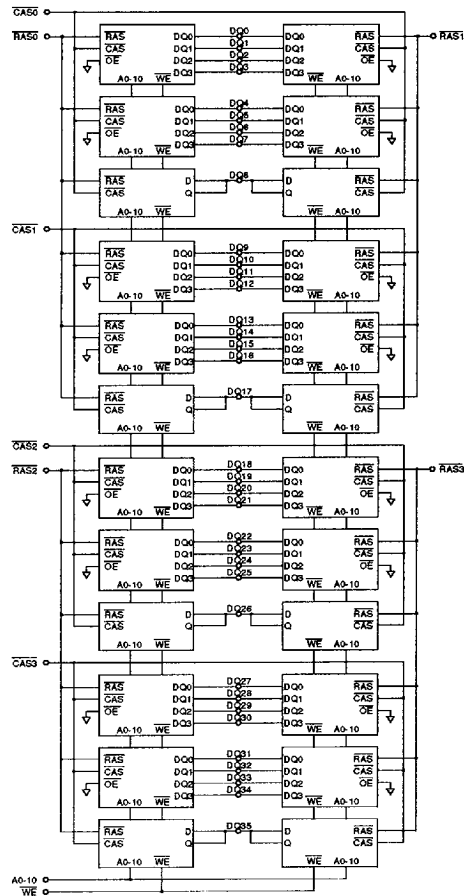
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PIN NAME

#	NAME	#	NAME
1	Vss	37	DQ17
2	DQ0	38	DQ35
3	DQ18	39	Vss
4	DQ1	40	CAS0
5	DQ19	41	CAS2
6	DQ2	42	CAS3
7	DQ20	43	CAS1
8	DQ3	44	RAS0
9	DQ21	45	RAS1
10	VCC	46	NC
11	NC	47	WE
12	A0	48	NC
13	A1	49	DQ9
14	A2	50	DQ27
15	A3	51	DQ10
16	A4	52	DQ28
17	A5	53	DQ11
18	A6	54	DQ29
19	A10	55	DQ12
20	DQ4	56	DQ30
21	DQ22	57	DQ13
22	DQ5	58	DQ31
23	DQ23	59	Vcc
24	DQ6	60	DQ32
25	DQ24	61	DQ14
26	DQ7	62	DQ33
27	DQ25	63	DQ15
28	A7	64	DQ34
29	NC	65	DQ16
30	Vcc	66	NC
31	A8	67	PD1
32	A9	68	PD2
33	RAS3	69	PD3
34	RAS2	70	PD4
35	DQ26	71	NC
36	DQ8	72	Vss

BLOCK DIAGRAM



PRESENCE DETECT PIN

PIN	-60	-70
PD1	NC	NC
PD2	Vss	Vss
PD3	NC	Vss
PD4	NC	NC

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
TA	Ambient Temperature	0 to 70	°C
TSTG	Storage Temperature	-55 to 150	°C
VIN, VOUT	Voltage on Any Pin Relative to VSS	-1.0 to 7.0	V
VCC	Voltage on VCC Relative to VSS	-1.0 to 7.0	V
Ios	Short Circuit Output Current	50	mA
Pd	Power Dissipation	9.2	W

NOTE : Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(TA = 0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
VCC	Supply Voltage	4.5	5.0	5.5	V
VIH	Input High Voltage	2.4	-	VCC + 1.0	V
VIL	Input Low Voltage	-1.0	-	0.8	V

NOTE : All voltages are referenced to VSS.

DC CHARACTERISTICS

(TA = 0°C to 70°C, VCC = 5V ± 10%, VSS = 0V, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED/ POWER	MIN.	MAX.	UNIT	NOTE
ILI	Input Leakage Current (Any Input Pin)	VSS ≤ VIN ≤ VCC + 1.0, All other pins not under test = VSS		-240	240	μA	
ILO	Output Leakage Current (High Impedance State)	VSS ≤ VOUT ≤ VCC, RAS & CAS at VIH		-10	10	μA	
ICC1	VCC Supply Current, Operating	trc = trc (min.)	60 70	-	1504 1324	mA	1,2,3
ICC2	VCC Supply Current, TTL Standby	RAS & CAS at VIH, other inputs ≥ VSS		-	48	mA	
ICC3	VCC Supply Current, RAS-only refresh	trc = trc (min.)	60 70	-	1504 1324	mA	1,3
ICC4	VCC Supply Current, Fast Page mode	tpc = tpc (min.)	60 70	-	844 764	mA	1,2,3
ICC5	VCC Supply Current, CMOS Standby	RAS & CAS ≥ VCC - 0.2V	L-part	-	24 8.0	mA	5
ICC6	VCC Supply Current, CAS-before-RAS refresh	trc = trc (min.)	60 70	-	1504 1324	mA	1,3
ICC7	VCC Supply Current, Battery Back Up (L-part only)	trc = 125μs, CAS = CBR cycling or 0.2V WE = VCC - 0.2V A0-A10 = VCC - 0.2V or 0.2V DQ0-DQ35 = VCC - 0.2V, 0.2V, or open	trAS ≤ 300ns	-	7.2	mA	1,4,5
			trAS ≤ 1μs	-	11.2		
VOL	Output Low Voltage	IOL = 4.2mA		-	0.4	V	
VOH	Output High Voltage	IOH = -5mA		2.4	-	V	

NOTE :

1. ICC1, ICC3, ICC4, ICC6 and ICC7 depend on cycle rate.
2. ICC1 and ICC4 depend on output loading. Specified values are obtained with the output open.
3. It depends on user whether column address is changed or not at least once while RAS = VIL and CAS = VIH.
4. Only trAS(max.) = 1μs is applied to refresh of battery backup but trAS(max.) = 10μs is applied to normal functional operation.
5. ICC5(max.) = 4.0mA and ICC7 are applied to L-part only (HYM536810LM, HYM536810LTM, HYM536810LMG and HYM536810LTMG).

AC CHARACTERISTICS

(TA = 0°C to 70°C, VCC = 5V ± 10%, VSS = 0V, unless otherwise noted.) NOTE : 1, 2, 3

#	SYMBOL	PARAMETER	HYM536810 M-series				UNIT	NOTE
			-60		-70			
			MIN.	MAX.	MIN.	MAX.		
1	tRC	Random Read or Write Cycle Time	110	-	130	-	ns	
2	tRPC	RAS to CAS Precharge Time	5	-	5	-	ns	
3	tPC	Fast Page Mode Cycle Time	40	-	45	-	ns	
4	tRHCP	Time from CAS Precharge	35	-	40	-	ns	
5	tRAC	Access Time from RAS	-	60	-	70	ns	4,9,10
6	tCAC	Access Time from CAS	-	15	-	20	ns	4,9
7	tAA	Access Time from Column Address	-	30	-	35	ns	4,9,10
8	tCPA	Access Time from CAS Precharge	-	35	-	40	ns	4
9	tCLZ	CAS to Output Low Impedance	0	-	0	-	ns	4
10	tOFF	Output Buffer Turn-off Delay	0	15	0	20	ns	5
11	tT	Transition Time (Rise and Fall)	3	50	3	50	ns	3
12	tRP	RAS Precharge Time	40	-	50	-	ns	
13	tRAS	RAS Pulse Width	60	10K	70	10K	ns	
14	tRASP	RAS Pulse Width (Fast Page Mode)	60	400K	70	400K	ns	
15	tRSH	RAS Hold Time	15	-	20	-	ns	
16	tCSH	CAS Hold Time	60	-	70	-	ns	
17	tCAS	CAS Pulse Width	15	10K	20	10K	ns	
18	tRCD	RAS to CAS Delay	20	45	20	52	ns	9
19	tRAD	RAS to Column Address Delay Time	15	30	15	35	ns	10
20	tCRP	CAS to RAS Precharge Time	5	-	5	-	ns	
21	tCP	CAS Precharge Time	10	-	10	-	ns	
22	tASR	Row Address Set-up Time	0	-	0	-	ns	
23	tRAH	Row Address Hold Time	10	-	10	-	ns	
24	tASC	Column Address Set-up Time	0	-	0	-	ns	
25	tCAH	Column Address Hold Time	15	-	15	-	ns	
26	tAR	Column Address Hold Time from RAS	50	-	55	-	ns	
27	tRAL	Column Address to RAS Lead Time	30	-	35	-	ns	
28	tRCS	Read Command Set-up Time	0	-	0	-	ns	
29	tRCH	Read Command Hold Time Referenced to CAS	0	-	0	-	ns	6
30	tRRH	Read Command Hold Time Referenced to RAS	0	-	0	-	ns	6
31	twCH	Write Command Hold Time	15	-	15	-	ns	
32	twCR	Write Command Hold Time from RAS	50	-	55	-	ns	
33	tWP	Write Command Pulse Width	15	-	15	-	ns	
34	tRWL	Write Command to RAS Lead Time	15	-	20	-	ns	
35	tcWL	Write Command to CAS Lead Time	15	-	20	-	ns	
36	tDS	Data-In Set-up Time	0	-	0	-	ns	7
37	tDH	Data-In Hold Time	15	-	15	-	ns	7
38	tdHR	Data-In Hold Time Referenced to RAS	50	-	55	-	ns	
39	tREF	Refresh Period (2048 cycles)	-	32	-	32	ms	
		L-part	-	256	-	256	ms	11
40	twCS	Write Command Set-up Time	0	-	0	-	ns	8

AC CHARACTERISTICS

(continued)

Continued

#	SYMBOL	PARAMETER	HYM536810 M-series				UNIT	NOTE
			-60		-70			
			MIN.	MAX.	MIN.	MAX.		
41	tCSR	CAS Set-up Time (CBR Cycle)	10	-	10	-	ns	
42	tCHR	CAS Hold Time (CBR Cycle)	10	-	15	-	ns	
43	tCPT	CAS Precharge Time (CBR Counter Test)	30	-	35	-	ns	
44	tWRP	WE to RAS Precharge Time (CBR Cycle)	10	-	10	-	ns	
45	tWRH	WE to RAS Hold Time (CBR Cycle)	10	-	10	-	ns	

NOTE :

1. An initial pause of 200 μ s is required after power-up followed by 8 RAS cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 CAS-before-RAS initialization cycles instead of 8 RAS-only refresh cycles are required. The device should carefully initialized to be prevented from being entered into multi bit test mode.
2. $V_{IH}(\text{min.})$ and $V_{IL}(\text{max.})$ are reference levels for measuring timing of input signals. Transition time is measured between V_{IH} and V_{IL} and assumed to be 5ns for all inputs.
3. Refer to the HY5117400 and HY514100A data sheet for detailed information.
4. Measured with a load equivalent to 2 TTL loads and 100pF.
5. $t_{OFF}(\text{max.})$ defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
7. These parameters are referenced to CAS leading edge in early write cycles.
8. tw_{CS} is not a restrictive operating parameter. It is included in the data sheet as electrical characteristics only. If $tw_{CS} \geq tw_{CS}(\text{min.})$, the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle.
9. Operation within the $t_{RCD}(\text{max.})$ limit insures that $t_{RAC}(\text{max.})$ can be met. $t_{RCD}(\text{max.})$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD}(\text{max.})$ limit, then access time is controlled by t_{CAC} .
10. Operation within the $t_{RAD}(\text{max.})$ limit insures that $t_{RAC}(\text{max.})$ can be met. $t_{RAD}(\text{max.})$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD}(\text{max.})$ limit, then access time is controlled by t_{AA} .
11. $t_{REF}(\text{max.}) = 256\text{ms}$ is applied to L-part only (HYM536810LM, HYM536810LTM, HYM536810LMG and HYM536810LTMG).

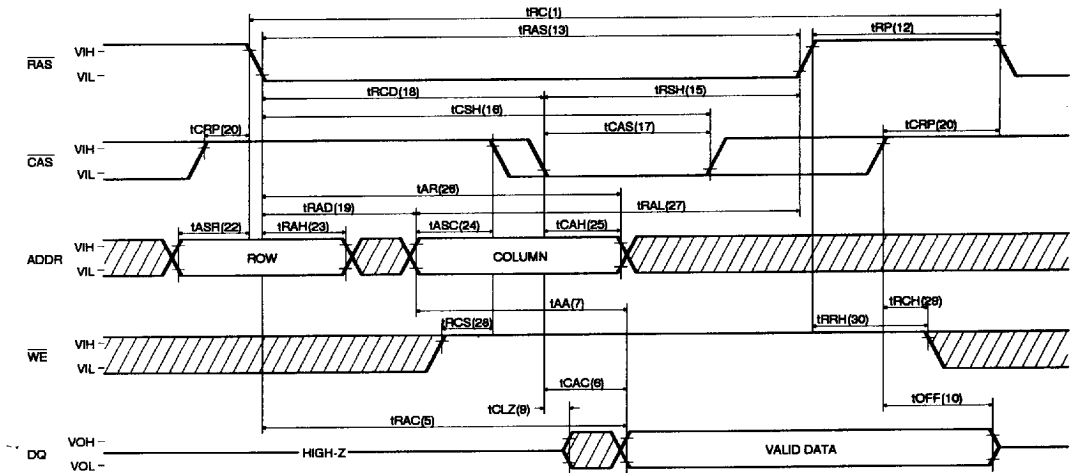
CAPACITANCE

($T_A = 25^\circ\text{C}$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, $f = 1\text{MHz}$, unless otherwise noted.)

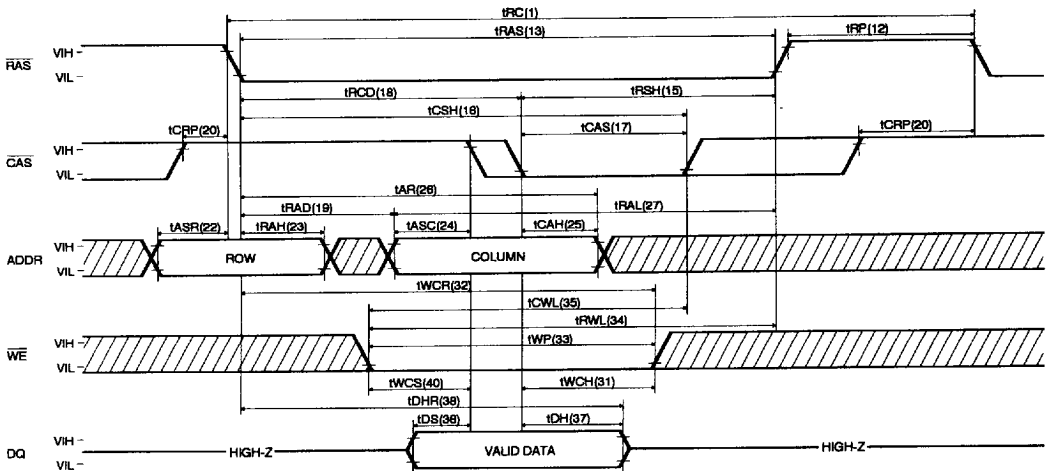
SYMBOL	PARAMETER	TYP.	MAX.	UNIT
CIN1	Input Capacitance (A0-A10)	-	161	pF
CIN2	Input Capacitance (WE)	-	174	pF
CIN3	Input Capacitance (RAS0-RAS3)	-	46	pF
CIN4	Input Capacitance (CAS0-CAS3)	-	46	pF
CDQ1	Data Input/Output Capacitance (DQ0-7,9-16,18-25,27-34)	-	29	pF
CDQ2	Data Input/Output Capacitance (DQ8,17,26,35)	-	39	pF

TIMING DIAGRAM

READ CYCLE



EARLY WRITE CYCLE



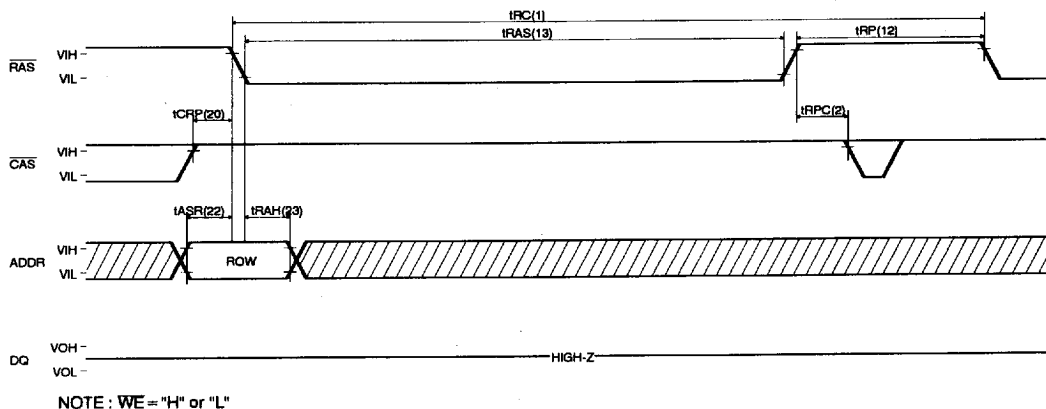
The timing diagram illustrates the relationship between the RAS, CAS, ADDR, WE, and DO signals. Key timing parameters include:

- RAS:** $t_{RASP}(14)$ (RAS pulse width), $t_{RHP}(4)$ (RAS hold time), $t_{RCP}(20)$ (RAS to CAS setup time), $t_{RSH}(16)$ (RAS to SH setup time), $t_{RCH}(29)$ (RAS to CH setup time), $t_{RRH}(30)$ (RAS to RH hold time).
- CAS:** $t_{CAS}(17)$ (CAS pulse width), $t_{CSP}(21)$ (CAS to CP setup time), $t_{CCH}(25)$ (CAS to CH setup time), $t_{CSC}(24)$ (CAS to SC setup time), $t_{CRH}(29)$ (CAS to RH setup time), $t_{CCH}(25)$ (CAS to CH setup time).
- ADDR:** $t_{ASQ}(22)$ (ASQ pulse width), $t_{ASD}(24)$ (ASD pulse width), $t_{ASCH}(25)$ (ASCH pulse width), $t_{ASQ}(22)$ (ASQ pulse width), $t_{ASD}(24)$ (ASD pulse width), $t_{ASCH}(25)$ (ASCH pulse width), $t_{ASQ}(22)$ (ASQ pulse width), $t_{ASD}(24)$ (ASD pulse width), $t_{ASCH}(25)$ (ASCH pulse width).
- WE:** $t_{WCS}(28)$ (WCS pulse width), $t_{WCH}(29)$ (WCH pulse width), $t_{WRH}(30)$ (WRH pulse width), $t_{WCH}(29)$ (WCH pulse width).
- DO:** $t_{DOF}(10)$ (DOF pulse width), $t_{DOZ}(9)$ (DOZ pulse width), $t_{DOF}(10)$ (DOF pulse width), $t_{DOZ}(9)$ (DOZ pulse width).

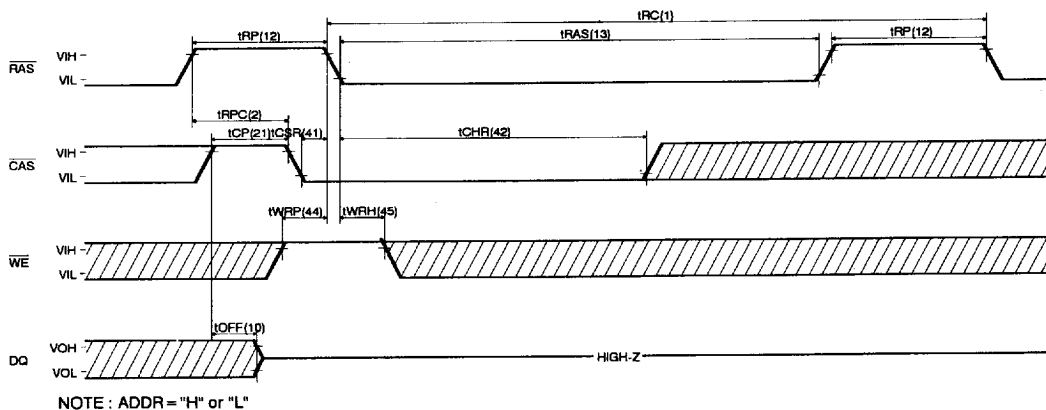
The timing diagram illustrates the sequence of signals for the 64K1602 LCD controller. The signals shown are RAS, CAS, ADDR, WE, and DQ. The diagram is divided into three main sections, each representing a different data transfer phase. The timing parameters are defined as follows:

- RAS:** $t_{RASP}(14)$ (RAS pulse width), $t_{RHP}(4)$ (RAS hold time), $t_{ICRP}(20)$ (RAS to ICRP delay), $t_{IRP}(12)$ (RAS to IRP delay).
- CAS:** $t_{CSH}(16)$ (CAS hold time), $t_{ICAS}(17)$ (CAS to ICRP delay), $t_{ICP}(21)$ (CAS to ICP delay), $t_{IRSH}(15)$ (CAS to IRSH delay), $t_{ICAS}(17)$ (CAS to ICRP delay), $t_{ICRP}(20)$ (CAS to ICRP delay).
- ADDR:** $t_{ASR}(22)$ (ADDR setup time), $t_{RAH}(23)$ (ADDR hold time), $t_{ASC}(24)$ (ADDR to ICRP delay), $t_{CAH}(25)$ (ADDR to ICRP delay), $t_{ASC}(24)$ (ADDR to ICRP delay), $t_{CAH}(25)$ (ADDR to ICRP delay), $t_{ASC}(24)$ (ADDR to ICRP delay), $t_{CAH}(25)$ (ADDR to ICRP delay).
- WE:** $t_{WCS}(40)$ (WE setup time), $t_{WCH}(31)$ (WE hold time), $t_{WIP}(33)$ (WE to ICRP delay), $t_{WCR}(32)$ (WE to ICRP delay), $t_{DHR}(38)$ (WE to ICRP delay).
- DQ:** $t_{DS}(36)$ (DQ setup time), $t_{DH}(37)$ (DQ hold time), $t_{DS}(36)$ (DQ to ICRP delay), $t_{DH}(37)$ (DQ to ICRP delay), $t_{DS}(36)$ (DQ to ICRP delay), $t_{DH}(37)$ (DQ to ICRP delay).

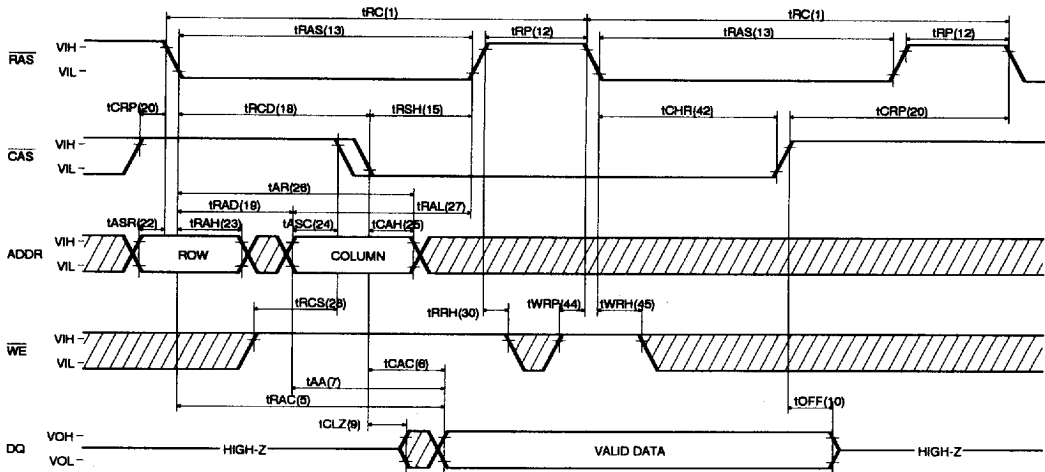
RAS-ONLY REFRESH CYCLE



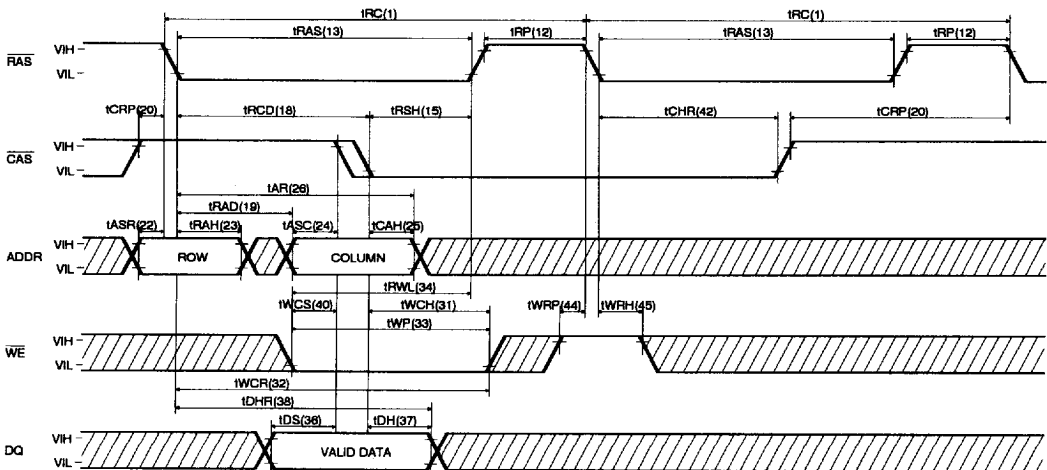
CAS-BEFORE-RAS REFRESH CYCLE



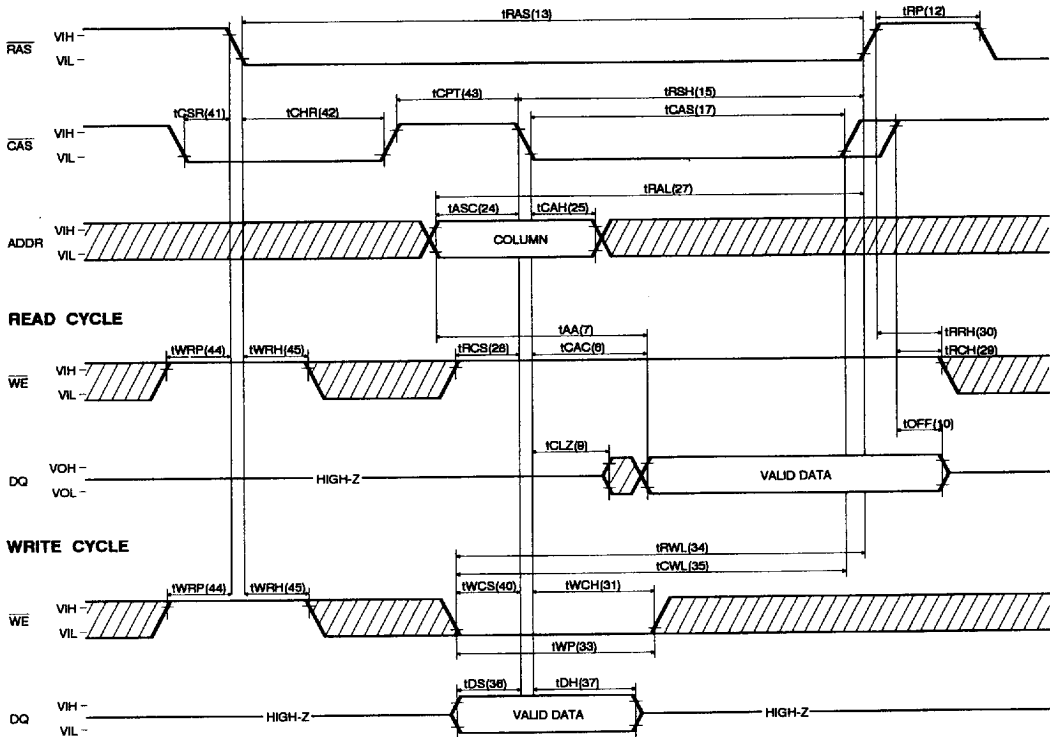
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)

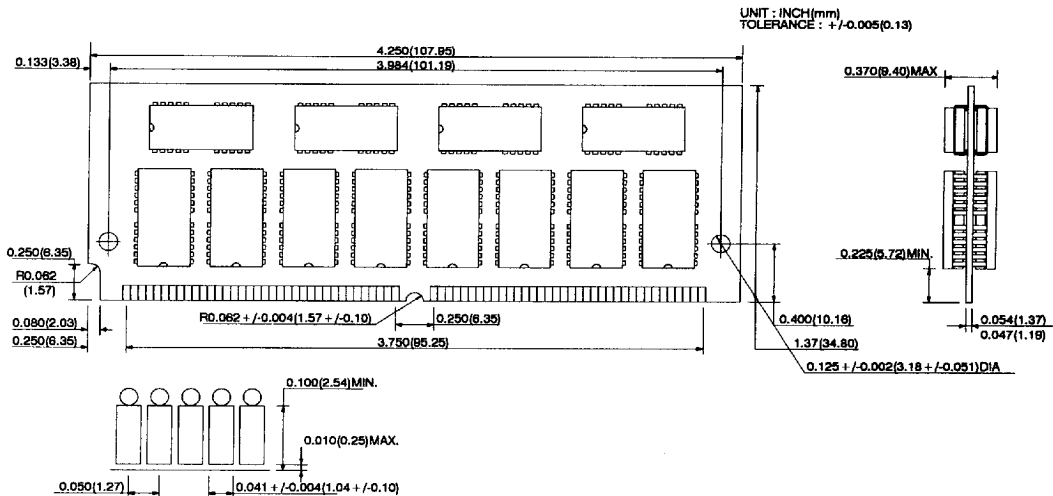


CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE

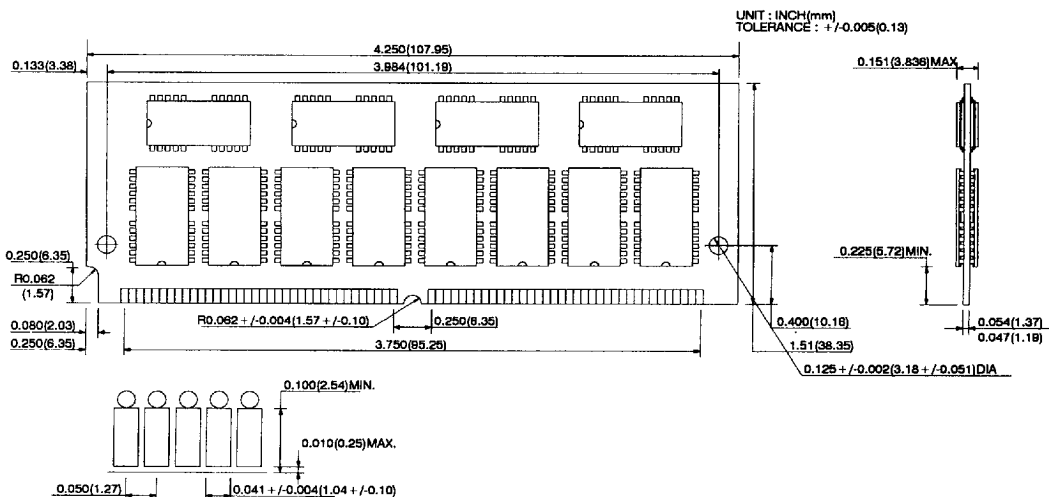


PACKAGE INFORMATION

**72 pin Single In-line Memory (M ; Tin-Lead plated, MG ; Gold plated)
HYM536810/L (SOJ Mounted)**



HYM536810T/LT (TSOPII Mounted)



ORDERING INFORMATION

PART NUMBER	SPEED	POWER	PACKAGE	PLATING
HYM536810M	60/70		SIMM	Tin-Lead
HYM536810LM	60/70	L-part	SIMM	Tin-Lead
HYM536810TM	60/70		SIMM	Tin-Lead
HYM536810LTM	60/70	L-part	SIMM	Tin-Lead
HYM536810MG	60/70		SIMM	Gold
HYM536810LMG	60/70	L-part	SIMM	Gold
HYM536810TMG	60/70		SIMM	Gold
HYM536810LTMG	60/70	L-part	SIMM	Gold