EQ6600

EQuality Clock Chip

Eleven Output, Zero Propagation Delay Clock Distribution Chip

April, 1995
Patent Pending

Features

- Operates from 30 MHz to 170 MHz with any variable frequency reference clock input
- Near-zero propagation delay (+/- 300 ps Max)
- All digital circuitry for ease of design
- Pin-to-pin output skew of 250 ps (Max)
- 3.3 V only and 5 volt options
- 10 symmetric, TTL-compatible outputs with 16 mA drive with rise and fall times of 1.4ns (Max)
- Meets or exceeds Pentium™ processor timing requirements
- Period to period jitter: 75 ps (Typ)
- Typical applications include low skew clock distribution for motherboards, CPU boards, and multi-CPU board applications.

General Description

The PLX EQuality clock chip generates near-zero propagation delay high fidelity clock outputs referenced to an input oscillator or crystal.

The chip's all digital implementation allows equal low skew clock output performance between any clock outputs across one or more EQuality clock chips.

The EQuality clock chip permits any variable frequency reference clock input to be distributed.

In addition, the chip's digital algorithm and design, as compared with analog designs, provide higher noise tolerance, lower power and ease of design.

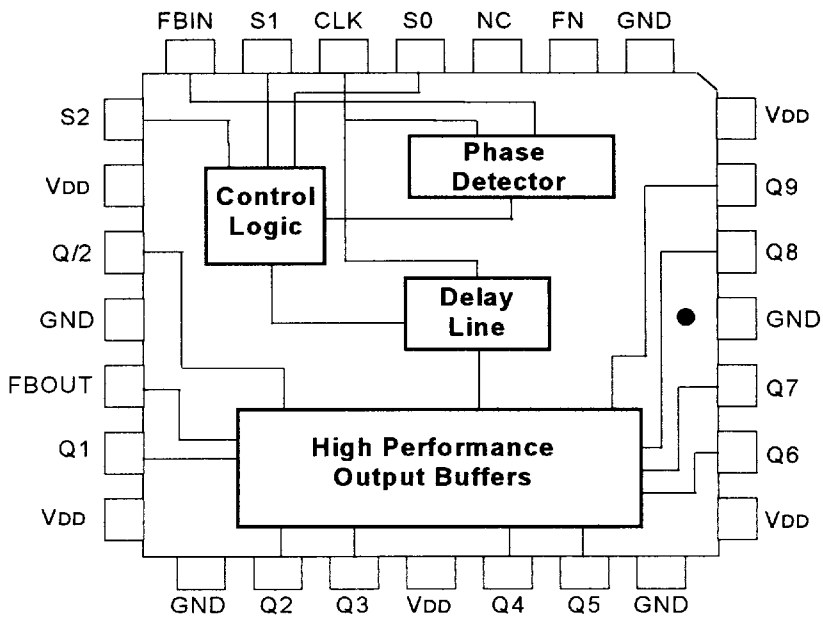


Figure 1. Block Diagram

Table of Contents

SECTION 1 - INTRODUCTION

The PLX EQuality clock chip generates multiple de-skewed copies of a reference clock which is a crystal or oscillator input. These clock copies or clock outputs from the EQuality chip all have equal high precision performance with respect to skew, rise and fall times, jitter and frequency tolerance. Typical applications for this type of clock generation are motherboards and CPU adapters which have a requirement for high fidelity CPU or system clock distribution from a reference clock.

The PLX EQuality clock chip achieves high fidelity de-skewed clock output performance by using a proprietary digital algorithm instead of a conventional analog phase lock loop technique. The digital algorithm provides near zero propagation delay (+/- 300 ps) from clock input to clock output.

Internal compensation logic digitally matches the delay or skew between the input clock and the clock outputs. In addition, the near zero propagation delay algorithm eliminates chip process variations which contribute to propagation delay and skew. This implementation, in addition to providing the performance, allows ease of design and flexibility.

Typical high performance clock distribution chips use active compensation techniques. The most common technique is the use of the analog PLL, or phase lock loop. PLL implementations typically require expensive process technologies and analog circuit design. The PLL's circuitry functions by internally regenerating the clock frequency input (or fractions thereof). The clock outputs require a highly constrained PCB design environment to maintain precise, stable low noise clock generation. The board designer may have to incorporate analog design techniques.

The EQuality chips' digital design allows the designer to utilize the chip like a regular digital chip. 850 ps chip to chip clock output skew can be achieved. In addition, the CMOS EQuality clock chip consumes low power and generates minimal noise compared with bipolar and Gallium Arsenide implementations. 3.3 volt only Vdd power supply is an option.

SECTION 2 - EQUALITY CLOCK CHIP FUNCTIONS

1. **Variable frequency operation from 30 MHz to 170 MHz.** The EQuality clock chip distributes copies of any variable frequency reference clock input from 30 MHz to 170 MHz.
2. **Near zero propagation delay.** The reference clock input to clock output delay is +/- 300 ps.
3. **All digital implementation.** The EQuality clock chip contains no analog circuitry. No special analog design techniques are required.
4. **Clock output skew of 250 ps (max).** Skew is measured from any clock output pin to any other clock output pin.
5. **Period to period clock ouput jitter of 75 ps (Typ).**
6. **Output buffer rise/fall times of 1.4 ns (max).** These are measured with the AC load circuit in Section 7 and .5 ns input rise/fall time signal.
7. **Output buffer current drive of 16 ma.**
8. **28 pin PLCC package.**
9. **Low power operation.** The EQuality clock chips' clock outputs can instantaneously switch to a DC state. This is ideal for low power PC design or for "Green" PCs. The digital implementation does not use internal high power consuming high frequency oscillators. The standby power consumption is less than 100 mW.
10. **Inherent noise tolerance.** The EQuality clock chips' all digital design has improved noise tolerance compared to analog or PLL counterparts.
11. **Distribution of clock signals of arbitrary duty cycle.** Since the EQuality clock chip copies the input reference frequency rather than regenerating the input clock frequency, the EQuality clock chip distributes the same duty cycle as the reference clock input.
12. **Low chip to chip clock output skew.** The EQuality clock chip is capable of many low skew clock copies with chip to chip connections (see figure 4).
13. **3.3 volt only or 5 volt power supply option.** The EQuality clock chip can operate off of a 5 volt or 3.3 volt power supply. All Vdd connections can be 3.3 volt only. In addition, if a 3.3 volt power supply is used, the EQuality clock chip can accept 5 volt or 3.3 volt input signals.
14. **Enhanced Mode operation.** The EQuality clock chip has a mode to configure half the clock outputs at half the frequency of the input reference clock.

SECTION 3 - EQUALITY CLOCK CHIP PIN OUT

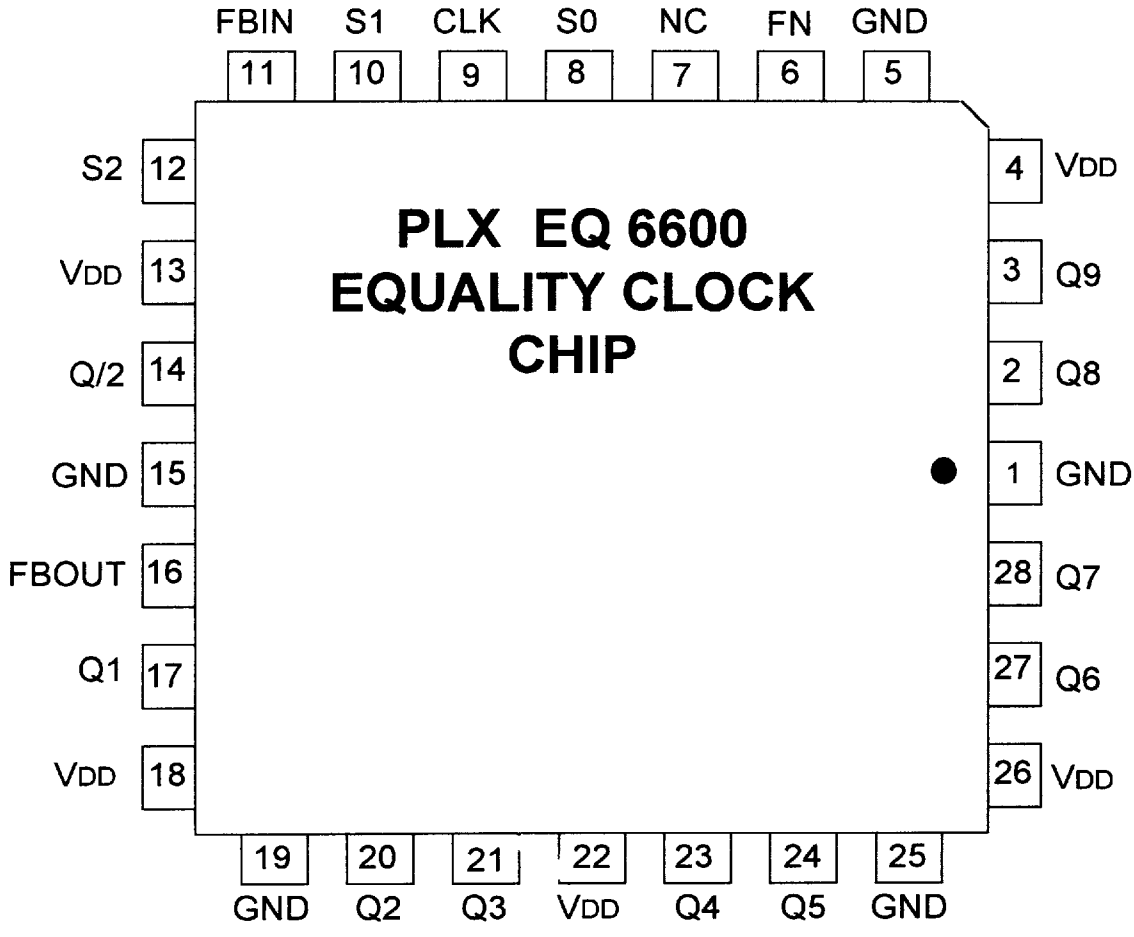


Figure 2. Pin Out

SECTION 4 - PIN DESCRIPTION

Pin Summary

Abbreviations used:

I - Input Pin Only O - Output Pin Only TP - Totem Pole Pin	**Note:** **IN** - Input is a standard input only signal. **OUT** - Totem pole output is a standard active driver.

Table 1 EQuality Clock Chip Functional Pins

Pin Name	Number of Signals	Input/ Output	Pin Type	Pin Drive (mA)
CLK	1	I	IN	
S[0-3]	3	I	IN	
Q[1-9]	9	O	TP	16
Q/2	1	O	TP	16
FBIN	1	I	IN	
FBOUT	1	O	TP	16
FN	1	I	IN	
TOTAL PINS	**17**			

Table 2 Power, Ground, and No Connections

Pin Name	Number of Signals	Input/ Output	Pin Type	Pin Drive (mA)
NC	1	-	-	-
VDD	5	I	-	-
GND	5	I	-	-
TOTAL PINS	**11**			

Table 3 EQuality Clock Chip Functional Pin Description

Symbol	Signal Name	I/O	Pin Number	Function
CLK	Reference clock input	I	9	Crystal or oscillator input.
S[0-2]	Mode control pins	I	8,10,12	Sets the EQuality clock chip into functional and test modes.
Q[1-9]	Clock output pins	O	17,20,21,23,24,27 28,2,3	Clock output buffers which replicate the CLK input with high fidelity.
Q/2	Half frequency clock output pin	O	14	Clock output buffer which replicates the CLK input with high fidelity at one half the frequency.
FBIN	Feedback input pin	I	11	Signal which gives the phase detector the phase difference between the CLK and clock outputs. Externally tied to FBOUT.
FBOUT	Feedback output pin	O	16	A clock output buffer signal which is used exclusively to connect to FBIN input for output buffer phase detection.
FN	Fine mode input pin	I	6	Sets fine mode if input is connected to Vdd. Fine mode is +/- 300 ps Tpd propagation delay. If input is not connected, NC, or is connected to GND, then the coarse mode is set. Coarse mode has an unspecified delay > +/- 300 ps.

Table 4 Power, Ground, and No Connect Pin Description

Symbol	Signal Name	I/O	Pin Number	Function
VDD	Power	I	4,13,18,22,26	Five volt power supply pins
GND	Ground	I	1,5,15,19,25	Ground pins
NC	No Connect	-	7	None

SECTION 5 - EQUALITY CLOCK CHIP FUNCTIONALITY

The EQuality clock chip consists of control logic, a phase detector, a delay line and the high performance buffers. The control logic, phase detector and delay line comprise the digital algorithm for near zero propagation delay clock output delays. The high performance buffers generate the equal performance high fidelity clock outputs.

The EQuality clock chips' pinouts consist of the clock outputs Q1-9 and Q/2, control pins S0-2, clock input CLK, and feedback pins FBIN and FBOUT.

The clock input can be any reference frequency generator such as a crystal or oscillator. Note that the EQuality clock chip replicates any duty cycle that is input to the CLK pin. The clock ouputs, Q1-9, replicate the CLK clock signal with high fidelity at the same frequency of the CLK input. The clock output, Q/2, replicates the CLK input with high fidelity at one half the frequency of the CLK input. Depending on the mode setting, the clock outputs Q1-3 can also replicate the reference clock input, CLK, at one half the the frequency.

The clock output buffers are rated to drive clock signals with rise/fall times of 1.4 ns with the AC load circuit designated in Section 7.

The two feedback signals, FBIN and FBOUT, should be connected together for proper operation of the phase detector and delay line. The phase detector monitors the phase difference between FBIN and the reference clock, CLK. This feedback path allows the digital algorithm to make the appropriate phase adjustments relative to the delay line to match the clock outputs with CLK. The loading and trace length on the short circuit trace between FBIN and FBOUT should be minimized. The trace length should be less than 12 inches.

The fine mode pin, FN, sets the EQuality clock chip to fine propagation delay of +/- 300 ps if the input is connected to Vdd. FN sets the EQuality clock chip to coarse propagation delay if the input is no connected, NC, or connected to GND.

The control signals, S0-2, provide the mode settings for the EQuality clock chip (please see Table 5). The S0-2 inputs can be tied to VDD or GND depending on the desired mode. Mode 000 (S2-0 = 000) is reserved. Mode 001 is a diagnostic mode used only by PLX. Mode 010 is the enhanced mode where Q1-3 is driving clock outputs half the frequency of CLK and Q4-9 drives clock outputs at the same frequency of CLK. Modes 011,100,110, and 111 are the standard mode with Q1-9 driving clock outputs at the same frequency as CLK. Mode 101 is a test mode where the delay line is set to the minimum delay value and the propagation delay between CLK and the clock outputs, Q/2, Q1-9, and FBOUT, can be measured.

Two or more clock EQuality chips can be driven from the same reference clock and drive multiple clock outputs with 850 ps skew across chip to chip outputs. One design rule must be observed to achieve this. The reference clock trace lengths to the inputs to the EQuality chips must match the FBIN and FBOUT connection trace lengths. All trace lengths and impedance loads must be equal. This gives the designer EQuality clock output driver performance for many clock loads.

The EQuality clock chip requires a synchronization time of 50 us typically for the algorithm to match the delay between FBIN and CLK. After the synchronization time, near zero propagation delay from CLK to clock outputs will be achieved.

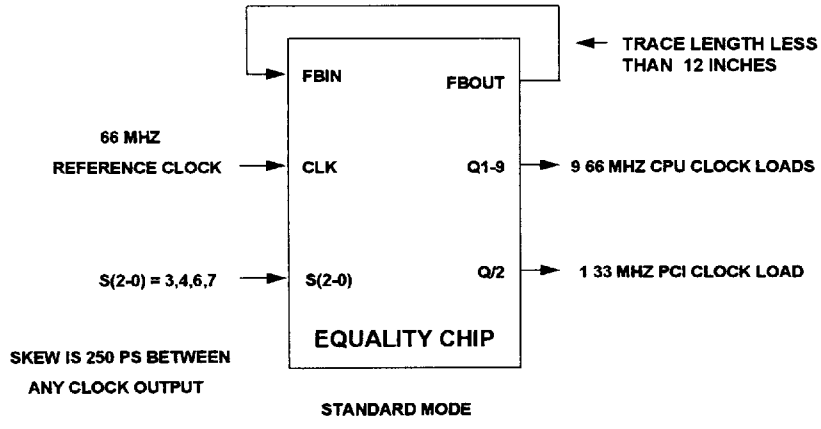
Since the EQuality clock chip is all digital, there are no internal high power consuming high frequency voltage controlled oscillators or other analog circuits. This allows the EQuality clock chip to be an ideal clock distribution chip for low power or "Green" PC environments. All clock outputs instantaneously switch to a DC value upon power down.

3.3 volt Vdd operation is an option for the EQuality clock chip. In addition, if a 3.3 volt operation power supply is used, the EQuality clock chip can accept 5 volt or 3.3 volt inputs.

Table 5 EQuality Clock Chip Mode Slection

S2	S1	S0	CLK	Q/2	Q1-3	Q4-9	COMMENTS
0	0	0					Reserved.
0	0	1	30-170 MHz	CLK/2	CLK	CLK	Diagnostic mode. Reserved for factory testing.
0	1	0	30-170 MHz	CLK/2	CLK/2	CLK	Enhanced mode. Sets Q1-3 to drive clock outputs at one half the frequency of CLK.
0	1	1	30-170 MHz	CLK/2	CLK	CLK	Standard mode. Sets Q1-3 to drive clock outputs at the same frequency as CLK.
1	0	0	30-170 MHz	CLK/2	CLK	CLK	Standard mode. Sets Q1-3 to drive clock outputs at the same frequency as CLK.
1	0	1	0-170 MHz	CLK/2	CLK	CLK	Test mode. Sets the progation delay between CLK and the clock outputs to a minimum value for measurement.
1	1	0	30-170 MHz	CLK/2	CLK	CLK	Standard mode. Sets Q1-3 to drive clock outputs at the same frequency as CLK.
1	1	1	30-170 MHz	CLK/2	CLK	CLK	Standard mode. Sets Q1-3 to drive clock outputs at the same frequency as CLK.

SECTION 6 - EQUALITY CLOCK CHIP IMPLEMENTATIONS



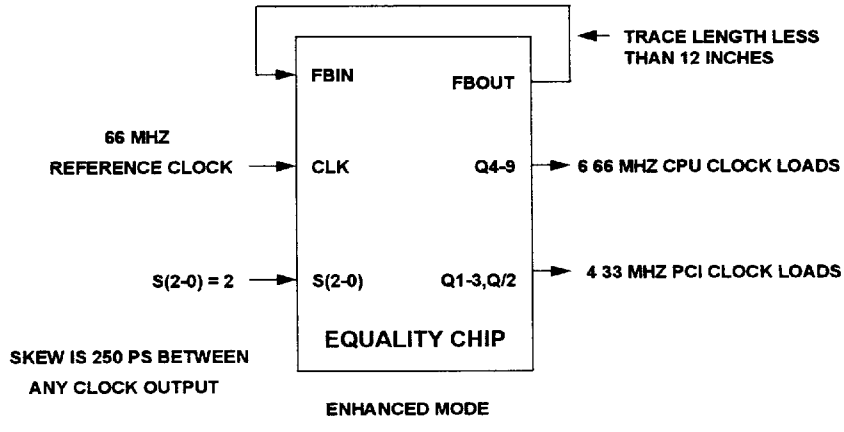


Figure 3. Chip Modes

The above show typical implementations for standard and enhanced modes

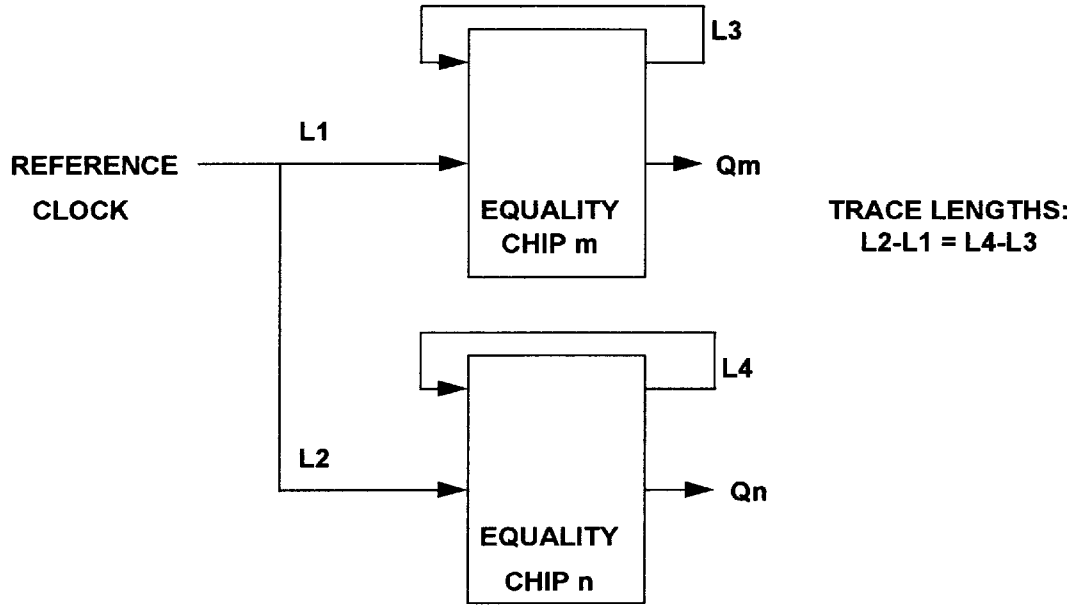
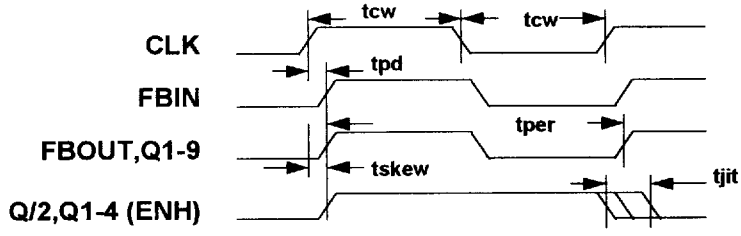


Figure 4. Driving Many Clock Loads

Application for driving many clock loads with multiple EQuality clock chips

Skew between Qm and Qn is 850ps (fine) if RC of Qm and Qn are equal

SECTION 7 - ELECTRICAL SPECIFICATIONS AND MAXIMUM RATINGS



AC TEST CIRCUIT

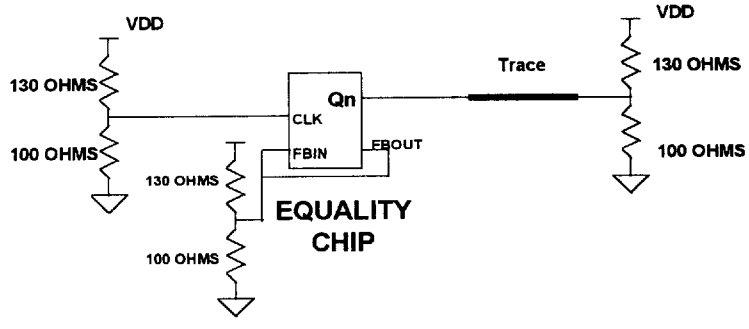


Figure 5. AC Timings

Table 6 AC Timings *** Please see ordering information**

		Min	Typ	Max
Fclk*	CLK frequency	30 Mhz	-	170 Mhz
tper	CLK and output period (Q/2 is two times the value)	5.8 ns	-	33 ns
tcw	CLK pulse width	5.8 ns	-	-
tir	CLK input rise time (0.8 - 2.0 V)	-	-	2.0 ns
tr/tf	Output rise and fall times (0.8 - 2.0 V)	.5 ns	-	1.4 ns
tpd	CLK to FBIN (or Qn) delay for fine delay setting	-300 ps	0	+300 ps
tvih	Minimum input high voltage	3.0 v	-	-
tskew	Skew between Q/2, Q1-9, and FBOUT (1.5 V)	-125 ps	-	+125 ps
tsw	Output switching window	-	100 ps	250 ps
tsynch	Output synchronization time	-	50 us	200 us
tdcyc	Output duty cycle variation (@ 1.8v)	-10%		+10%
tjit	output period to period jitter (RMS)	-	75 ps	-
Pac	Typical AC power consumption	-	3 ma/Mhz	-

Absolute Maximum Ratings

Storage Temperature	-65 °C to +150 °C
Ambient Temperature with Power Applied	-55 °C to +125 °C
Supply Voltage to Ground	-0.5V to +7.0V
Input Voltage (VIN)	VSS - 0.5V VDD + 0.5V
Output Voltage (VOUT)	VSS - 0.5V VDD + 0.5V

Operating Ranges

Ambient Temperature	Supply* Voltage (VDD)	Input Voltage (VIN)
0 °C to +70 °C	5V +/- 5% 3.3V +/- .3V	Min = VSS Max = VDD

* See ordering information

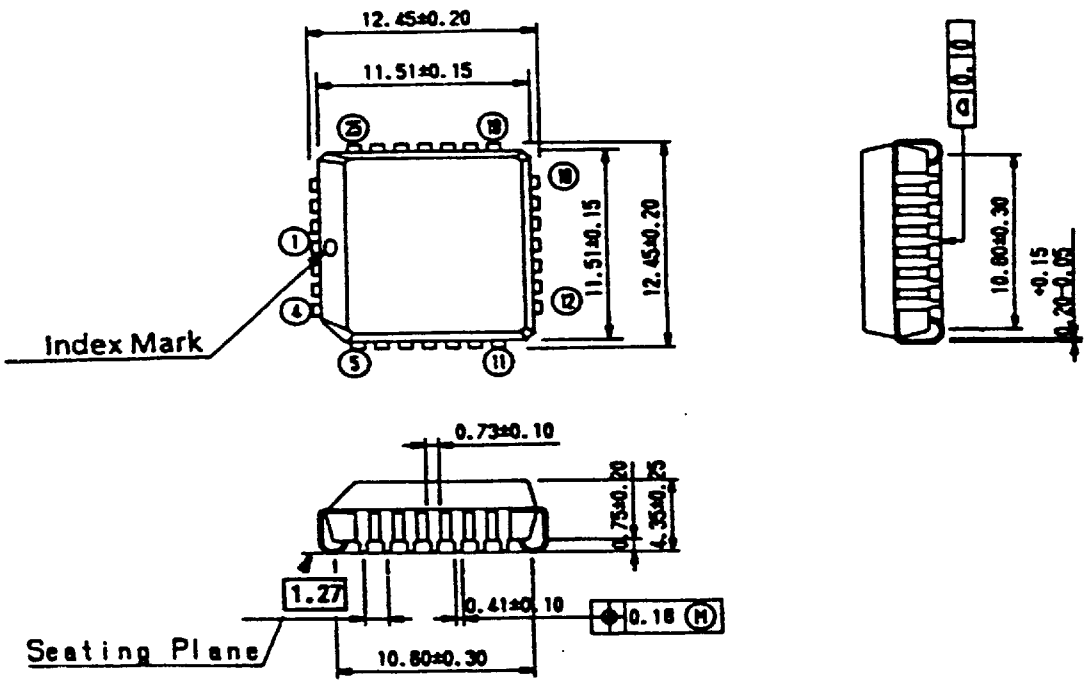
Capacitance (sample tested only)

Parameter	Test Conditions	Pin Type	Typical Value	Units
CIN	VIN = 2.0V f = 1 MHz	Input	5	pF
COUT	VOUT = 2.0V f = 1 MHz	Output	10	pF

DC Electrical Characteristics Tested Over Operating Range

Para-meter	Description	Test Conditions		Min	Max	Units
VOH	Output High Voltage	VDD = Min,	IOH = -16 mA	2.4		V
VOL	Output Low Voltage	VIN = VIH or VIL	IOL per Table 16 ma		0.4	V
VIH	Input High Level			2.0		V
VIL	Input Low Level			-0.3	0.8	V
ILI	Input Leakage Current	VSS ≤ VIN ≤ VDD VDD = Max		-10	+10	µA
IOZ	Tri-state Output Leakage Current	VDD = Max VSS ≤ VIN ≤ VDD		-10	+10	µA
ICC	Power Supply Current	VDD = Max Quiescent DC Mode			20	mA
ISC	Short Circuit Current			-130		

SECTION 8 - PACKAGE MECHANICAL DIMENSIONS



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SECTION 9 - ORDERING INFORMATION

Part Markings

EQ6600	80 Mhz: Input reference clock rated up to 80 Mhz (5 volt only)
EQ6600-L1	100 Mhz: Input reference clock rated up to 100 Mhz (3.3 and 5 volt operation)
EQ6600-L3	133 Mhz: Input reference clock rated up to 133 Mhz (3.3 and 5 volt operation)
EQ6600-L7	170 Mhz: Input reference clock rated up to 170 Mhz (3.3 volt operation only)

Clock Distribution IC Selection - A Primer

I. Introduction

Clocks and clock distribution networks are essential to any digital system. Clock distribution networks may be as simple as a single crystal connected to a flip flop or as complicated as hundreds of precise active compensation ICs providing multiple phase gated clocks to hundreds of high density ICs with internal clock distribution networks on multiple boards. The clock distribution network impacts the performance, cost, reliability, and design of the client digital system.

Closely related to clock distribution ICs are clock synthesis ICs. These ICs are designed to take an input clock at some fixed frequency and provide a number of clocks at some other fixed frequencies. These ICs may provide the input clocks to clock distribution ICs.

The goal of a clock distribution network is to provide the number of required clocks with the needed frequencies and phases at the necessary tolerances.

While it is straightforward to design a clock distribution network which provides the number and types of clocks required, it is the tolerances on these clocks which will determine whether the system will operate with no timing problems at the desired performance level. The tolerances on clocks include the jitter and the skew from an ideal phase position. All clocks may or may not require the same tolerances.

The key consideration to clock distribution IC selection is the tolerances necessary on the clocks.

II. The Importance of Tolerance

The effect of clock tolerance on system performance is easy to understand. A 50 MHz system is equivalent to a 20 ns clock period. If the tolerance on the clocks is 4 ns or 20% then only 16 ns are available for reliable logic operations and interconnect delay. If an SRAM access is to be performed, a 12 ns SRAM would leave 4 ns for address setup and interconnect delay.

If the tolerance on the clocks is 500 ps or 2.5%, then 19.5 ns would be available for reliable logic operation and interconnect delay. The clock period could be reduced to 16.5 ns, frequency increased to 60.6 MHz, or the 12 ns SRAM could be changed to a 15 ns SRAM and still leave 4.5 ns for address setup and

interconnect delay. This example illustrates how a higher precision clock distribution network can lead to higher performance or a net cost savings.

Perhaps the most important impact of clock tolerance is on system reliability. Clocks which have more skew or jitter than anticipated will lead to very hard to trace timing problems. These timing problems will often manifest themselves as sporadic system crashes when some program or hardware is used.

The determination of what clock tolerance is adequate must be made from a detailed timing analysis of the complete system. The min./max. specification of each IC which requires a clock and the electrical characteristics of the system packaging including board and connectors must be considered. In practice, the worst paths are usually readily known and are used as the driving requirement.

Timing problems can usually be identified if the failing system will run when all clocks are slowed down but will not run at full speed. This easy identification technique may not work if any of the software is using a clock for timing loop.

III. Choices in Clock Distribution ICs

The simplest clock distribution ICs are 244, 245 type of buffers. These ICs may introduce several ns of clock tolerance across multiple parts. Pin to pin skew are not specified but may be 1 ns for adjacent pins. For low frequency clocks, less than 20 MHz, these ICs are probably adequate. The next step up are buffers optimized for clock distribution. These may be the 805, 806 or similar types of 1 to 5 to 1 to 9 buffers. These buffers have tighter specification for pin to pin skew and part to part skew. For systems where all critical clocks may be supplied from one IC, these ICs are suitable.

The final choice of clock distribution ICs are active compensation ICs. These ICs are mostly PLLs, phase locked loop, with an internal analog VCO, voltage controlled oscillator. The only known alternative to the PLL ICs is the PLX Technology EQuality 6600 IC. The common feature of these active compensation ICs is the use of a feedback input to allow the IC to sample external conditions and adjust its outputs. The typical connection is to connect one of the outputs to the feedback input. This allows the IC to adjust the outputs until they are in phase with the reference input, resulting in effectively a zero propagation delay buffer.

The pin to pin skew of the active ICs are similar to the pin to pin skew of the optimized passive buffer clock ICs. The part to part skew is much better because of the zero propagation delay effect of the feedback input. For any clock distribution network where one IC cannot supply all of the critical clocks, the active compensation ICs are the only choice.

The key consideration in deciding which class of ICs to select is the number of critical clocks. A critical clock is typically a clock with skew tolerance of less than

1 ns. In practice the designer may not be certain of the number of critical clocks. The common temptation of attaching variable number of ICs to different clock nets and unexpected movement of ICs during board placement make the tolerance of critical clocks hard to monitor. High frequency, greater than 67 MHz, systems and/or multiple processors are likely candidates for active ICs.

IV. Advantages of Feedback

Even in designs where all of the critical clocks can be supplied from one IC, the feedback input of active ICs allows an additional degree of design option not possible with passive clock buffers. Figure 1. shows a very simple pipeline stage with a register supplying the address to a SRAM and another register holding the data. With the active IC connected as shown, the clock edge will be positioned to coincide with address being valid. This automatic alignment effectively gives the data register more time for the SRAM access.

With a passive clock buffer, the clock edge will be earlier and part of the clock cycle will be used by the clock to Q and Q to output delays of the register. While the clock line to the data register could be lengthened to give more time to the SRAM access, the active IC allows this adjustment to be made automatically according to the actual characteristic of the address register instead of a fixed estimation. Note that only the EQuality 6600 may be used in this manner because the feedback is half the frequency of the reference input.

PLL ICs require the feedback to be the same frequency as the reference input. The EQuality 6600 employs a proprietary control technique which filters out the mismatch which will occur every other clock period in this case. Another similar usage for this automatic phase adjustment capability of active ICs is illustrated in Figure 2. In this case, the feedback is used to align external clocks with the internal clocks of a large ASIC. Large ASICs also have internal clock distribution networks. Because ASICs usually have large min/max on their internal cell delays, it is difficult to specify precisely the relationship between internal clocks and external clocks. In Figure 2. an internal clock is brought out of the ASIC and used as the feedback input. This allows the other clocks from the active clock IC to be adjusted in phase with the ASIC internal clock. The interconnect delays may need to be considered if the closest phase alignment is needed.

The feedback input of active ICs is extremely useful in allowing a modulation to be continuously and automatically applied to the clock outputs.

V. Problems With Active Compensation ICs

For all the advantages of active compensation ICs, there are a number of reasons why they are not more commonly used. The top 10 reasons are:

1. Noise sensitive. The analog VCOs in PLL ICs are controlled by small voltage variations. Noise going into the IC can easily cause failure to lock or excessive jitter. The result is worse performance than passive clock buffers.
2. Cost. PLL ICs are typically 3 to 5 times the cost of passive buffers. In addition, some PLL ICs require external loop filter components as well as separate analog power and ground planes.
3. Power consumption. The analog VCOs in PLL ICs are running at frequencies several times that of the reference frequency. The VCO is always oscillating at this high frequency, typically 200 MHz to 800 MHz. The result is high power consumption.
4. Frequency Gaps. PLL ICs needs to be switched or selected for different frequency bands. These frequency bands are usually not contiguous so certain frequencies cannot be used. This makes it hard to operate the system at various frequencies.
5. Jitter. PLL ICs have larger jitter than passive clock buffers due to the continuous adjustment of the internal analog VCO. These adjustments effectively cause greater clock to clock skew.
6. Clock stoppage. PLL ICs cannot stop the clock since the VCO must oscillate continuously. This makes power management difficult.
7. Voltage sensitivity. PLL ICs require close control over the supply voltage since the analog VCO is directly influenced by the supply voltage.
8. Process dependence. Since PLL ICs have analog VCOs which are designed and characterized for a particular process, it is difficult to migrate PLL ICs from process to process. This translate to difficulty in providing the advantages offered by new processes.
9. Integration complexity. The close dependence of PLL ICs on the semiconductor process and layout make PLLs difficult to integrate into larger ASICs.
10. PLL interaction. The continuous adjustment of a PLL IC's VCO make cascaded chains of PLLs unstable. Large amount of jitter may result from all the PLL ICs trying to adjust to changing inputs.

VI. The Beauty of EQuality 6600

Of course, the EQuality 6600 have all the advantages of active compensation clock ICs with none of the disadvantages of PLL ICs. None of the above 10 limitations apply to the EQuality 6600 due to the totally different approach used to design the IC.

EQuality 6600 is a wide frequency band, broad voltage range, low jitter, rugged and easy to use active compensation IC. Once the designer has determined that active clock ICs are necessary, the EQuality 6600 is a natural choice. The only current reasons to not use this IC is if frequency multiplication and phase shifting

capability is required. These additional capabilities will be available soon in the next members of the EQuality clock distribution family.

To summarize the above discussion:

A. If a system can accept clock tolerance, skew + jitter, greater than 4 ns then passive clock buffers are usable.
B. If a system needs clock tolerance, skew + jitter, less than 1 ns and the number of critical clocks are less than 9 and no automatic phase alignment is needed then passive clock buffers are usable. If automatic phase alignment is needed, then active ICs are needed.
C. If a system needs clock tolerance, skew + jitter, less than 1 ns and the number of critical clocks are more than 9 then active compensation clock buffers are necessary.
D. If the system tolerance is between 4 ns and 1 ns, and the number of clocks is less than 9 then passive buffers are usable.
E. If the system tolerance is between 4 ns and 1 ns, and the number of clocks over 67 MHz is more than 9 then active compensation clock buffers are necessary.
F. If it is not clear what the clock tolerance is or the number of critical clocks, then if the project schedule has time for a second design iteration then passive buffers may be used. If timing problems occur, either try to tweak the problems out or redesign using active buffers. If schedule is tight, then use active buffers for the initial design.

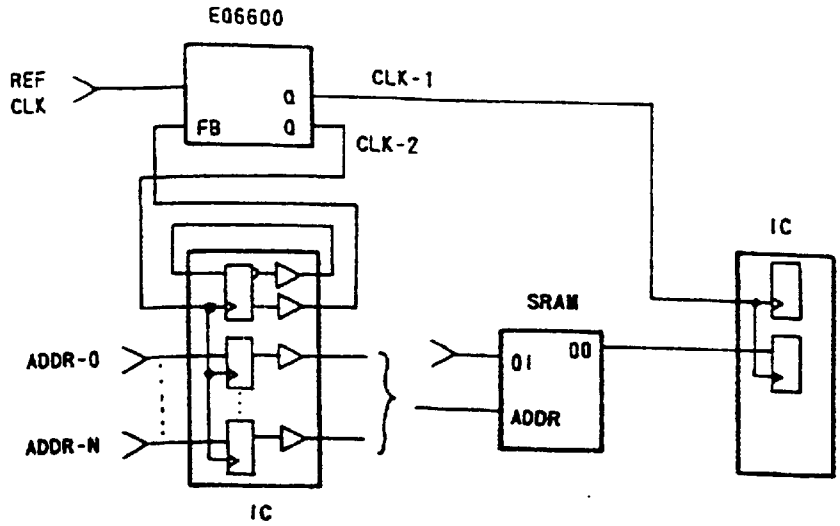

Figure 1.

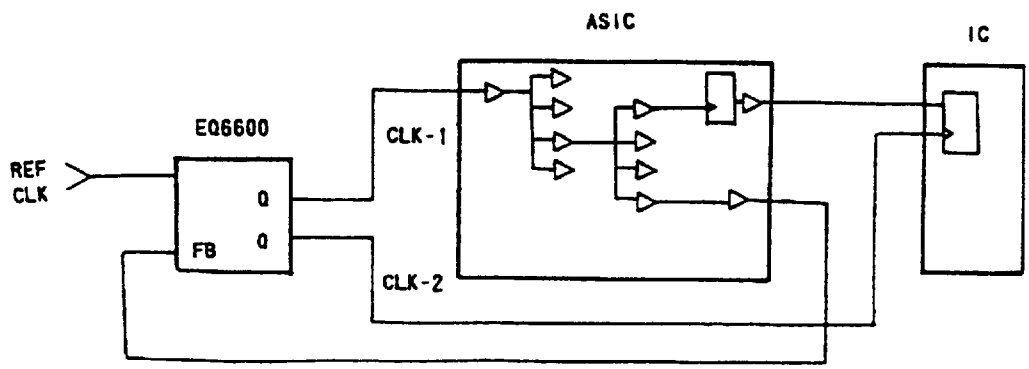

Figure 2.