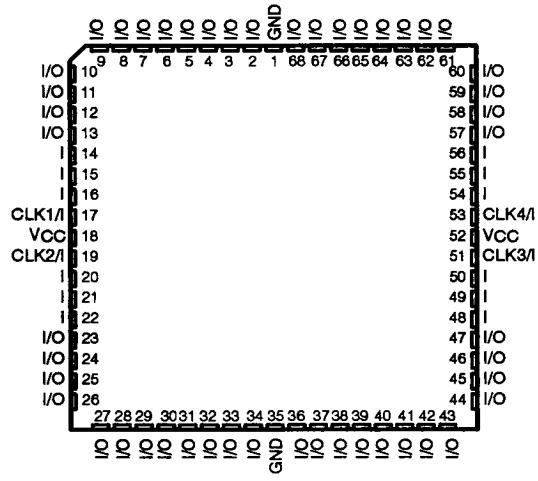
- **User-Configurable LSI Circuit Capable of Implementing 2100 Equivalent Gates of Conventional and Custom Logic**
- **High-Performance CMOS Process Allows:**
  Maximum t_{pd}: - 20C . . . 20 ns
  - 25C . . . 25 ns
  - 30C . . . 30 ns
  - 25I . . . 25 ns
  - 30I . . . 30 ns
- **Low Operating Current:**
  I_{CC} max (standby) . . . 150 µA
  I_{CC} max (turbo bit off) . . . 40 mA
  I_{CC} max (turbo bit on) . . . 225 mA
- **Programmable Clock Option Allows Asynchronous Clocking of All Registers or Banked Register Operation From 4 Synchronous Clocks**
- **Programmable Asynchronous Clear of All Registers**
- **Forty-Eight Macrocells With Configurable I/O Architecture Allowing for up to 64 Inputs and 48 Outputs**
- **Macrocell Flip-Flops can be Individually Programmed as D-, T-, JK-, SR-Type Flip-Flops or for Combinational Operation**
- **Programmable Design Security Bit Prevents Copying of Logic Stored in Device**
- **Available Third-Party Design and Programming Support**

FN PACKAGE
(TOP VIEW)



AVAILABLE OPTIONS

T_A RANGE	SPEED CLASS	PLASTIC CHIP CARRIER (PLCC)
0°C to 70°C	20 ns	EP1830-20CFN
	25 ns	EP1830-25CFN
–40°C to 85°C	25 ns	EP1830-25IFN
	30 ns	EP1830-30IFN

description

general

The EP1830 series of CMOS EPLDs from Texas Instruments offer LSI density, TTL equivalent speed performance and low power consumption. Each device is capable of implementing over 2100 equivalent gates of SSI, MSI, and custom logic circuits. The EP1830 series is packaged in a 68-pin J-leaded plastic (one-time programmable) Chip Carrier.

The EP1830 series is designed as an LSI replacement for traditional low-power Schottky TTL logic circuits. Its speed and density also make it suitable for high-performance complex functions such as dedicated peripheral controllers and intelligent support chips. Integrated-circuit count and power requirements can be reduced by several orders of magnitude allowing similar reduction in total size and cost of the system, with significantly enhanced reliability.

The EP1830 uses a 1.0 µm CMOS EPROM technology employing EPROM transistors to configure logic connections. The EPROM technology allows 100% generic testing (all devices are 100% tested at the factory).

Programming the EP1830 is made easy by the availability of third-party support for design entry, design processing and device programming.

The EP1830-20C and EP1830-25C devices are characterized for operation from 0°C to 70°C. The EP1830-25I and EP1830-30I are characterized for operation from −40°C to 85°C.

functional

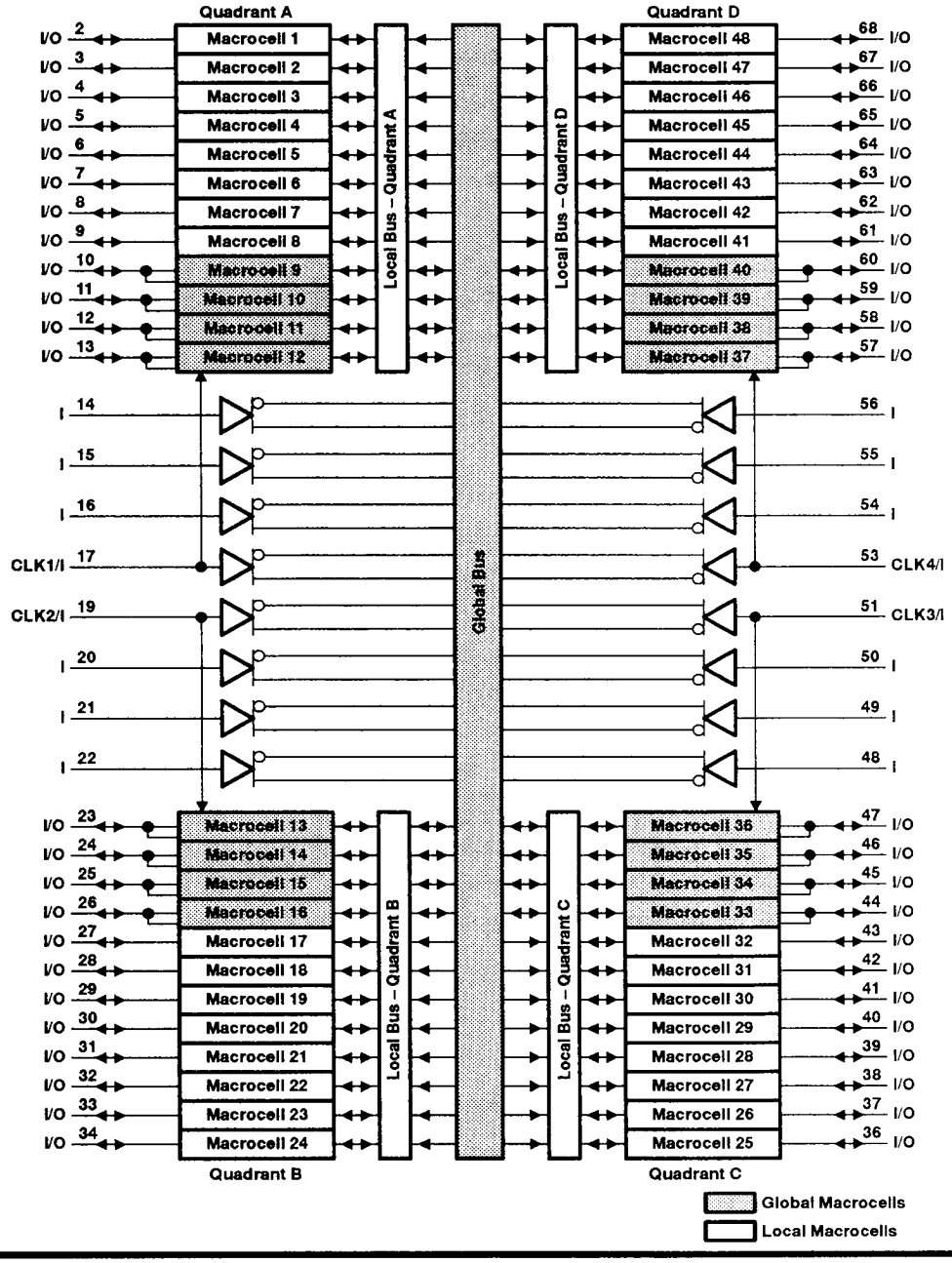
The EP1830 series use CMOS EPROM cells to configure logic functions within the device. The EP1830 architecture is 100% user configurable, allowing the device to accommodate a variety of independent logic functions. Externally, the EP1830 provides 16 dedicated data inputs, four of which may be used as system clock inputs. There are 48 I/O pins, which may be individually configured for input, output, or bidirectional data flow.

macrocells

The EP1830 architecture consists of a series of macrocells. All logic is implemented within these macrocells. Each macrocell, shown in Figure 1, contains three basic elements: a logic array, a selectable register element, and 3-state I/O buffer. All combinational logic such as exclusive-OR, NAND, NOR, AND, OR and inverted gates are implemented within the logic array. For register applications, each macrocell provides one of two possible flip-flop options: D or T. Third party software will allow design with JK or SR flip-flops, implementing these with the T flip-flop option. Each EP1830 macrocell is equivalent to over 40 2-input NAND gates.

The EP1830 is partitioned into four identical quadrants. Each quadrant contains 12 macrocells. Input signals into the macrocells come from the EP1830 internal bus structures. Macrocell outputs may drive the EP1830 external pins as well as the internal buses. Figure 2 illustrates a simple logic function that can be implemented within a single macrocell. Note that all combinational logic is implemented within the logic array, a JK flip-flop is selected, and the 3-state buffer is permanently enabled.

functional block diagram



Each EP1830 macrocell consists of 3 basic components (see Figure 1)

Step 1. A logic array for gated logic
Step 2. A flip-flop for data storage (selectable options include D, T and software emulated JK and SR). The flip-flop may be bypassed for purely combinational functions.
Step 3. A 3-state buffer to define input, output, or bidirectional data flow.

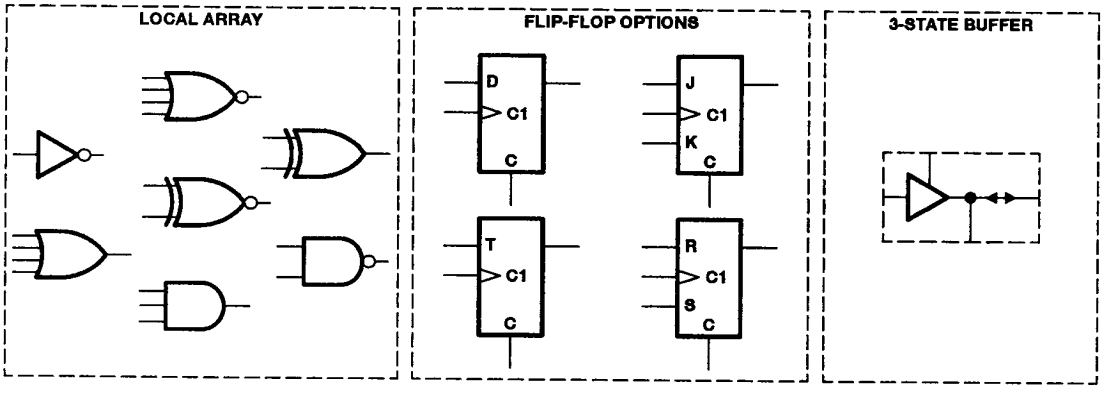


Figure 1. Marcocell Components

Typical logic function implemented into a single macrocell. Each EP1830 macrocell can accommodate the equivalent of 40 gates.

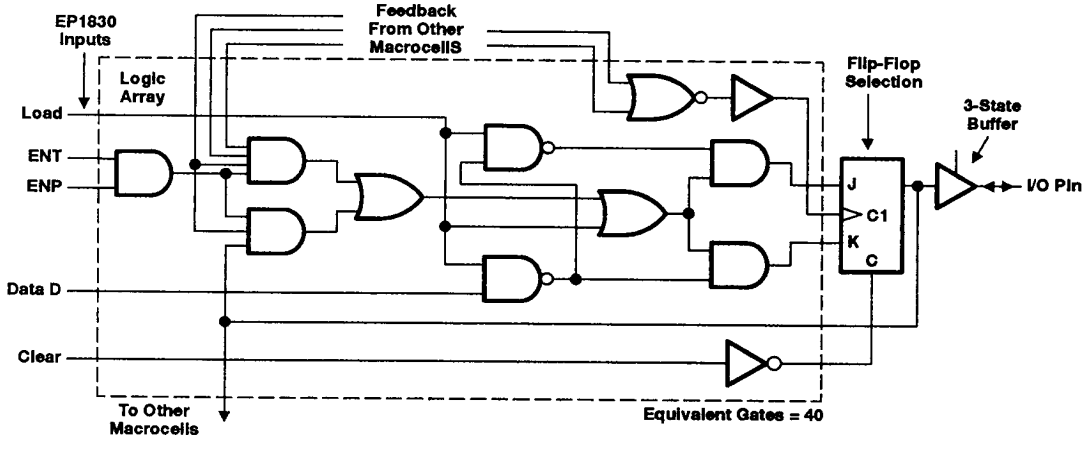


Figure 2. Sample Circuit

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The EP1830 macrocell architecture is shown in Figures 3 and 4. There are 32 macrocells called local macrocells. These macrocells offer a multiplexed feedback path (pin or internal) which drives the local bus of the respective quadrant.

There are another 16 macrocells known as the global macrocells (see Figure 4). These global macrocells have features that allow each macrocell to implement buried logic functions and at the same time serve as dedicated input pins. Thus the EP1830 may have an additional 16 input pins giving a total of 32 inputs. The global macrocells have the same timing characteristics as the local macrocells.

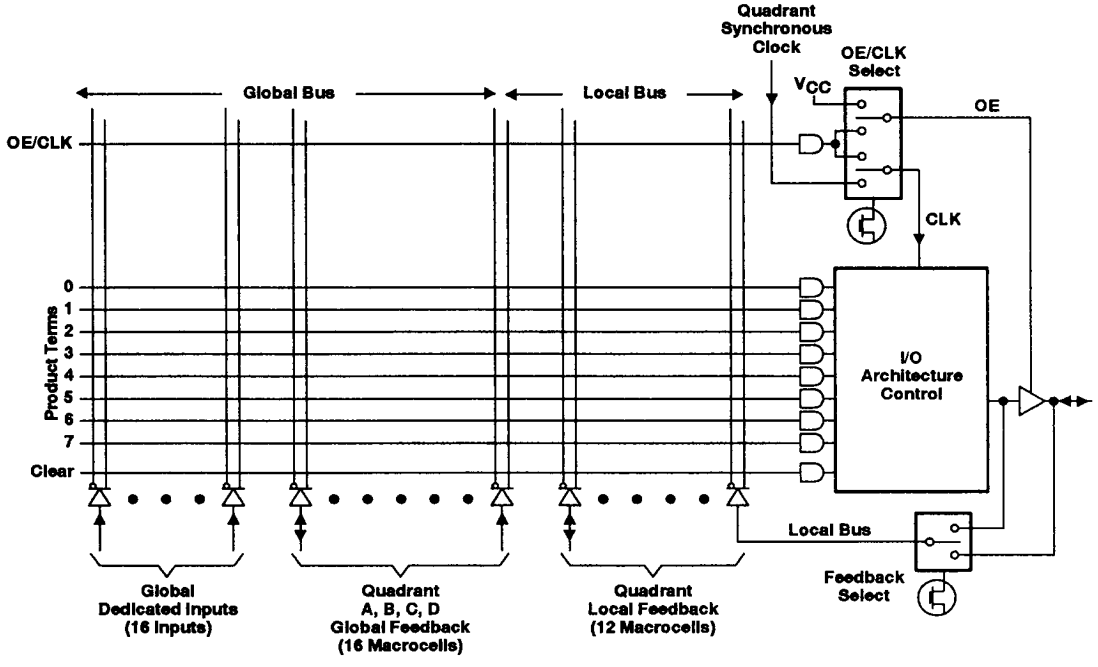


Figure 3. Local Macrocell Logic Array

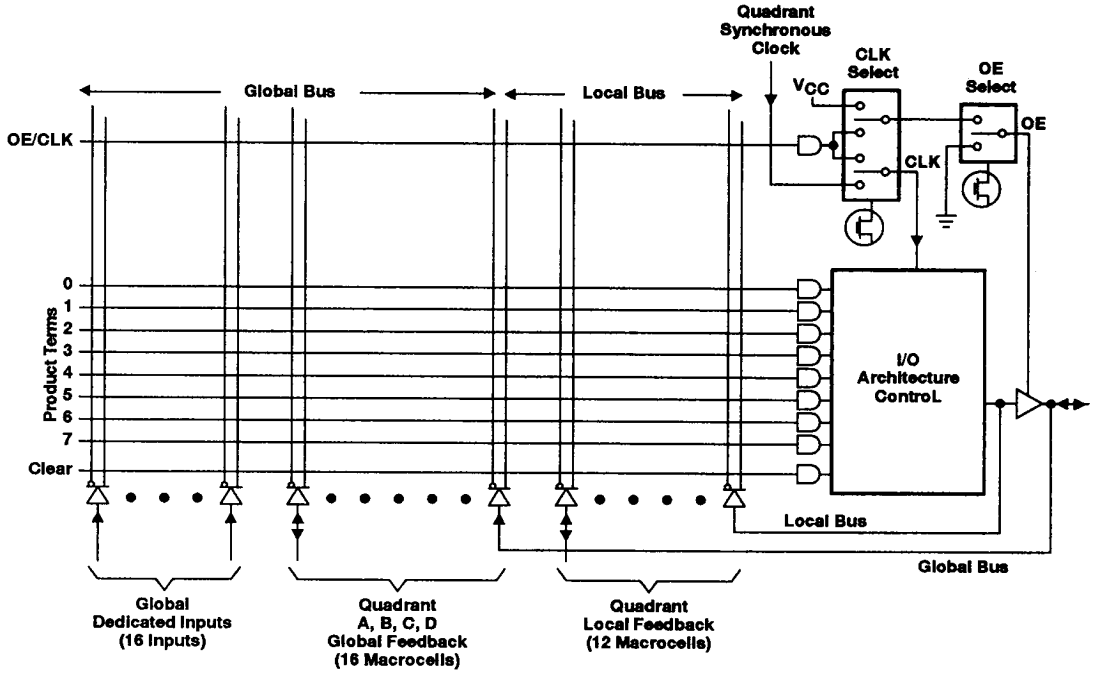


Figure 4. Global Macrocell Logic Array

clock options

Each of the EP1830 internal flip-flops may be clocked independently or in user defined groups. The architecture allows for asynchronous clocking using the OE/CLK product term to provide input or internal logic functions as a clock. If this mode is used the output enable buffer cannot be controled by this product term. The flip-flops can be configured for positive or negative edge triggered operation with asyncronous clock mode.

Four dedicated system clocks (CLK1 thru CLK4) also provide clock signals to the flip-flops. System clocks are connected directly from the EP1830 external pins. With this direct connection, system clocks give enhanced clock to output delay times than internally operated clock signals. There is one system clock per EP1830 quadrant. When using system clocks, the flip-flops are positive edge triggered (data transitions occur on the rising edge of the clock).

third party design support

Texas Instruments is working in conjunction with several software manufacturers to provide excellent design software support for the EP1830. This support ranges from high level design entry compilers to schematic capture programs in which the designer may implement his design with standard TTL SSI and MSI based circuits such as counters, comparators, shift registers, etc. Please contact Texas Instruments applications hotline at (214) 997-5666 for current status of third-party programming support.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V_{CC} (see Note 1) ..... –0.3 V to 7 V
Instantaneous supply voltage range, V_{CC} ($t \leq 20$ ns) ..... –2 V to 7 V
Programming supply voltage range, V_{PP} ..... –0.3 V to 14 V
Instantaneous programming supply voltage range, V_{PP} ($t \leq 20$ ns) ..... –2 V to 14 V
Input voltage range, V_I ..... –0.3 V to 7 V
Instantaneous input voltage range, V_I ($t \leq 20$ ns) ..... –2 V to 7 V
V_{CC} or GND current range ..... –300 mA to 300 mA
Continuous total power dissipation at or below 25°C free-air temperature (see Note 2) ..... 1500 mW
Operating free-air temperature, T_A ..... –65°C to 135°C
Storage temperature range ..... –65°C to 150°C

NOTES: 1. All voltage values are with respect to GND terminal.
2. For operation above 25°C free-air temperature, derate to 180 mW at 135°C at a rate of 12 mW/°C

recommended operating conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		4.75	5.25	V
V_I	Input voltage		0	V_{CC}	V
V_{IH}	High-level input voltage		2	V_{CC}+0.3	V
V_{IL}	Low-level input voltage (see Note 3)		–0.3	0.8	V
V_O	Output voltage		0	V_{CC}	V
t_r	Rise time	CLK input		20	ns
		Other inputs		50	
t_f	Fall time	CLK input		20	ns
		Other inputs		50	
T_A	Operating free-air temperature		0	70	°C

NOTE 3: The algebraic convention, in which the more negative value is designated minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	TTL	V_{CC} = 4.75 V,	I_{OH} = –4 mA	2.4			V
		CMOS	V_{CC} = 4.75 V,	I_{OH} = –2 mA	3.84			
V_{OL}	Low-level output voltage		V_{CC} = 4.75 V,	I_{OL} = 4 mA			0.45	V
I_I	Input current		V_{CC} = 5.25 V,	$V_I = V_{CC}$ or GND			±10	µA
I_{OZ}	Off-state output current		V_{CC} = 5.25 V,	$V_O = V_{CC}$ or GND			±10	µA
I_{CC}	Supply current	Standby	V_{CC} = 5.25 V,	See Note 4		50	150	µA
		Nonturbo	$V_I = V_{CC}$ or GND,	See Note 5		20	40	mA
		Turbo	No load	See Note 5		150	225	
C_i	Input capacitance		V_I = 0, f = 1 MHz,	T_A = 25°C		20		pF
C_o	Output capacitance		V_O = 0, f = 1 MHz,	T_A = 25°C		20		pF
C_{clk}	Clock capacitance		V_I = 0, f = 1 MHz,	T_A = 25°C		25		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTES: 4. When in the nonturbo mode, the device automatically goes into the standby mode approximately 100 ns after the last transition.
5. These parameters are measured with the device programmed as four 12-bit counters and f = 1 MHz.

external switching characteristics and timing requirements over recommended ranges of supply voltage and operating free air temperature (unless otherwise noted)

turbo-bit on (turbo mode)

PARAMETER†		TEST CONDITIONS	EP1830-20C		EP1830-25C		EP1830-30C		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}	Maximum clock frequency	See Note 6	62.5		50		41.7		MHz
f_{cnt}	Maximum internal frequency	See Note 7	50		40		33.3		MHz
t_{pd1}	Input to nonregistered output delay	C_L = 35 pF		20		25		30	ns
t_{pd2}	I/O input to nonregistered output delay			22		28		34	ns
t_{su}	System clock setup time		13		17		21		ns
t_{hs}	System clock hold time		0		0		0		ns
t_{ch}	System clock high		8		10		12		ns
t_{cl}	System clock low		8		10		12		ns
t_{co1}	System clock to output delay	C_L = 35 pF		15		18		21	ns
t_{asu}	Array clock setup time		8		10		12		ns
t_{ah}	Array clock hold time		8		10		12		ns
t_{aco1}	Array clock to output delay			20		25		30	ns
t_{cnt}	Minimum system clock period			20		25		30	ns

turbo-bit off (non-turbo mode)

PARAMETER†		TEST CONDITIONS	EP1830-20C		EP1830-25C		EP1830-30C		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}	Maximum clock frequency	See Note 6	62.5		50		41.7		MHz
f_{cnt}	Maximum internal frequency	See Note 7	50		40		33.3		MHz
t_{pd1}	Input to nonregistered output delay	C_L = 35 pF		45		50		55	ns
t_{pd2}	I/O input to nonregistered output delay			47		53		59	ns
t_{su}	System clock setup time		38		42		46		ns
t_{hs}	System clock hold time		0		0		0		ns
t_{ch}	System clock high		8		10		12		ns
t_{cl}	System clock low		8		10		12		ns
t_{co1}	System clock to output delay	C_L = 35 pF		15		18		21	ns
t_{asu}	Array clock setup time		33		35		37		ns
t_{ah}	Array clock hold time		8		10		12		ns
t_{aco1}	Array clock to output delay			45		50		55	ns
t_{cnt}	Minimum system clock period			20		25		30	ns

† Letter symbols for switching characteristics and timing requirements in this data sheet have been chosen for compatibility with those used in other documentation previously prepared by another supplier for similar products. Any similarity to symbols used on other TI data sheets or to those shown in glossaries in TI data books is coincidental. The meanings may not be the same.

NOTES: 6. The f_{max} values shown represent the highest frequency of operation without feedback.
7. This parameter is measured with the device programmed as four 12-bit counters.

internal timing requirements over recommended ranges of supply voltage and operating free air temperature (unless otherwise noted)

turbo-bit on (turbo mode)

PARAMETER†		TEST CONDITIONS	EP1830-20C		EP1830-25C		EP1830-30C		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{in}	Input pad and buffer delay			5		7		9	ns
t_{io}	I/O input pad and buffer delay			2		3		4	ns
t_{lad}	Logic array delay			9		12		15	ns
t_{od}	Output pad and buffer delay	C_L = 35 pF		6		6		6	ns
t_{zx}	Output buffer enable time	C_L = 35 pF		6		6		6	ns
t_{xz}	Output buffer disable time	C_L = 5 pF, See Note 8		6		6		6	ns
t_{su}	Register setup time		8		10		12		ns
t_h	Register hold time		8		10		12		ns
t_{ic}	Array clock delay			9		12		15	ns
t_{ics}	System clock delay			4		5		6	ns
t_{fd}	Feedback delay			3		3		3	ns
t_{clr}	Register clear delay			9		12		15	ns

turbo-bit off (non-turbo mode)

PARAMETER†		TEST CONDITIONS	EP1830-20C		EP1830-25C		EP1830-30C		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{in}	Input pad and buffer delay			5		7		9	ns
t_{io}	I/O input pad and buffer delay			2		3		4	ns
t_{lad}	Logic array delay			34		35		40	ns
t_{od}	Output pad and buffer delay	C_L = 35 pF		6		6		6	ns
t_{zx}	Output buffer enable time	C_L = 35 pF		6		6		6	ns
t_{xz}	Output buffer disable time	C_L = 5 pF, See Note 8		6		6		6	ns
t_{su}	Register setup time		8		10		12		ns
t_h	Register hold time		8		10		12		ns
t_{ic}	Array clock delay			34		35		40	ns
t_{ics}	System clock delay			4		5		6	ns
t_{fd}	Feedback delay	See Note 9		–22		–22		–22	ns
t_{clr}	Register clear delay			34		35		40	ns

† Letter symbols for switching characteristics and timing requirements in this data sheet have been chosen for compatibility with those used in other documentation previously prepared by another supplier for similar products. Any similarity to symbols used on other TI data sheets or to those shown in glossaries in TI data books is coincidental. The meanings may not be the same.

NOTES: 8. This is for an output voltage change of 500 mV.

9. The negative number shown for this specification is to compensate for the 30 ns that is being added to the t_{lad} parameter in the turbo-bit off mode. In the non-turbo mode, t_{fd} is not affected by the additional propagation delay because the logic array is already taken out of the non-turbo mode by the first transition into the array. See the section on delay elements.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V_{CC} (see Note 1) ..... −0.3 V to 7 V
Instantaneous supply voltage range, V_{CC} ($t \le 20$ ns) ..... −2 V to 7 V
Programming supply voltage range, V_{PP} ..... −0.3 V to 14 V
Instantaneous programming supply voltage range, V_{PP} ($t \le 20$ ns) ..... −2 V to 14 V
Input voltage range, V_I ..... −0.3 V to 7 V
Instantaneous input voltage range, V_I ($t \le 20$ ns) ..... −2 V to 7 V
V_{CC} or GND current range ..... −300 mA to 300 mA
Continuous total power dissipation at or below 25°C free-air temperature (see Note 2) ..... 1500 mW
Operating free-air temperature, T_A ..... −65°C to 135°C
Storage temperature range ..... −65°C to 150°C

NOTES: 1. All voltage values are with respect to GND terminal.
2. For operation above 25°C free-air temperature, derate to 180 mW at 135°C at a rate of 12 mW/°C

recommended operating conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		4.5	5.5	V
V_I	Input voltage		0	V_{CC}	V
V_{IH}	High-level input voltage		2	V_{CC}+0.3	V
V_{IL}	Low-level input voltage (see Note 3)		−0.3	0.8	V
V_O	Output voltage		0	V_{CC}	V
t_r	Rise time	CLK input		20	ns
		Other inputs		50	
t_f	Fall time	CLK input		20	ns
		Other inputs		50	
T_A	Operating free-air temperature		−40	85	°C

NOTE 3: The algebraic convention, in which the more negative value is designated minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	TTL	V_{CC} = 4.5 V,	I_{OH} = −4 mA	2.4			V
		CMOS	V_{CC} = 4.5 V,	I_{OH} = −2 mA	3.84			
V_{OL}	Low-level output voltage		V_{CC} = 4.5 V,	I_{OL} = 4 mA			0.45	V
I_I	Input current		V_{CC} = 5.5 V,	$V_I = V_{CC}$ or GND			±10	µA
I_{OZ}	Off-state output current		V_{CC} = 5.5 V,	$V_O = V_{CC}$ or GND			±10	µA
I_{CC}	Supply current	Standby	V_{CC} = 5.5 V,	See Note 4		50	150	µA
		Nonturbo	$V_I = V_{CC}$ or GND,	See Note 5		20	40	mA
		Turbo	No load	See Note 5		150	260	
C_i	Input capacitance		V_I = 0, f = 1 MHz,	T_A = 25°C		20		pF
C_o	Output capacitance		V_O = 0, f = 1 MHz,	T_A = 25°C		20		pF
C_{clk}	Clock capacitance		V_I = 0, f = 1 MHz,	T_A = 25°C		25		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTES: 4. When in the nonturbo mode, the device automatically goes into the standby mode approximately 100 ns after the last transition.
5. These parameters are measured with the device programmed as four 12-bit counters and f = 1 MHz.

external switching characteristics and timing requirements over recommended ranges of supply voltage and operating free air temperature (unless otherwise noted)

turbo-bit on (turbo mode)

PARAMETER†		TEST CONDITIONS	EP1830-25I		EP1830-30I		UNIT
			MIN	MAX	MIN	MAX	
f_{max}	Maximum clock frequency	See Note 6	50		41.7		MHz
f_{cnt}	Maximum internal frequency	See Note 7	40		33.3		MHz
t_{pd1}	Input to nonregistered output delay	C_L = 35 pF		25		30	ns
t_{pd2}	I/O input to nonregistered output delay			28		34	ns
t_{su}	System clock setup time		17		21		ns
t_{hs}	System clock hold time		0		0		ns
t_{ch}	System clock high		10		12		ns
t_{cl}	System clock low		10		12		ns
t_{co1}	System clock to output delay	C_L = 35 pF		18		21	ns
t_{asu}	Array clock setup time		10		12		ns
t_{ah}	Array clock hold time		10		12		ns
t_{aco1}	Array clock to output delay			25		30	ns
t_{cnt}	Minimum system clock period			25		30	ns

turbo-bit off (non-turbo mode)

PARAMETER†		TEST CONDITIONS	EP1830-25I		EP1830-30I		UNIT
			MIN	MAX	MIN	MAX	
f_{max}	Maximum clock frequency	See Note 6	50		41.7		MHz
f_{cnt}	Maximum internal frequency	See Note 7	40		33.3		MHz
t_{pd1}	Input to nonregistered output delay	C_L = 35 pF		60		55	ns
t_{pd2}	I/O input to nonregistered output delay			53		59	ns
t_{su}	System clock setup time		42		46		ns
t_{hs}	System clock hold time		0		0		ns
t_{ch}	System clock high		10		12		ns
t_{cl}	System clock low		10		12		ns
t_{co1}	System clock to output delay	C_L = 35 pF		18		21	ns
t_{asu}	Array clock setup time		35		37		ns
t_{ah}	Array clock hold time		10		12		ns
t_{aco1}	Array clock to output delay			50		55	ns
t_{cnt}	Minimum system clock period			25		30	ns

† Letter symbols for switching characteristics and timing requirements in this data sheet have been chosen for compatibility with those used in other documentation previously prepared by another supplier for similar products. Any similarity to symbols used on other TI data sheets or to those shown in glossaries in TI data books is coincidental. The meanings may not be the same.

NOTES: 6. The f_{max} values shown represent the highest frequency of operation without feedback.
7. This parameter is measured with the device programmed as four 12-bit counters.

internal timing requirements over recommended ranges of supply voltage and operating free air temperature (unless otherwise noted)

turbo-bit on (turbo mode)

PARAMETER†		TEST CONDITIONS	EP1830-25I		EP1830-30I		UNIT
			MIN	MAX	MIN	MAX	
t_{in}	Input pad and buffer delay			7		9	ns
t_{io}	I/O input pad and buffer delay			3		4	ns
t_{lad}	Logic array delay			12		15	ns
t_{od}	Output pad and buffer delay	C_L = 35 pF		6		6	ns
t_{zx}	Output buffer enable time	C_L = 35 pF		6		6	ns
t_{xz}	Output buffer disable time	C_L = 5 pF, See Note 8		6		6	ns
t_{su}	Register setup time		10		12		ns
t_h	Register hold time		10		12		ns
t_{ic}	Array clock delay			12		15	ns
t_{ics}	System clock delay			5		6	ns
t_{fd}	Feedback delay			3		3	ns
t_{clr}	Register clear delay			12		15	ns

turbo-bit off (non-turbo mode)

PARAMETER†		TEST CONDITIONS	EP1830-25I		EP1830-30I		UNIT
			MIN	MAX	MIN	MAX	
t_{in}	Input pad and buffer delay			7		9	ns
t_{io}	I/O input pad and buffer delay			3		4	ns
t_{lad}	Logic array delay			37		40	ns
t_{od}	Output pad and buffer delay	C_L = 35 pF		6		6	ns
t_{zx}	Output buffer enable time	C_L = 35 pF		6		6	ns
t_{xz}	Output buffer disable time	C_L = 5 pF, See Note 8		6		6	ns
t_{su}	Register setup time		10		12		ns
t_h	Register hold time		10		12		ns
t_{ic}	Array clock delay			37		40	ns
t_{ics}	System clock delay			5		6	ns
t_{fd}	Feedback delay	See Note 9		–22		–22	ns
t_{clr}	Register clear delay			37		40	ns

† Letter symbols for switching characteristics and timing requirements in this data sheet have been chosen for compatibility with those used in other documentation previously prepared by another supplier for similar products. Any similarity to symbols used on other TI data sheets or to those shown in glossaries in TI data books is coincidental. The meanings may not be the same.

NOTES: 8. This is for an output voltage change of 500 mV.

9. The negative number shown for this specification is to compensate for the 30 ns that is being added to the t_{lad} parameter in the turbo-bit off mode. In the non-turbo mode, t_{fd} is not affected by the additional propagation delay because the logic array is already taken out of the non-turbo mode by the first transition into the array. See the section on delay elements.

design security

The EP1830 contains a programmable design security feature that controls the access to the data programmed into the device. If this programmable feature is used, a proprietary design implemented in the device cannot be copied or retrieved. This enables a high level of design control to be obtained since programmed data within the EPROM cells is invisible.

turbo bit

The EP1830 contains a programmable option to control the automatic power-down feature that enables the low-standby-power mode of the device. This option is controlled by a turbo bit that can be set during programming. When the turbo bit is on, the low-standby-power mode is disabled. The typical I_{CC} versus frequency data for both the turbo-bit-on mode and the turbo-bit-off (low power) mode is shown in Figure 10.

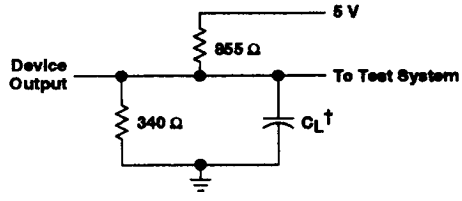
device programming

The EP1830 can be programmed using certified third-party programming equipment. Please contact Texas Instruments applications hotline at (214) 997-5666 for current status of third-party programming support.

functional testing

The EP1830 is functionally tested including complete testing of each programmable EPROM bit and all internal logic elements. The erasable nature (in wafer form) of the EP1830 allows test program patterns to be used and then erased.

Figure 5 shows the dynamic load circuit and the conditions under which dynamic measurements are made. Because power supply transients can affect dynamic measurements, simultaneous transitions of multiple outputs should be avoided to ensure accurate measurement. The performance of threshold tests under dynamic conditions should not be attempted. Large-amplitude fast ground-current transients normally occur as the device outputs discharge the load capacitances. These transients flowing through the parasitic inductance between the device ground terminal and the test-system ground can create significant reductions in observable input noise immunity.



† Includes jig capacitance
All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f \leq 3$ ns, duty cycle = 50%.
Equivalent loads may be used for testing

Figure 5. Dynamic Load Circuit

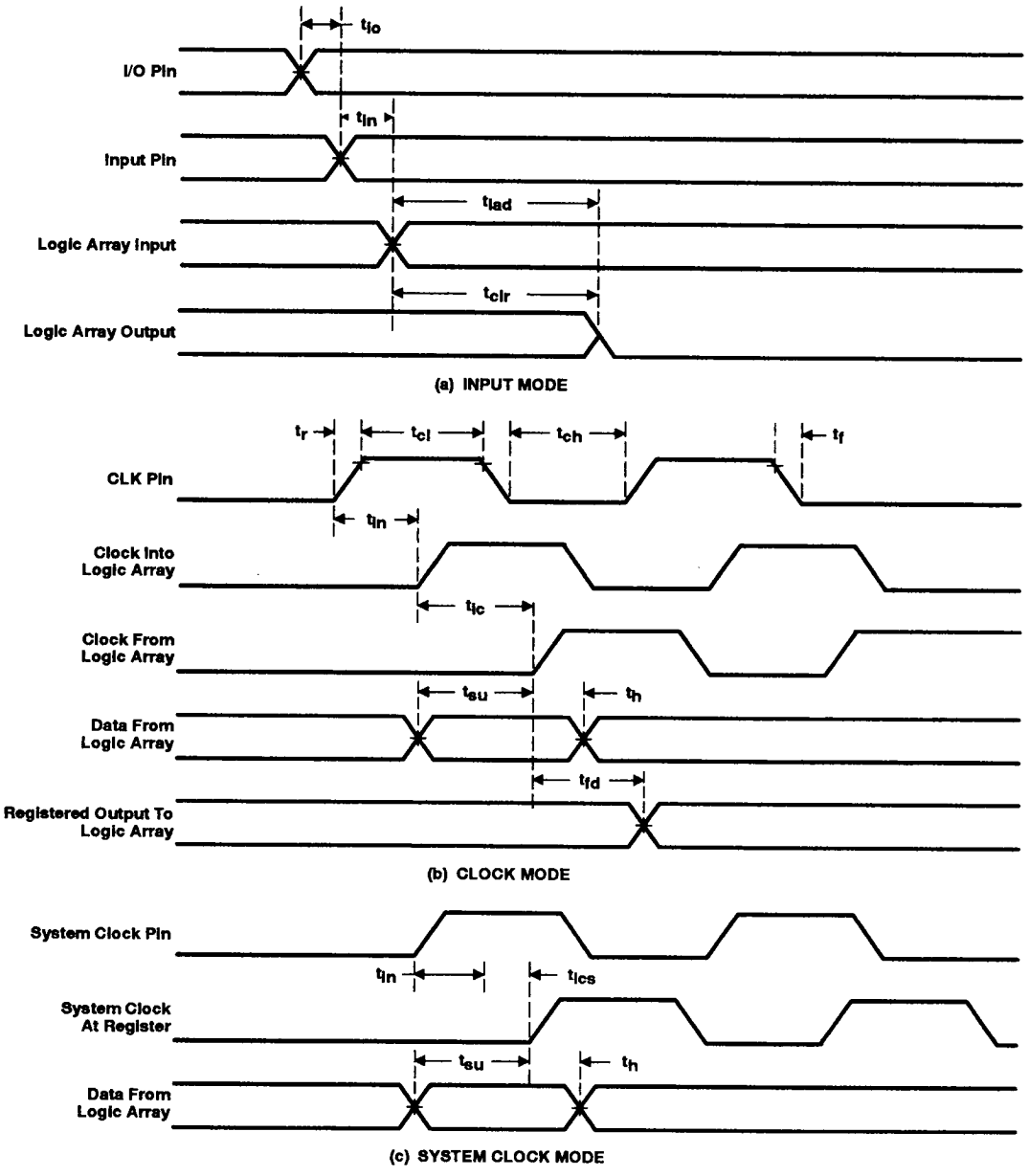


Figure 6. Switching Waveforms

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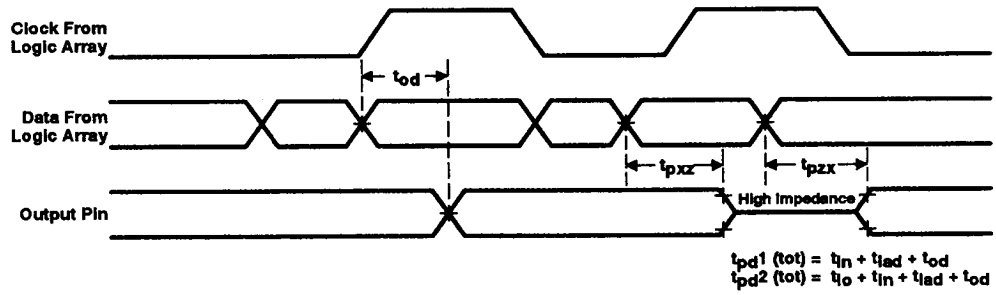


(d) OUTPUT MODE

Figure 6. Switching Waveforms (continued)

understanding EP1830 timing characteristics

introduction

One of the most important benefits of using an EP1830 in any design is the integration of complex logic functions into single-chip solutions. In most cases, however, when the functional compatibility of a design has been determined, timing analysis should be completed to ensure dynamic parameter compatibility.

The purpose of this applications supplement is to discuss the timing delays which exist when using an EP1830. The focus here is on the inherent delay paths that exist in every EP1830 and their relation to the data sheet switching specifications. This should aid designers in modelling and simulating their logic designs.

gate delays versus timing characteristics

Accurate modelling of the timing characteristics requires an understanding of how a given application is implemented within the EP1830. Most designs contain basic gates, and TTL macrofunctions, which are emulated by the general macrocell structure. The macrocell structure is an array of logic in an AND/OR configuration with a programmable inversion followed by an optional flip-flop and feedback, (See Figure 7).

When designing with EP1830s, the term "gate delay" is not a useful measure. Within the EP1830 AND array are product terms. A product term is simply an n input AND gate where n is the number of connections. Depending on the logic implemented, a single product term may represent one to several gate equivalents. Therefore, gate delays do not necessarily provide EP1830 timing characteristics.

summary

To understand timing relationships of the EP1830, it is very important to break up the internal paths into meaningful microparameters that model portions of the architecture. Once internal paths are decomposed, it is then possible to obtain accurate timing information by summing the appropriate combinations of these microparameters. The EP1830 data sheet provides architectural information on which the parameters apply. Knowledge of the architecture allows characterization of any timing path within the EP1830.

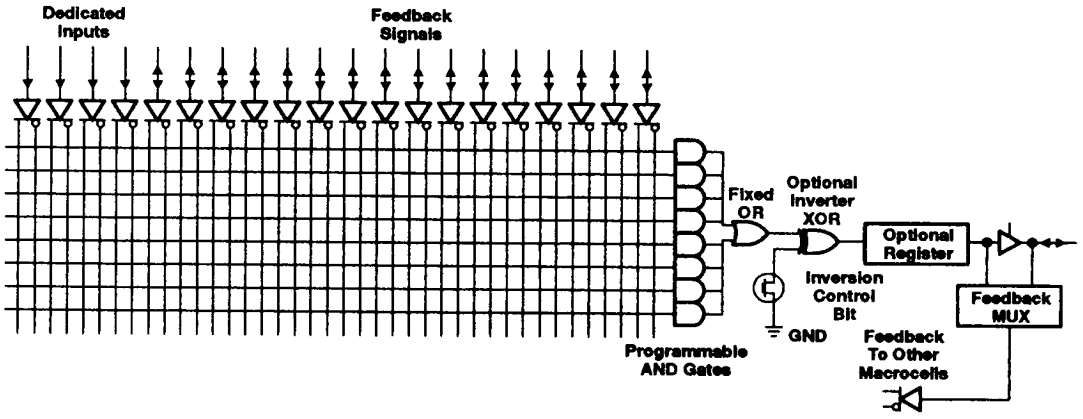
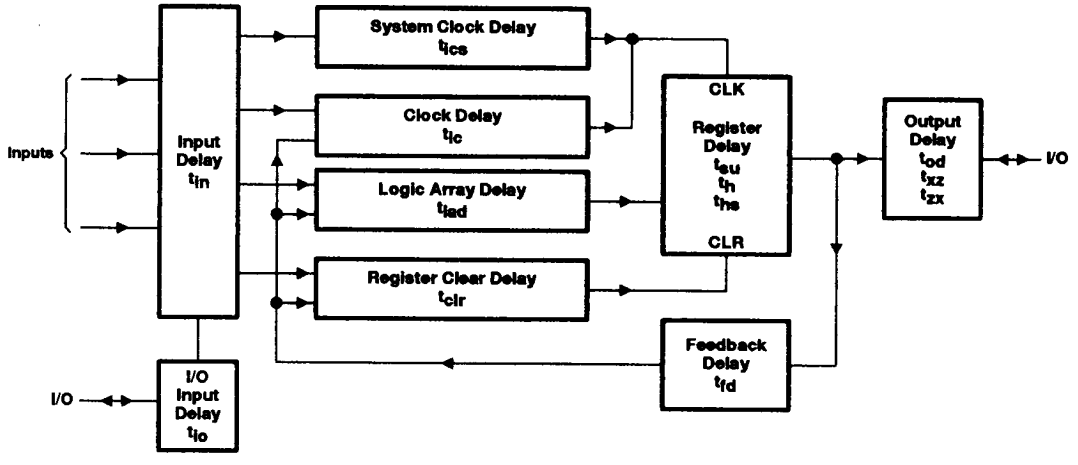


Figure 7. Macrocell

If the design requires low-power operation, the turbo bit should be off (disabled). When operating in this mode, some dynamic parameters are subject to increase.



For combinational outputs, the delay between the logic array and the output buffer is zero. (i. e., $t_{SU} = 0$ or $t_h = 0$)

Figure 8. Macrocell Delay Paths Model

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delay elements

The simplest solution to the architectural requirements is to model time through the logic array as a constant. This parameter is called t_{lad}. The rest of the elements in the timing model are similar to those found in conventional logic. There are input and output delay parameters (t_{in}, t_{io}, t_{od}); register parameters t_{su}, t_h, t_{clr}, t_{hs}, t_{ics}, t_{ic}); and internal connection parameters (t_{fd}). A detailed diagram of an Macrocell Delay Paths Model is shown in Figure 8 with a description of the signals.

glossary – internal delay elements

t_{clr} – Asynchronous register clear time. This is the amount of time it takes for a low signal to appear at the output of a register after the transition of the logic array, including the time required to go through the logic array.

t_{fd} – Feedback delay. In registered applications, this is the delay from the output of the register to the input of the logic array. In combinational applications, it is the delay from the combinational feedback to the input of the logic array.

t_h – Register hold time. This is the internal hold time of the register inside a macrocell – measured from the register clock to the register data input.

t_{lad} – Logic array delay. This parameter incorporates all delay from an input or feedback through the AND/OR structure.

t_{ic} – Clock delay. This delay incorporates all the delay incurred between the output of an input pad or I/O pad and the clock input of a register including the time required to go through the logic array.

t_{ics} – System clock delay. This delay incorporates all delays incurred between the output of the input pad and the clock input of the registers for dedicated clock pins.

t_{in} – Input delay. This is the delay from input pads through the buffers that direct the true and complement data input signals into the AND array.

t_{io} – I/O input pad delay. This delay applies to I/O pins committed as inputs.

t_{od} – Output buffer and pad delay. For registered applications, this incorporates the clock to output delay of the flip-flop. In combinational applications, it incorporates delay from the output of the array to the output of the device.

t_{su} – Register setup time. This is the internal setup time of the register inside a macrocell – measured from the register data input until the register clock.

t_{xz} – Time to high-impedance-state output delay. This delay incorporates the time between a high-to-low transition on the enable input of the 3-state buffer to assertion of a high impedance value at an output pin.

t_{zx} – 3-state to active output delay. This delay incorporates the time between a low-to-high transition on the enable input of the 3-state buffer to assertion of a high or low logic level at an output pin.

glossary – external delay elements

$t_{aco1(tot)}$ – Asynchronous clock to output delay. This is the time required to obtain a valid output after a clock is asserted on an input pin. This delay is the sum of the input delay (t_{in}), the clock delay (t_{ic}), and the output delay (t_{od}).

$t_{acnt(tot)}$ – Asynchronous clocked counter period. This is the minimum period a counter can maintain when asynchronously clocked. This delay is the sum of the feedback delay (t_{fd}), the logic array delay (t_{lad}), and the register setup time (tsu).

$t_{ah(tot)}$ – Asynchronous hold time. This is the amount of time required for data to be present after an asynchronous clock. This value is the difference between the sum of the input delay (t_{in}), the clock delay (t_{ic}), and the hold time (t_h) and the sum of the input delay (t_{in}) and logic array delay (t_{lad}).

$t_{asu(tot)}$ – Asynchronous setup time. This is the time required for data to be present at the input to the register before an asynchronous clock. This value is the difference between the sum of the input delay (t_{in}), array delay (t_{lad}), the register setup time (t_{su}), the sum of the input delay (t_{in}), and the clock delay (t_{ic}).

$t_{co1(tot)}$ – System clock to output delay. This is the time required to obtain a valid output after the system clock is asserted on an input pin. This delay is the sum of the input delay (t_{in}), the system clock delay (t_{ics}), and the output delay (t_{od}).

$t_{clr(tot)}$ – Delay required to clear register. This is the time required to change the output from high to low through a register clear measured from an input transition. This delay is the sum of input delay (t_{in}), register clear delay (t_{clr}), and the output delay (t_{od}).

$t_{cnt(tot)}$ – System clock counter period. This is the minimum period a counter can maintain. This delay is the sum of the feedback delay (t_{fd}), the logic array delay (t_{lad}), and the internal register setup time (t_{su}).

$t_{h(tot)}$ – Hold time for the register. This is the amount of time the data must be valid after the system clock. It is the difference between the sum of the internal input delay (t_{in}), the system clock (t_{ics}), and the system clock hold time (t_{hs}) and the sum of the input delay (t_{in}) and logic array delay (t_{lad}).

$t_{pd1(tot)}$ – Propagation Delay period; This is the delay from a dedicated input to a nonregistered output. This is the time required for data to propagate through the logic array and appear at the external output pin. This delay is the sum of input delay (t_{in}), array delay (t_{lad}), and output delay (t_{od}).

$t_{pd2(tot)}$ – Propagation Delay period; This is the delay from I/O pin to a non-registered output. This is the time required for data from any external I/O input to propagate through any combinational logic and appear at the external output pin. This delay is the sum of the I/O delay (t_{io}), input delay (t_{in}), array delay (t_{lad}), and the output delay (tod).

$t_{PXZ(tot)}$ – Time to enter into the high-impedance state. This is the time required to change an external output from a valid high or low logic level to the high-impedance state from an input transition. This delay is the sum of input delay (t_{in}), array delay (t_{lad}), and the time to disable the 3-state buffer (t_{xz}).

$t_{PZX(tot)}$ – Delay from high impedance to active output. This is the time required to change an external output from the high-impedance state to a valid high or low logic level measured from an input transition. This delay is the sum of input delay (t_{in}), array delay (t_{lad}), and the time to enable the 3-state buffer (t_{ZX}).

$t_{su(tot)}$ – Set up time for the register. This is the time required for data to be present at the register before the system clock. This value is the difference between the sum of input delay (t_{in}), array delay (t_{lad}), and an internal register setup time (t_{su}) and the sum of the input delay (t_{in}) and the system clock delay (t_{ics}).

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explaining the data sheet specifications

The data sheet references timing parameters that characterize the switching operating specifications. These parameters are measured values, derived from extensive device characterization and 100% device testing. Among the switching characteristics are the following: $t_{aco(tot)}$, $t_{acnt(tot)}$, $t_{ah(tot)}$, $t_{asu(tot)}$, $t_{co1(tot)}$, $t_{clr(tot)}$, $t_{cnt(tot)}$, $t_{h(tot)}$, $t_{pd1(tot)}$, $t_{pd2(tot)}$, $t_{PXZ(tot)}$, $t_{PZX(tot)}$, $t_{su(tot)}$. These parameters, described below in detail, may be represented by the internal delay elements. (See Figure 9)

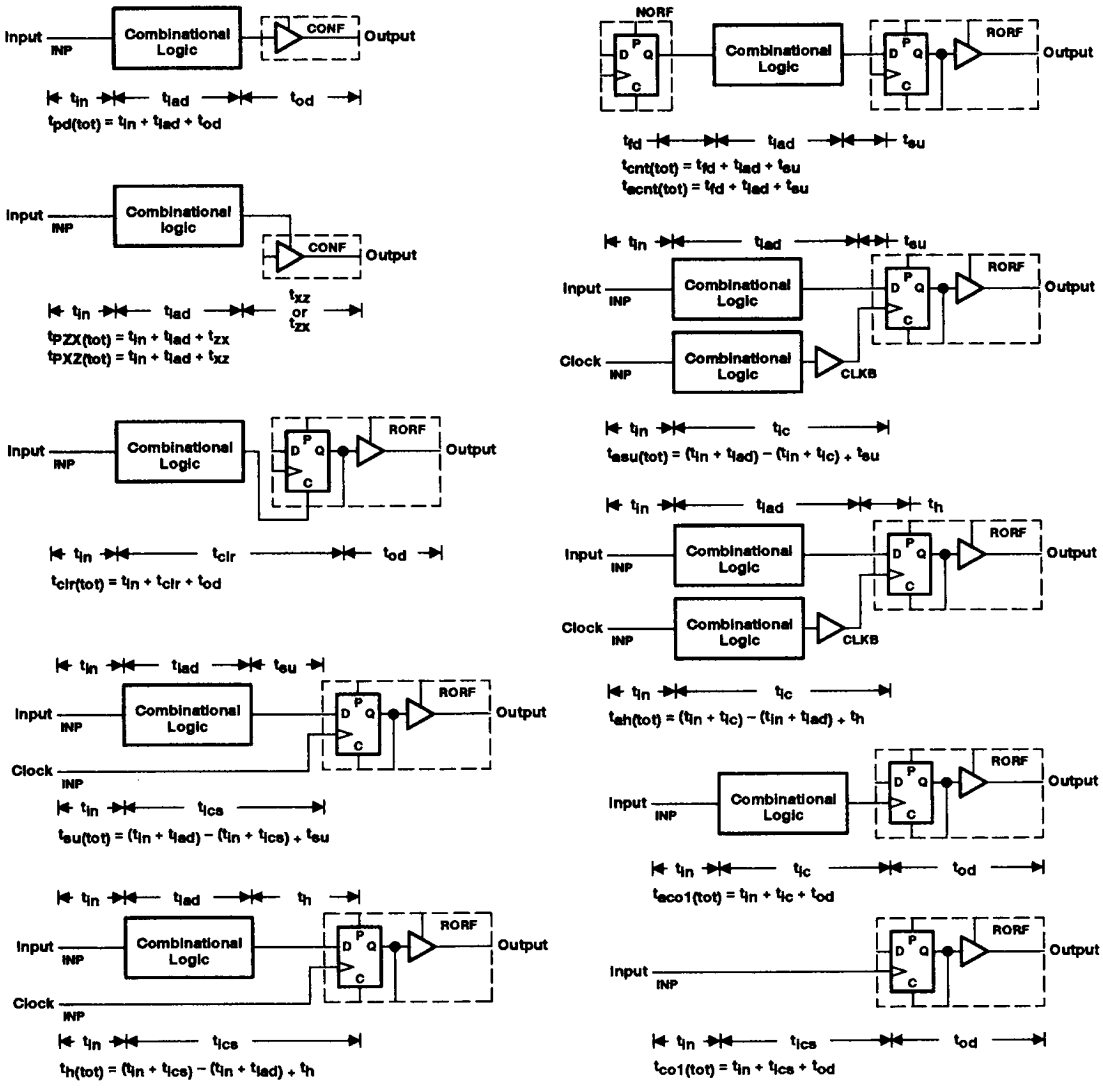

Figure 9. Timing Equations

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
MAXIMUM FREQUENCY

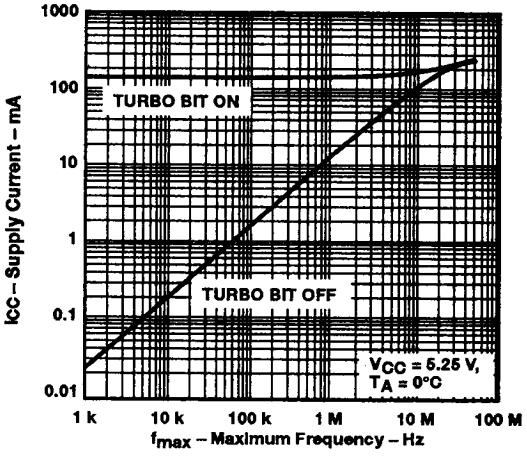

Figure 10

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

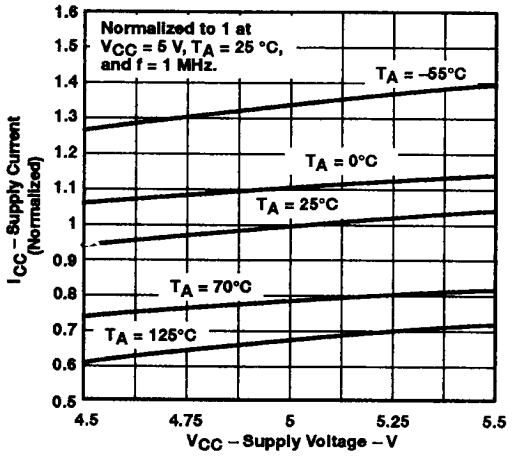

Figure 11

PROPAGATION DELAY TIME
vs
SUPPLY VOLTAGE

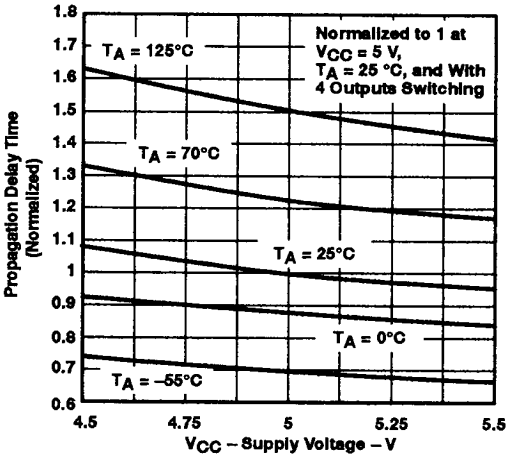

Figure 12

PROPAGATION DELAY TIME
vs
NUMBER OF OUTPUTS SWITCHING

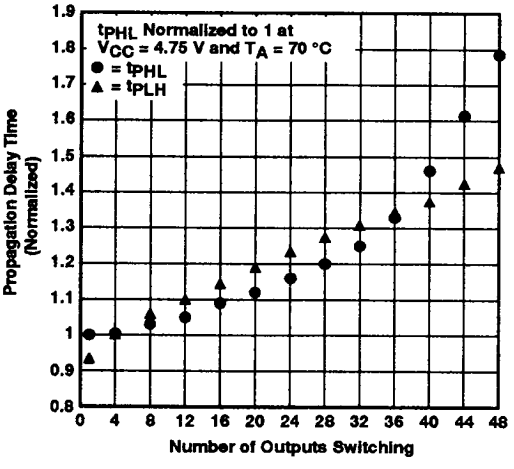

Figure 13

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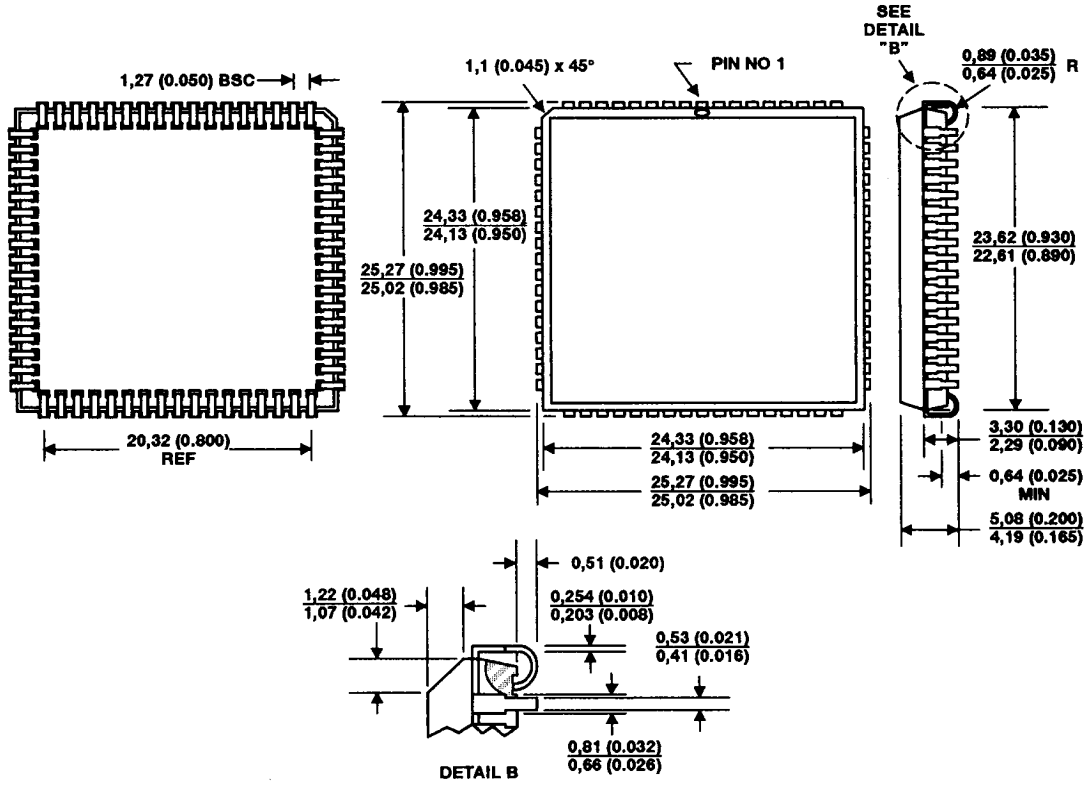
MECHANICAL DATA



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.