HITACHI SEMICONDUCTOR TECHNICAL UPDATE

DATE	8th June, 1999	No.	TN-PSC-340A/E
THEME	The Usage Note of Overrun Status of HD64572 SCA-II.		
CLASSIFICATION	☐ Spec. ☐ Supplement of	■ Limitation on ☐ Correction	
PRODUCT NAME	HD64572FL33 , HD64572AFL33	Lot No.etc.	All lots
REFERENCE DOCUMENTS	HD64572 SCA-II User's Manual (ADE-602-127 and127A)	Effective Date	forever
		From	Now

There are some insufficiency on the Overrun Status Operation of HD64572 SCA-II.
Please take notice on this HITACHI SEMICONDUCTOR TECHNICAL UPDATE.

1. Malfunction of the Overrun Status

When an overrun occurres at the receive FIFO of the SCA-II, and the data read is processed by the MPU or the DMAC simultaneously, there may be a case that the overrun status is not indicated in the status registers and the descriptor status area.

Related status bits are;

OVRNC0 bit of the CST0 register
OVRNC1 bit of the CST1 register
OVRNC2 bit of the CST2 register
OVRNC3 bit of the CST3 register
OVRN bit of the ST2 register
OVRNF bit of the FST register
and Overrun bit of the descriptor status

Because the cause of this malfunction is the disappearance of the overrun status in the status FIFO, all of the statuses, which should be indicated continuously in the status registers and the descriptor status area, is not indicated, when the overrun status attached to the overrun data is once disappeared.

2. Appearance rate of this phenomenon

The appearance rate of this phenomenon is in proportion to the serial rate and in inverse proportion to the system clock frequency. The denominator of the appearance rate is the number of the occurrence of the total overrun, not the number of the frame.

If the read operation is not processed simultaneously when the overrun occurres, this phenomenon never occurres.

Table 1. Rate of the disappearance of the overrun status (System clock = 33.3MHz)

Serial rate	Rate of the disappearance
64kbps	1/16666
1Mbps	1/1064
1.5Mbps	1/711
2Mbps	1/532
30Mbps	1/35

In the table above, 1/16666 means that the phenomenon occurres once in the 16666 occurrence of the overrun error.

3. Countermeasures

(1) To have the overrun never occurred.

a) To make the bus band width bigger as possible.
b) To make the DMA over-head smaller as possible.
c) To set a smaller value to the RNR register.

Mentioned above is possible to reduce the appearance rate of the phenomenon, but it is very hard to make the appearance rate as zero. So, please investigate your system performance.

(2) To use the upper layer protocol to back up the detection of the overrun.

a) To use frames having a constant length, so that it can find an overrun when a frame is detected as the frame having different length from the specified.
Or, to have frames having a data length field in its own, so that it can find an overrun when a frame is detected as the frame having different length from the length which is held in the frame.
b) To control the frame sequense number which is held in the frame itself, so that it can detect the overrun frame which has the normal length caused by the following frame which is also overrun at first part.