mosaic
semiconductor, inc.

# 32K x 32 SRAM MODULE

## PUMA 2S1000-55/70/85/10

Issue 4.2 : June 1996

### Description

The PUMA 2S1000 is a 1Mbit high speed static RAM organised as 32K x 32 in a 66 pin PGA package. Access times of 55ns, 70ns, 85ns or 100ns are available. The devices has a user configurable output width as by 8 , 16 or 32 bits and features a low power standby mode with 3.0V battery back-up compatible, completelty static operation and is directly TTL compatible. The package includes on board decoupling capacitors and is suitable for thermal ladder applications.

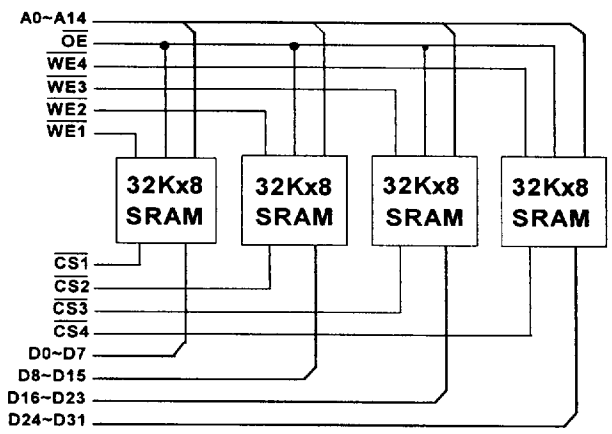
It may be screened in accordance with MIL-STD-883.

1,048,576 bit CMOS Static RAM

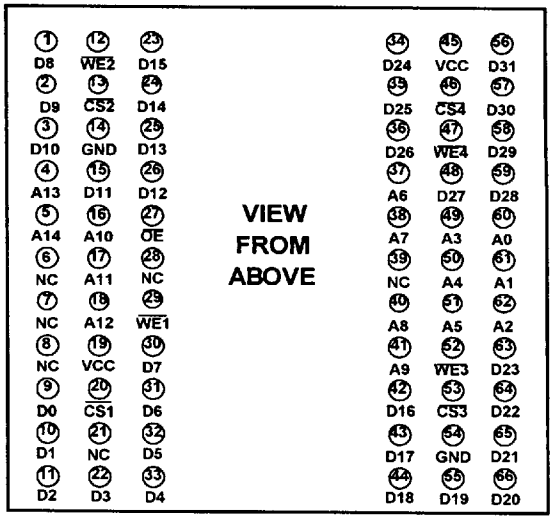
### Features

Very Fast Access times of 55/70/85/10 ns.
Pin grid array gives 2:1 improvement over DIL.
User Configurable as 8 / 16 / 32 bit wide output.
Operating Power 435 / 803 / 1540 mW (Max)
Low Power Standby 4.4mW (Max) -L version.
3.0V Battery Back-up Capability.
On board decoupling capacitors.
Completely Static Operation.
Directly TTL compatible.
May be screened in accordance with MIL-STD-883

### Block Diagram




### Pin Definition




### Pin Functions

| | | | |
|---|---|---|---|
| **A0 -A14** | Address Inputs | **D0-D31** | Data Inputs/Outputs |
| **$\overline{CS1\text{-}4}$** | Chip Select | **$\overline{OE}$** | Output Enable |
| **WE1-4** | Write Enable | **NC** | No Connect |
| **$V_{cc}$** | Power (+5V) | **GND** | Ground |

## DC OPERATING CONDITIONS

### Absolute Maximum Ratings (1)

| | | | |
|---|---|---|---|
| Voltage on any pin relative to $V_{SS}$ (2) | $V_T$ | -0.5V to +7 | V |
| Power Dissipation | $P_T$ | 4 | W |
| Storage Temperature | $T_{STG}$ | -65 to +150 | °C |

Notes : (1) Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

(2) Pulse width:- 3.0V for less than 50ns.

### Recommended Operating Conditions

| *Parameter* | *Symbol* | *min* | *typ* | *max* | |
|---|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 4.5 | 5.0 | 5.5 | V |
| Input High Voltage | $V_{IH}$ | 2.2 | - | $V_{CC}$+0.5 | V |
| Input Low Voltage | $V_{IL}$ | -0.5 | - | 0.8 | V |
| Operating Temperature | $T_A$ | 0 | - | 70 | °C |
| | $T_{AI}$ | -40 | - | 85 | °C (**I** suffixI) |
| | $T_{AM}$ | -55 | - | 125 | °C (**M**, **MB** suffix) |

### DC Electrical Characteristics ($V_{CC}$=5V±10%,$T_A$=-55°C to +125°C)

| *Parameter* | | *Symbol* | *Test Condition* | *min* | *typ*(1) | *max* | *Unit* |
|---|---|---|---|---|---|---|---|
| Input Leakage Current | | $I_{LI1}$ | $V_{IN}$=0V to $V_{CC}$ | - | - | 8 | µA |
| Output Leakage Current | | $I_{LO}$ | $\overline{CS}$(2)=$V_{IH}$ or OE=$V_{IH}$, $V_{I/O}$=0V to $V_{CC}$ | - | - | 8 | µA |
| Operating Supply Current | 32 bit | $I_{CC}$ | $\overline{CS}$(2)=$V_{IL}$, I/P's static, $I_{I/O}$=0mA | - | 32 | 60 | mA |
| Average Supply Current | 32 bit | $I_{CC32}$ | $\overline{CS}$(2)=$V_{IL}$, Min. cycle, $I_{I/O}$=0mA | - | 200 | 280 | mA |
| | 16 bit | $I_{CC16}$ | As above | - | 101 | 146 | mA |
| | 8 bit | $I_{CC8}$ | As above | - | 52 | 79 | mA |
| Standby Supply Current | TTL | $I_{SB}$ | $\overline{CS}$(2)=$V_{IH}$, I/P's Static | - | 2 | 12 | mA |
| | -L version | $I_{SB1}$ | $\overline{CS}$(2)≥$V_{CC}$-0.2V, 0.2V≥$V_{IN}$≥$V_{CC}$-0.2V | - | - | 800 | µA |
| Output Voltage Low | | $V_{OL}$ | $I_{OL}$= 2.1 mA | - | - | 0.4 | V |
| Output Voltage High | | $V_{OH}$ | $I_{OH}$= -1.0 mA | 2.4 | - | - | V |

Notes: (1) Typical values are at $V_{CC}$=5.0V,$T_A$=25°C and specified loading.

(2) $\overline{CS}$ and $\overline{WE}$ above are accessed through CS1-4 and WE1-4 respectively. These inputs must be operated simultaneously for 32 bit mode, in pairs for 16 bit mode and singly for 8 bit mode.

### Capacitance ($V_{CC}$=5V±10%,$T_A$=25°C)

| *Parameter* | *Symbol* | *Test Condition* | *typ* | *max* | *Unit* |
|---|---|---|---|---|---|
| Input Capacitance: | $C_{IN}$ | $V_{IN}$=0V | - | 42 | pF |
| I/O Capacitance: | $C_{I/O}$ | $V_{I/O}$=0V | - | 50 | pF |

Note: This parameter is calculated and not measured.

## Operating Modes

The table below shows the logic inputs required to control the operating modes of each of the SRAMs on the PUMA 2S1000.

| *Mode* | $\overline{CS}$ | $\overline{OE}$ | $\overline{WE}$ | $V_{CC}$ *Current* | *I/O Pin* | *Reference Cycle* |
|---|---|---|---|---|---|---|
| Not Selected | 1 | X | X | $I_{SB}$,$I_{SB1}$ | High Z | Power Down |
| OutputDisable | 0 | 1 | 1 | $I_{CC}$ | High Z | |
| Read | 0 | 0 | 1 | $I_{CC}$ | $D_{OUT}$ | Read Cycle |
| Write | 0 | X | 0 | $I_{CC}$ | $D_{IN}$ | Write Cycle |

$1 = V_{IH}$, $0 = V_{IL}$, X = Don't Care

Note: $\overline{CS}$ is accessed through $\overline{CS1\text{-}4}$, and $\overline{WE}$ is accessed through $\overline{WE1\text{-}4}$. For correct operation, $\overline{CS1\text{-}4}$ must operate simultaneously for 32 bit operation, in pairs for 16 bit operation, or singly for 8 bit operation. $\overline{WE1\text{-}4}$ must also be operated in the same manner.

## Low $V_{cc}$ Data Retention Characteristics - L Version Only ($T_A$=-55°C to +125°C)

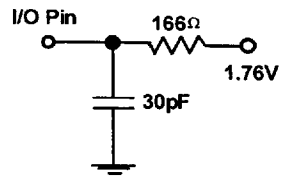
| *Parameter* | *Symbol* | *Test Condition* | *min* | *typ* | *max* | *Unit* |
|---|---|---|---|---|---|---|
| $V_{CC}$ for Data Retention | $V_{DR}$ | $\overline{CS1\sim4} \geq V_{CC}$-0.2V, $V_{IN} \geq 0V$ | 2.0 | - | - | V |
| Data Retention Current | $I_{CCDR1}$ | $V_{CC}$=3.0V, $V_{IN} \geq 0V$, $\overline{CS1\sim4} \geq V_{CC}$-0.2V. | - | - | 680 | µA |
| Chip Deselect to Data Retention Time | $t_{CDR}$ | See Retention Waveform | 0 | - | - | ns |
| Operation Recovery Time | $t_R$ | See Retention Waveform | $t_{RC}$ (1) | - | - | ns |

Notes (1) $t_{RC}$ = Read Cycle Time

## AC Test Conditions

* Input pulse levels: GND to 3.0V
* Input rise and fall times: 5ns
* Input and Output timing reference levels: 1.5V
* $V_{cc}$=5V±10%
* Module is tested in 32bit mode.
* Output load : 1 TTL gate + 100pF

## Output Load Circuit



## AC OPERATING CONDITIONS

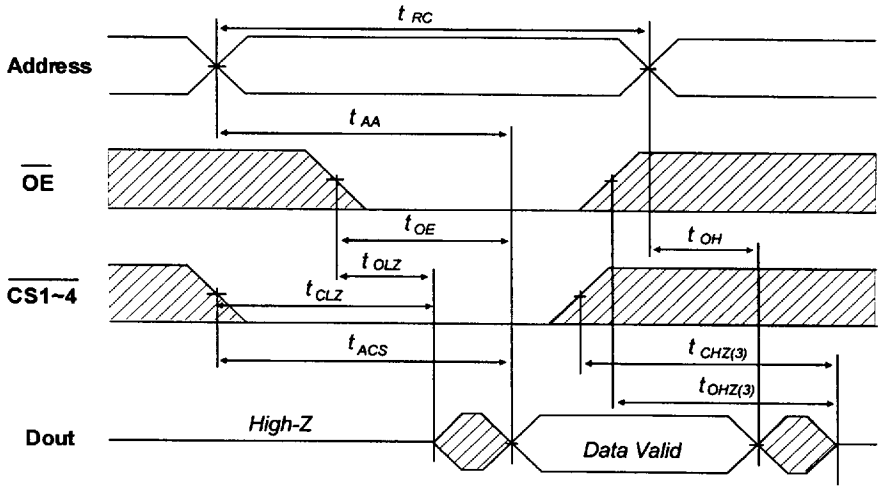
### Read Cycle

| | | 55 | | 70 | | 85 | | 10 | | |
|---|---|---|---|---|---|---|---|---|---|---|
| *Parameter* | *Symbol* | *min* | *max* | *min* | *max* | *min* | *max* | *min* | *max* | *Unit* |
| Read Cycle Time | $t_{RC}$ | 55 | - | 70 | - | 85 | - | 100 | - | ns |
| Address Access Time | $t_{AA}$ | - | 55 | - | 70 | - | 85 | - | 100 | ns |
| Chip Select Access Time | $t_{ACS}$ | - | 55 | - | 70 | - | 85 | - | 100 | ns |
| Output Enable to Output Valid | $t_{OE}$ | | 35 | - | 40 | - | 45 | - | 50 | ns |
| Output Hold from Address Change | $t_{OH}$ | 5 | - | 5 | - | 5 | - | 10 | - | ns |
| Chip Selection to Output in Low Z | $t_{CLZ}$ | 5 | - | 5 | - | 10 | - | 10 | - | ns |
| Output Enable to Output in Low Z | $t_{OLZ}$ | 0 | - | 0 | - | 5 | - | 5 | - | ns |
| Chip Deselection to Output in High Z[3] | $t_{CHZ}$ | - | 25 | - | 25 | 0 | 30 | 0 | 35 | ns |
| Output Disable to Output in High Z[3] | $t_{OHZ}$ | - | 25 | - | 25 | 0 | 30 | 0 | 35 | ns |

### Write Cycle

| | | 55 | | 70 | | 85 | | 10 | | |
|---|---|---|---|---|---|---|---|---|---|---|
| *Parameter* | *Symbol* | *min* | *max* | *min* | *max* | *min* | *max* | *min* | *max* | *Unit* |
| Write Cycle Time | $t_{WC}$ | 55 | - | 70 | - | 85 | - | 100 | - | ns |
| Chip Selection to End of Write | $t_{CW}$ | 50 | - | 65 | - | 75 | - | 80 | - | ns |
| Address Valid to End of Write | $t_{AW}$ | 50 | - | 65 | - | 75 | - | 80 | - | ns |
| Address Setup Time | $t_{AS}$ | 0 | - | 0 | - | 0 | - | 0 | - | ns |
| Write Pulse Width | $t_{WP}$ | 45 | - | 60 | - | 60 | - | 60 | - | ns |
| Write Recovery Time | $t_{WR}$ | 0 | - | 0 | - | 0 | - | 0 | - | ns |
| Write to Output in High Z | $t_{WHZ}$ | 0 | 30 | 0 | 30 | 0 | 30 | 0 | 35 | ns |
| Data to Write Time Overlap | $t_{DW}$ | 35 | - | 40 | - | 40 | - | 40 | - | ns |
| Data Hold from Write Time | $t_{DH}$ | 0 | - | 0 | - | 0 | - | 0 | - | ns |
| Output Disable to Output in High Z | $t_{OHZ}$ | - | 25 | 0 | 25 | 0 | 30 | 0 | 35 | ns |
| Output Active from End of Write | $t_{OW}$ | 5 | - | 5 | - | 5 | - | 5 | - | ns |

## Read Cycle Timing Waveform (1,2)



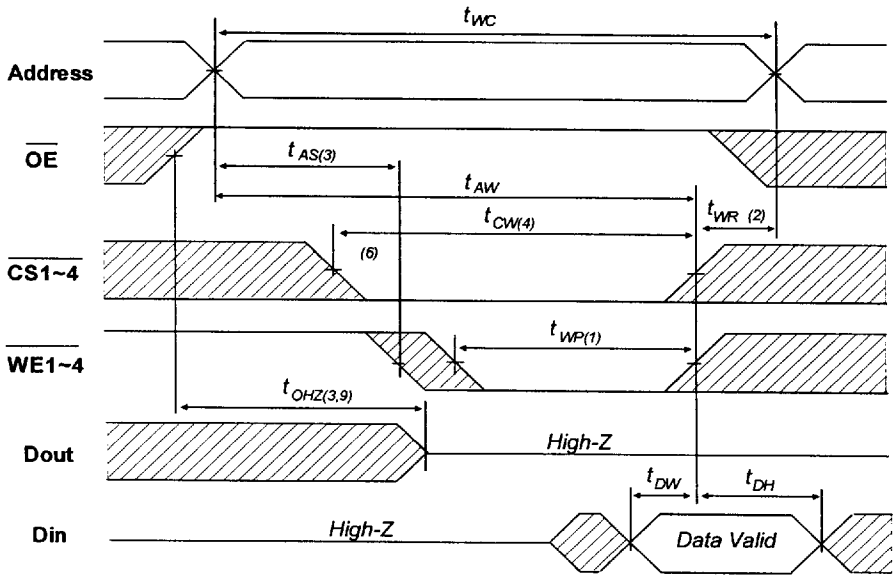

Notes:

(1) During the Read Cycle, $\overline{WE1\sim4}$ is high for the PUMA 2S1000 module.

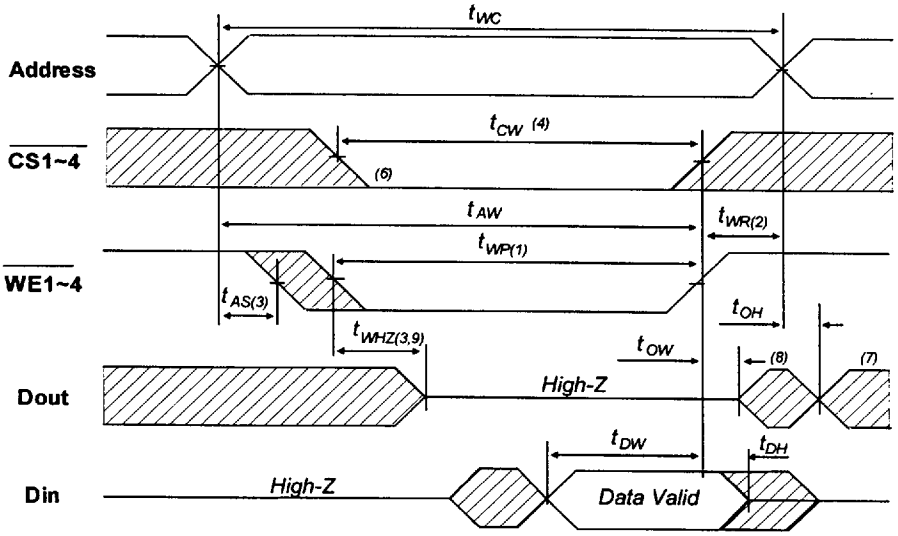
(2) Address valid prior to or coincident with $\overline{CS1\sim4}$ transition Low.

(3) $t_{CHZ}$ and $t_{OHZ}$ are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels. These parameters are sampled and not 100% tested.

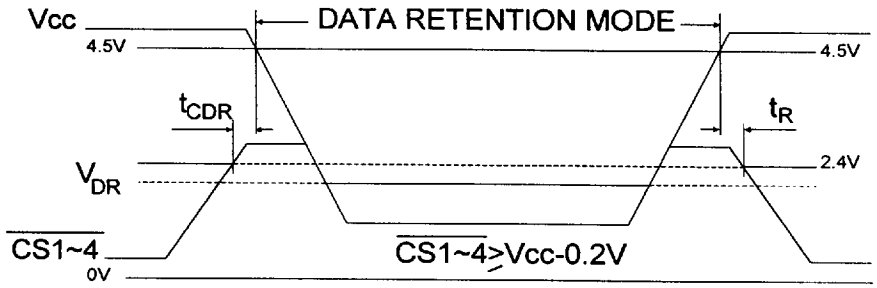
## Write Cycle 1 Timing Waveform



## Write Cycle 2 Timing Waveform [5]




## Low $V_{CC}$ Data Retention Timing Waveform




## AC Characteristics Notes

(1) A write occurs during the overlap ($t_{WP}$) of a low $\overline{CS}$ and a low $\overline{WE}$.

(2) $t_{WR}$ is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.

(3) During this period, I/O pins are in the output state. Input signals out of phase must not be applied.

(4) If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ low transition, outputs remain in a high impedance state.

(5) $\overline{OE}$ is continuously low. ($\overline{OE}$=$V_{IL}$)

(6) $D_{OUT}$ is in the same phase as written data of this write cycle.

(7) $D_{OUT}$ is the read data of next address.

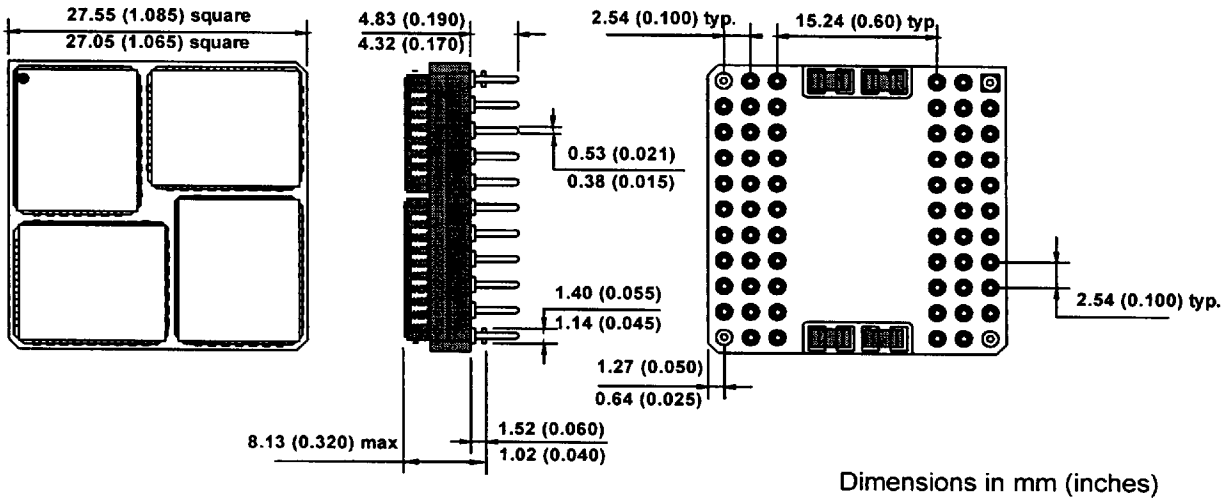
(8) If $\overline{CS}$ is low during this period, I/O pins are in the output state. Input signals out of phase must not be applied.

(9) $t_{WHZ}$ and $t_{OHZ}$ are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels. These parameters are sampled and not 100% tested.

$\overline{CS}$ and $\overline{WE}$ above refers to $\overline{CS1~4}$ and $\overline{WE1~4}$ respectively.

## PACKAGE DETAILS

### 66 Pin PGA




Dimensions in mm (inches)

## SCREENING

### Military Screening Procedure

**Module Screening Flow** for high reliability product is in accordance with Mil-883 method 5004 .

| MB MODULE SCREENING FLOW | | |
|---|---|---|
| ***SCREEN*** | ***TEST METHOD*** | ***LEVEL*** |
| **Visual and Mechanical** | | |
| External visual | 2017 Condition B or manufacturers equivalent | 100% |
| Temperature cycle | 1010 Condition C (10 Cycles, -65°C to +150°C) | 100% |
| **Burn-In** | | |
| Pre-Burn-in electrical | Per applicable Device Specifications at $T_A$=+25°C | 100% |
| Burn-in | $T_A$=+125°C,160hrs minimum. | 100% |
| **Final Electrical Tests** | Per applicable Device Specification | |
| Static (DC) | a) @ $T_A$=+25°C and power supply extremes | 100% |
| | b) @ temperature and power supply extremes | 100% |
| Functional | a) @ $T_A$=+25°C and power supply extremes | 100% |
| | b) @ temperature and power supply extremes | 100% |
| Switching (AC) | a) @ $T_A$=+25°C and power supply extremes | 100% |
| | b) @ temperature and power supply extremes | 100% |
| **Percent Defective allowable (PDA)** | Calculated at Post Burn-in at $T_A$=+25°C | 10% |
| **Quality Conformance** | Per applicable Device Specification | Sample |
| **External Visual** | 2009 Per vendor or customer specification | 100% |

## Ordering Information

**PUMA 2S1000LMB-55**

| | | |
|---|---|---|
| Speed | 55 | = 55 ns |
| | 70 | = 70 ns |
| | 85 | = 85 ns |
| | 10 | = 100 ns |
| Temp. range/screening | Blank | = Commercial Temperature. |
| | I | = Industrial Temperature. |
| | M | = Military Temperature. |
| | MB | = Screened in accordance with MIL-STD-883. |
| Power Consumption | Blank | = Standard Part. |
| | L | = Low Power Part. |
| Memory Organisation | 1000 | = 32K x 32, configurable as 64K x 16 and 128K x 8 |
| Memory Technology | S | = Static RAM. |
| Package | PUMA 2 | = 66 pin Ceramic PGA. |