Flip Chip TVS Evaluation and Assembly Guide

Introduction

The Semtech flip chip TVS is a state-of-the-art component designed to meet the protection needs of today's portable electronic devices. The advantages of flip chip technology include reduced size and weight, improved electrical performance, and low profile. These devices are designed to be compatible with standard surface mount technology (SMT) assembly processes. This document will explain a few assembly and layout guidelines needed to successfully implement Semtech's flip chip TVS components.

Description

There is often confusion as to the classification of devices as flip chip or chip scale packages (CSP). There is no precise definition for either. CSP configurations are often broadly classified by solder bump height or by package sizes. The latter definition is a device with a package size that is 1.2 to 1.5 times the size of the die. Devices that are smaller then 1.2 times the die area are often referred to as flip chip. Additionally, CSP devices are sometimes defined as requiring an interposer (such as a film or laminate layer) between the silicon IC and the PCB for purposes of redistributing the device connections. However, this is not always true. Many CSP devices do not require an interposer layer. Additionally, some literature defines CSP devices as being compatible with current surface mount assembly technologies, while flip chip devices are not. Semtech's devices have a package to die size ratio of 1:1 and do not require an interposer layer. They are also compatible with current high volume assembly technology. Therefore, Semtech's devices could be classified as either flip chip or CSP components.

Package Construction

The flip chip TVS consists of a silicon IC with a proprietary surface passivation and solder balls or bumps on the active side of the device. The solder bump structure is a key component to the long-term reliability and assembly considerations of the device. The solder bump is actually a metallurgical system consisting of a metal pad, under bump metal (UBM), and a solder ball. There are several technologies for applying solder bumps to flip chip components.

Semtech utilizes a proprietary electroless nickel plate process for the UBM paired with screen printed solder balls. The balls are laid out in a grid with a pin out pattern per JEDEC standard outline MO-211.

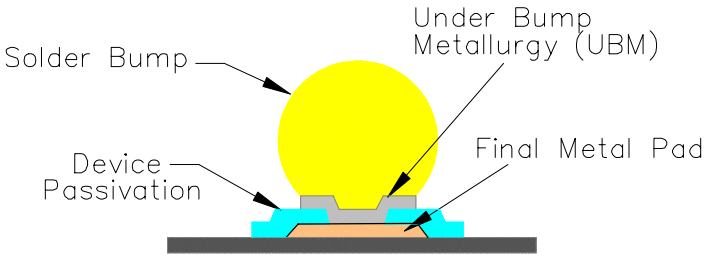


Figure 1 - Anatomy of a Solder Bump

Assembly Processes and Design Optimization

The reliability performance of the solder balls after the device is attached to the board is a strong function of the board design and assembly parameters. Although a flip chip wafer level device is designed to be compatible with standard surface mount technology assembly process, certain precautions and design considerations must be in place to assemble these devices for maximum reliability.

Board Design

The first consideration the designer is faced with is pad size and definition. Figure 2 shows the recommended printed circuit board (PCB) footprint for the 3 x 2 grid array (1 x 1.5 0.7mm) flip chip TVS. The solder pads are circular with a diameter of 0.225 ± 0.010mm. This size was chosen because it is the minimum diameter that can be consistently achieved by most PCB manufacturers. Ideally, the pad size would not deviate more than +/- 0.010mm from the nominal diameter of the solder balls.

Theoretically, SMD (solder mask defined) pads should provide increased thermal cycling reliability over NSMD (non-solder mask defined) pads due to higher stand off of SMD solder balls. However, this is not the case. The mask on SMD will touch solder ball after reflow potentially introducing a stress concentration point near the solder mask/ball interface. This can cause cracks in the solder ball leading to premature solder joint failure during extreme fatigue conditions (such as temperature cycle) for an SMD pad design. By leaving the gap in the solder mask (NSMD), the stress at the

solder mask/ball interface is eliminated.

The traces to the pads should be 0.100 mm or less and 1 oz copper layer thickness. Large traces can lead to excess solder wicking on one side of the component resulting in "tombstoning" (leaning to one side) of the component.

Board Finish

A uniform board finish is critical for good assembly yield. Two finishes that provide uniform surface coatings are immersion nickel gold and organic surface protectant (OSP). A non-uniform finish such as hot air solder leveling (HASL) can lead to mounting problems and should be avoided. If a gold finish is used, the thickness of the immersion gold should be kept to less than 0.5 micron in order to avoid solder joint embrittlement.

Board Assembly

Initially, OSP finished boards were used and were assembled without solder paste. A water soluble, tacky flux was used to mount the devices to the board. Other assembly variations that Semtech has evaluated are OSP finish with solder paste, immersion gold with solder paste, immersion gold with flux, and fused tin/lead with solder paste. In cases where solder paste is used, a paste with a Sn62/Pb36/Ag2 or Sn62.8/Pb36.8/Ag0.4 composition and type 4 or finer powder is recommended. The small amount of silver impregnation is recommended for slowing the eutectic transition point and thus reducing the possibility of tombstoning. Some experimentation may be required

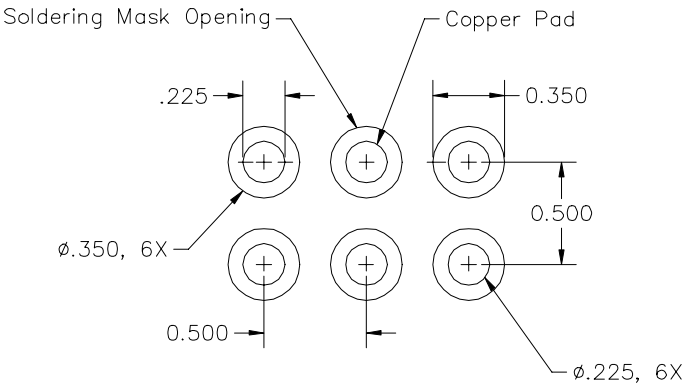


Figure 2 - NSMD Package Footprint

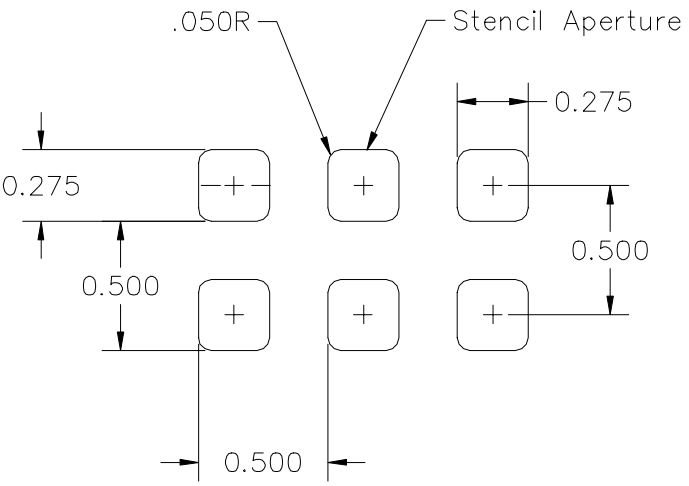


Figure 3 - Stencil Design

Table 1 - Summary of assembly information for SFC05-4 CSP TVS	
Copper Pad Dimension	0.200mm, round
Copper pad Definition	Non solder mask defined (NSMD)
Copper Pad Pitch	0.500mm
Solder Mask Opening	0.3500mm
Soldering Stencil Thickness	0.100mm
Soldering Stencil Aperture Opening	0.275mm Square with rounded corners
Soldering Stencil Fabrication Method	Laser cut, electro-polished
Solder Paste Specification	Type 4, Sn62/Pb36/Ag2 or Sn62.8/Pb36.8/Ag0.4
Flux Specification	No Clean or tacky, water-soluble

to optimize the process.

A properly designed stencil is key to achieving adequate solder volume without compromising assembly yields. A laser cut, electro-polished stencil with 0.275mm square apertures and rounded corners was used for paste application. The electro-polished stencil ensures tapering aperture walls that facilitate uniform deposition. The thickness of the stencil also affects solder volume. A 0.100 mm thick stencil yields good results.

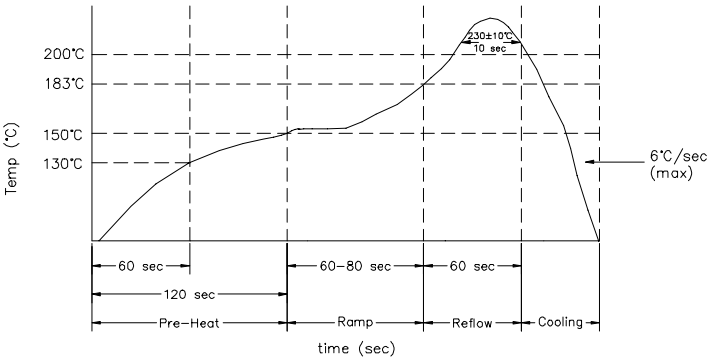
Automatic pick and place equipment with optical component centering is used to place the devices on the board. The placement height should be programmed to adjust for the height of the device. The mechanical pick-up and placement force must be minimized to avoid any damage to the solder balls. Insufficient force however will prevent the solder balls from making contact with the pads. The placement force used to assemble the Semtech evaluation boards was 12 pounds/square inch. The devices are picked from tape and reel. Assembly parameters are listed in Table 1.

Reflow Profile

The flip chip TVS can be assembled using standard SMT reflow processes. Semtech's evaluation boards were reflowed in an IR convection oven. As with any component, thermal profiles at specific board locations can vary and must be determined by the manufacturer. The flip chip TVS peak reflow temperature is 230 ± 10°C. Time above eutectic temperature (183 °C) should be 50 ± 10 seconds. During reflow, the component will self-align itself on the pad. The solder bumps will uniformly collapse and form a cohesive shiny solder joint.

Underfill

Underfill epoxy is designed to enhance thermal performance and give greater mechanical protection to flip chip, CSP and BGA components. The need to underfill can depend upon several factors including the physical size of the device. Semtech has achieved reliable results without the use of underfill material. The reliability data reported below is for boards built with no underfill material.



Typical solder reflow profile for OSP finish FR–4 bond.

Pre–heat to 150°C	120 sec max
Time to eutectic (183°C)	60–80 sec
Time above eutectic	50±10 sec
Peak reflow temp	230±10°C
Time w/in 10°C of peak	10 seconds
Ramp down rate	6°C/sec max

Figure 3 - Reflow Profile

Temperature Cycle

Temperature cycling is one of the most critical tests for this type of device. It is designed to test the mechanical integrity of the solder bump to package and solder bump to board interfaces. The devices were temperature cycled from –40 to +125°C. This temperature range is more severe than the generally used temperature range of 0 to +100°C for commercial devices. It was chosen to model the worst case conditions and operating environments. Temperature cycle testing results are available upon request. In all cases, the devices passed >1000 cycles before the first failure occurred.

High Temperature Operating Life (HTOL)

High temperature operating life is designed to accelerate failures due to process contamination as well as the effects of electromigration on the solder bump/UBM interface. The test involves simulating the worst case operating environment by biasing the devices at the working voltage at an elevated temperature of 125°C for 1,000 hours. All lots tested to date have passed with zero failures after 1000 hours of testing.