# SRT-141A/1045
# ENCODER/DECODER

**SPACE RESEARCH TECHNOLOGY, INC**                    **DATA SHEET**

## FEATURES

- A complete implementation of the FEC sub-layer functions specified in MIL-STD-188-141A and FED-STD-1045.

- TX and RX data I/O buffering.

- Easy to use: flexible microprocessor interface.

- Selectable serial or Tri-bit modem I/F.

- High speed processing increases design flexibility and options.

- Golay encoder/decoder based on SRT's proven design.

- Bypass control of the Golay, interleaving and majority vote FEC modes.

- Maintenance of up to three simultaneous calls.

- Single chip solution fabricated in CMOS technology.

- Single 6MHz clock input.

- Single +5V, +/-10% power supply.

- Commercial, industrial, MIL temperature and MIL-STD-883(C) Class B versions available.
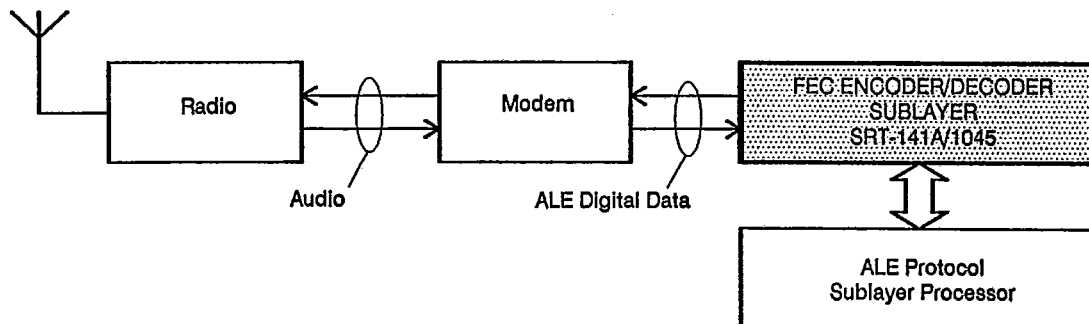
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**Figure 1. SRT-141A/1045 Typical Implementation**

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# FUNCTIONAL DESCRIPTION

## Product Overview

The SRT-141A/1045 is a complete implementation of Data Link forward error correction (FEC) sublayer of the Automatic Link Establishment (ALE) Protocol specified in MIL-STD-188-141A and FED-STD-1045.

MIL-STD-188-141A, "Interoperability and Performance Standards for Medium And High Frequency Radio Equipment", and FED-STD-1045, "Automatic Link Establishment Protocol", are new mandatory military and federal interoperability standards, respectively, applicable to new MF and HF radio equipment and those MF and HF radios undergoing major modifications.

The requirements implemented by the SRT-141A/1045 are contained in the following paragraphs of the two standards:

| MIL-STD-188-141A | FED-STD-1045 |
|---|---|
| Coding: 60.3 | Coding: 5.2.3 |
| Framing: 60.4.2 | Framing: 5.2.4.2 |
| Synchronization: 60.4.3 | Synchronization: 5.2.4.3 |

In terms of the International Standards Organization (ISO) Open System Interconnect (OSI) seven-layer reference model (International Standard 7498), the ALE protocol occupies the data link layer. As shown in Figure 2, the ALE protocol is divided into two sub-layers within the data link layer.

The lower sublayer contains the ALE protocol FEC function (implemented by the SRT-141A/1045) and the upper sublayer contains the ALE protocol Link Establishment, Data Communication and Link Quality Analysis functions.

The SRT-141A/1045 will enable designers of equipment implementing the new ALE protocol to:

● Minimize cost

● Decrease design time

● Improve design reliability and flexibility

All the FEC sublayer functions are implemented by the SRT-141A/1045 and include:

● Golay Encoding and Decoding,

● Interleaving and De-Interleaving,

● Redundancy Encoding and Majority Vote Decoding,
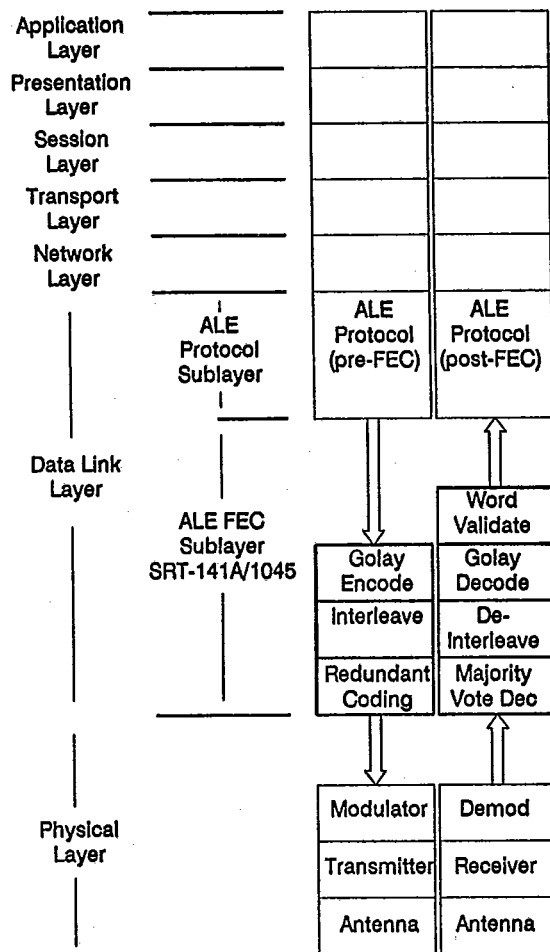


**Figure 2. ALE Protocol**

● Preamble, character and word phase validation checks against preset word acceptance criteria thresholds, and

● Majority vote decoder unanimous vote count, word phase and Golay decoder error correction count measurements and reporting.

The SRT-141A/1045 has two major modes of operation: TRANSMIT MODE and the RECEIVE MODE. Both TRANSMIT and RECEIVE modes can operate simultaneously and asynchronously. A functional block diagram of the SRT-141A/1045 is shown in Figure 3.

**RECEIVER**

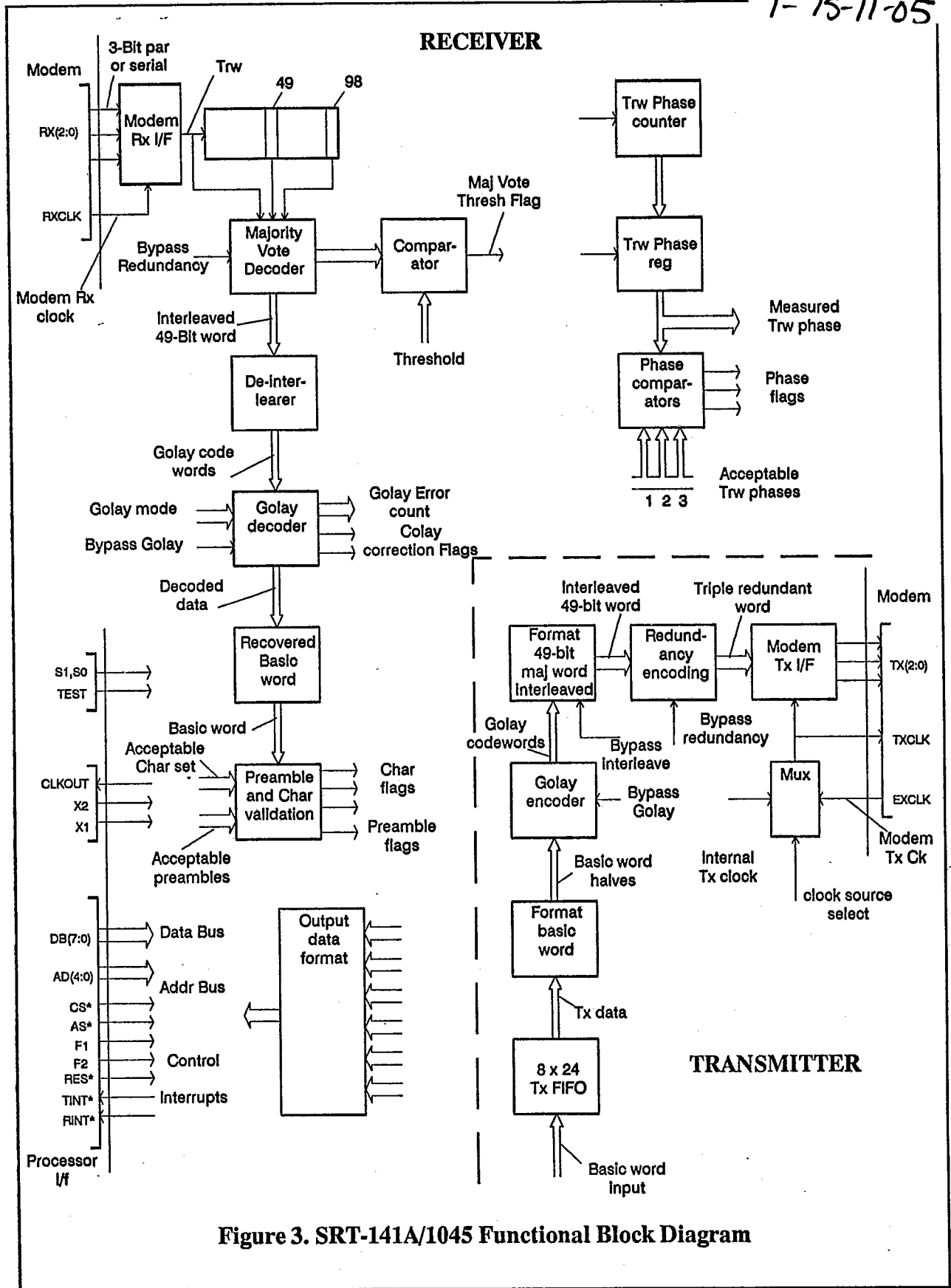Figure 3. SRT-141A/1045 Functional Block Diagram

**TRANSMITTER**

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## Processor Interface

The SRT-141A/1045 interfaces to the system processor over an eight-bit bi-directional data bus and associated control timing. Transfer of all data, control, status and flag information between the SRT-141A/1045 internal registers and the system processor is accomplished over this bus. Table 1 lists all the accessible internal registers and their I/O bus assignments.

The processor interface is programmable to one of four processor interface types. Programming pins S0 and S1 select the interface type most suitable for the particular processor used. Refer to "Switching and Timing Characteristics" for I/O timing in different processor interface configurations.

Flexibility in scheduling processor I/O to the SRT141A/1045, is made possible by the built-in 8 basic word deep transmit First-In-First-Out (FIFO) buffer. This flexability expands the application potential of the SRT141A/1045 while decreasing processor I/O overhead. For example, several separate channels, each channel using a single SRT-141A/1045, can be easily controlled by a single processor. Controlling several channels can be utilized in the design of gateways, relay nodes and other multiple channel handling devices.

## Modem Interface

As may be seen from Figure 3, the SRT141A/1045 directly interfaces to the system modem. The data interface to/from the modem is set by the Format Control Register to be either a parallel 3-bit byte (a tri-bit) interface or a serial interface. Each tri-bit represents the 3-bits associated with each transmited or received tone. The serial interface requires that the tri-bits associated with each tone be serialized before sending them or receiving them to or from the modem respectively.

When receiving data from the modem the modem must supply a 375Hz clock synchronized to either the serial data or tri-bit data (three clocks pre tri-bit value). The transmit section can utilize either an internally generated 375Hz clock or an externally supplied clock. The transmit clock is available as an output and can be used by the external modem as desired.

## Transmit Operation

In TRANSMIT MODE the SRT141A/1045 receives from the system processor the 24-bit ALE words

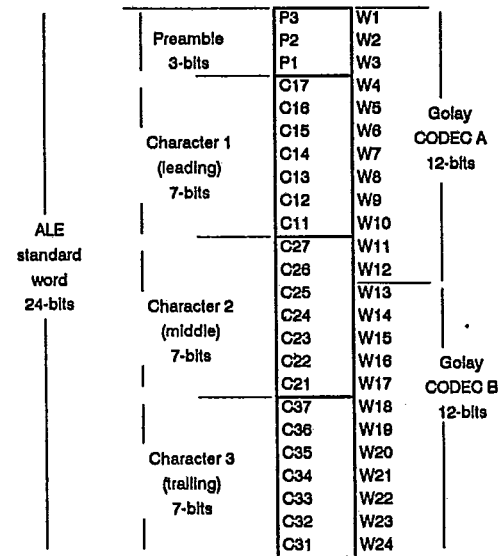| ALE standard word 24-bits | | | |
|---|---|---|---|
| Preamble 3-bits | P3 | W1 | |
| | P2 | W2 | |
| | P1 | W3 | |
| Character 1 (leading) 7-bits | C17 | W4 | Golay CODEC A 12-bits |
| | C16 | W5 | |
| | C15 | W6 | |
| | C14 | W7 | |
| | C13 | W8 | |
| | C12 | W9 | |
| | C11 | W10 | |
| Character 2 (middle) 7-bits | C27 | W11 | |
| | C26 | W12 | |
| | C25 | W13 | |
| | C24 | W14 | |
| | C23 | W15 | |
| | C22 | W16 | Golay CODEC B 12-bits |
| | C21 | W17 | |
| Character 3 (trailing) 7-bits | C37 | W18 | |
| | C36 | W19 | |
| | C35 | W20 | |
| | C34 | W21 | |
| | C33 | W22 | |
| | C32 | W23 | |
| | C31 | W24 | |

**Figure 4. Basic Word Format**

("basic" words) to be transmitted. The basic words can be downloaded from the processor in either a three-byte packed format or a four-byte unpacked format. Figure 4 shows the format of the Basic Word. The SRT-141A/1045 then performs Golay encoding, interleaving and redundancy encoding on each basic word and outputs the resulting 147-bit triple redundant words (Trw) to the modem for transmission.

### Basic Word FIFO

The SRT-141A/1045 incorporates an eight word deep 24-bit wide FIFO. Basic words are stored in the FIFO by the system processor and are read out under control of the SRT-141A/1045 for transmission. The transmit FIFO removes much of the processing overhead from the system processor. Three FIFO flags are available for use by the system processor indicating FIFO full, FIFO half empty and FIFO empty. After reset the FIFO is cleared.

### Encoding Functions

The SRT-141A/1045 supports all data formatting requirements including:

● **Golay Encoding.** Generation of Golay codewords A and B corresponding to the two twelve bit halves of the basic word.

● **Interleaving.** Interleaving of the 48 bit word comprising Golay codewords A and B (interleaving degree = 2) and addition of a zero stuff bit to form the 49-bit majority word.
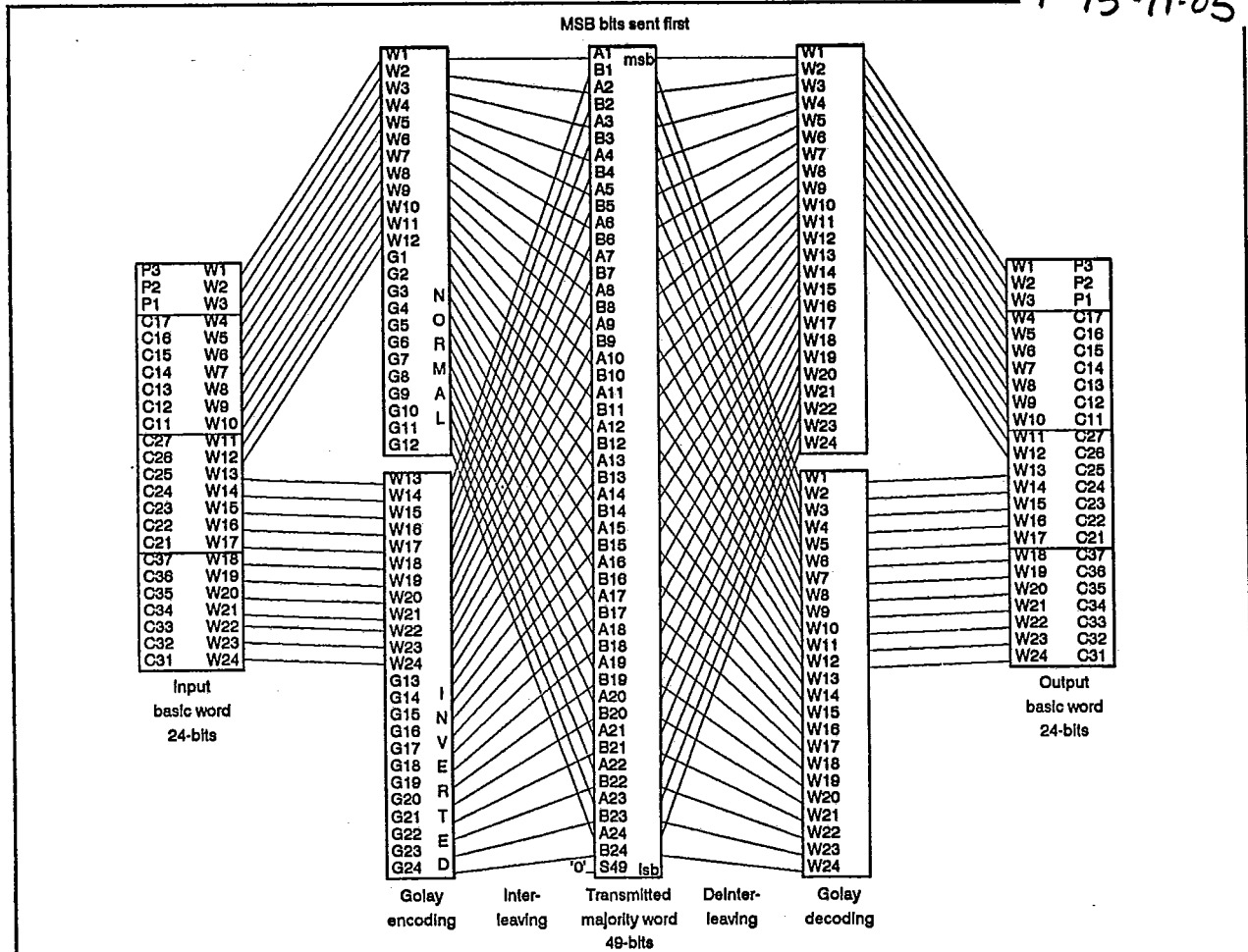
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MSB bits sent first

**Figure 5. Basic Word Coding**

- **Redundancy Encoding.** Triple redundantly transmitting the resulting 49-bit majority word.

Each basic word received from the processor is split into two, twelve bit halves corresponding to the data sections of Golay codewords A and B.

Figure 5 shows the format of the 24-bit basic ALE word and the corresponding 49-bit majority word. Each 49-bit majority word is transmitted contiguously three times to form the 147-bit triple redundant word (Trw).

### Clock source

Internally generated transmit clocks (TXCLK1,2) of 375Hz and 125Hz can be used to clock out the Trw in either a serial or tri- bit format respectively (TX2-TX0). Selection of either serial or tri-bit format is made during device initialization by the Format Control Register.

If desired, the Trw can be clocked out using an externally supplied 375Hz clock (EXCLK).

### Interrupt Generation

A flexible transmit interrupt mechanism is provided in the SRT-141A/1045 to further offload the system processor. The interrupt can be programmed by the Format Control Register to occur either when the transmit FIFO is empty or half empty. The interrupt will be internally cleared when the interrupting condition is removed. The interrupt can be programmed to be either a low level or low pulse. The output driver for the interrupt line is an open drain to facilitate wire-OR-ing of interrupts.

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## Receive Operation

In RECEIVE MODE the received triple redundant words from the modem are majority vote decoded, de-interleaved and Golay decoded to recover the basic 24-bit words. In addition, the decoded characters, preamble and word phase are checked against the preset acceptance criteria. A receive interrupt (RINT*) is generated to the system processor to indicate that a validated receive word has been decoded and is ready to be read. The status data and flag information reflects the state of the word relative to the preset word acceptance criteria.

### Pattern Synchronization

The SRT-141A/1045 decodes on a bit-by-bit basis the most recently received 147 bits in search of valid incoming triple redundant words. The preset threshold acceptance criteria used to establish the 147-bit Trw pattern synchronization must first be downloaded by the processor into the internal registers (refer to Table 1). The internal registers that must be preset with acceptance criteria values and the corresponding status flags are:

- Majority vote decode threshold (Majority Vote Flag).
- Acceptable Preambles (Preamble Flag).
- Acceptable Character set (Character Flags).
- Golay correction mode (A and B Correctable Flags).

When the pattern synchronization criteria are met a receive interrupt (RINT*) is generated. The processor then reads the status and data bytes. If the call is accepted, then a triple redundant word phase (Trwp) value register is preset by the processor with the phase of the Trw's associated with the call. An associated comparator is also enabled with the desired acceptable window (Trwp Window Register). The processor has access to the Measured Trwp Register associated with every received Trw.

Once pattern synchronization is established, majority vote decoding and Golay codeword pair decoding are only necessary every Trw period (147 bits or 392 msec) to continue reception of the established call. However, in order to detect new calls that may come in (and momentarily override the established call), it is necessary to continue looking for valid basic words on a bit-by-bit basis ("always listening").

### Majority Vote Decoding

Each input bit time, the SRT-141A/1045 majority vote decoder collates a pattern comprised of three bits equally spaced 49 input bit times apart. The SRT-141A/1045 then maintains a running count of the number of non-unanimous votes (2 out of 3) over the prior 147 bit times. The number of non-unanimous votes must be less than or equal to the value preset in the Majority Vote Decoder Threshold register. In an error free transmission, whenever the 3 corresponding bits of each 49 bit majority word comprising the Trw are aligned these bits are identical and the non-unanimous vote count will be zero. The majority vote threshold flag indicates the result of the comparison and is included in the receive interrupt generation decision.

The majority vote decoding of the 147-bit Trw results in a 49-bit majority word which is then de-interleaved and Golay decoded. The majority vote decode logic is bypassed if other than triple- redundant transmission format is selected (see "FEC Bypass Modes").

### De-interleaving

The resulting 49-bit majority word from the majority vote logic is de-interleaved and the stuff bit is discarded.

### Golay Decoding

The de-interleaved 48-bit word is passed through the Golay correction function in two 24-bit halves (codewords A and B). The Golay decoding function may be preset by the system processor via the Golay Correction Mode Register to one of four error correction/detection modes (the "Golay correction mode").

The Golay correction mode sets the maximum number of errors guaranteed detectable and correctable per Golay codeword and the maximum number of errors guaranteed detectable but not guaranteed correctable per Golay codeword.

The successful Golay decode status flags (the A or B Correctable Flags) are set to zero (indicating a successful Golay decode) if the number of errors reported by the Golay decoder is less than or equal to detectable and correctable error value determined by the preset Golay correction mode.

Figure 6 shows the Golay codeword correctable flag status, the decoder error count report, the actual maximum error count possible in the decoded data, versus, the actual number of errors present in the input Golay codeword.

### Preamble Validation

The recovered 24-bit basic word is verified for an acceptable 3-bit preamble value. Preambles are accept-

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| Actual No. of input codeword errors per codeword | Number of errors reported by decoder (always between 0 and 4) | Golay Correction mode | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | 3/4 | | 2/5 | | 1/6 | | 0/7 | |
| | | CF | OEC | CF | OEC | CF | OEC | CF | OEC |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 2 | 2 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 |
| 3 | 3 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| 4 | 4 | 1 | 4 | 1 | 4 | 1 | 4 | 1 | 4 |
| 5 | 3 | 0 | 8 | 1 | 8 | 1 | 8 | 1 | 8 |
| 6 | 4 (84%) | 1 | 6 | 1 | 6 | 1 | 6 | 1 | 6 |
| 6 | 2 (16%) | 0 | 8 | 0 | 8 | 1 | 8 | 1 | 8 |
| 7 | 3 (98%) | 0 | 8 | 1 | 8 | 1 | 8 | 1 | 8 |
| 7 | 1 (2%) | 0 | 8 | 0 | 8 | 0 | 8 | 1 | 8 |
| 8 | 0 (0.1%) | 0 | 8 | 0 | 8 | 0 | 8 | 0 | 8 |
| 8 | 2 (13.2%) | 0 | 8 | 0 | 8 | 1 | 8 | 1 | 8 |
| 8 | 4 (86.7%) | 1 | 8 | 1 | 8 | 1 | 8 | 1 | 8 |
| . | . | . | . | . | . | . | . | . | . |

CF = Correctable Flag (0 = Ok)
OEC = Output Error Count (actual maximum error count possible in decoder)
Golay Correction Mode = n/m (n = correction threshold, m = detection threshold)
Above shaded area = Gauranteed correctable
Shaded area = Gauranteed detectable

*Notes:*
*1. If the actual number of errors exceeds the detection threshold range (m), for the correction mode selected, then the correctable flag may be erroneously set.*
*2. Percentages shown indicate the probability of occurance of the corresponding reported error count.*

**Figure 6. Error Count Status**

able is they match any of the preset preamble values. The preamble flag is set to zero if the decoded basic word has an acceptable preamble.

**Character Validation**

The three, 7-bit characters from the 24-bit basic word are separately verified for an acceptable value. Characters are acceptable if they belong to the preset character set. Acceptable characters are indicated by setting the appropriate character flag to zero.

**Interrupt Generation**

A flexible receive interrupt mechanism is provided in the SRT-141A/1045 to further offload the system processor. When enabled by the processor, receive interrupts are generated for all received validated basic words. The interrupt will be internally cleared when the received basic word has been read by the system processor. The interrupt can be programmed to be either a low level or low pulse. The output driver for the interrupt line is an open drain to facilitate wire-or-ing of interrupts.

**Triple redundant word phase (Trwp).**

The phase of the triple redundant word boundaries for each call received and accepted is measured and stored (Measured Trwp). The phase parameter is expressed as a 10-bit binary count measured with respect to an internal timer counter. The phase parameter is measured and assigned to the call during call synchronization. This criteria only applies to established calls and requires that the phase of the

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received Trw match (within a preset phase window) the preset phase established during call synchronization.

Since each call is composed of contiguous 147-bit triple redundant words, knowing the phase of the incoming call's triple redundant words enables pattern synchronization to be quickly re-established if the call should be overridden by another incoming call or disrupted for any reason.

For example, if during the reception of CALL A, a Trw is received that meets the pattern synchronization criteria but does not correspond to any existing call, i.e. its Trwp does not correspond to any preset Trwp (Trwp OK FLAG = 1), the Rx interrupt is generated. The Rx interrupt signals the processor to look at this new basic word and take the following action:

If this basic word corresponds to a new call (CALL B) overriding existing CALL A (e.g., CALL B collides with CALL A) then the processor may choose to:

- Receive the new call basic words by reading the Trwp of CALL B (Trwpb) and presetting a second phase match register to Trwpb. CALL A is then ignored (by disabling the Trwpa match register) until CALL B is processed. When CALL B terminates, the processor may choose to re-establish the reading of CALL A words again by presetting a phase match register to Trwpa.

- Receive both CALL B and A even though CALL A and/or CALL B words may not meet the acceptance criteria and may contain bit errors due to the collision of the two received signals.

- Ignore CALL B and continue to read CALL A (even though CALL A words may not meet the acceptance criteria and may also contain errors).

The basic word may not correspond to a valid incoming call. In this case the processor may then choose to ignore the new incoming basic words.

Including correct Trwp in the basic word validation criteria also provides a measure of call security against false or counterfeit basic words that may, except for redundant word phase, meet all the validation criteria. For example, false or counterfeit words could be generated by an illegal or unauthorized transmitter intent on compromising the security of the call. However, transmitting these words with a phase matching the true call's phase (within the phase match window) would be very difficult if not impossible.

Even though it is unlikely that more than one call will be actively received and processed at any one time, a total of three Trwp registers are included in the SRT-141A/1045. This permits up to three calls to be received and processed simultaneously.

When a Trwp phase match occurs and that phase comparator is enabled a receive interrupt is always generated, regardless of the current state of the status flags used to generate an interrupt during call synchronization. If more than one new 147-bit value is received with a phase match (large phase match window value) then a receive interrupt is generated at each bit position within the phase match window.

## FEC Bypass Mode

The SRT141A/1045 gives the user the flexibility to bypass the encoding/decoding operations implemented by the SRT 141A/1045. This coding bypass flexibility lets the user utilize the chip as a general purpose error correction/detection coder/decoder in non-141A or non-1045 applications. For example, a good quality VHF channel running at 9600 baud may only require Golay coding without interleaving or redundancy to satisfy the desired BER requirements. A data throughput rate of 9600 baud can easily be handled by the chip.

The four encoding/decoding configuration modes that can be selected are:

- Golay coding, interleaving (degree = 2) and triple redundancy coding. This is the normal coding required by the 141A and 1045 ALE and DTM modes.

- Golay coding and interleaving (degree = 2). No 49th "0" stuff bit.

- Golay coding (no interleaving, no inverted parity on code word B).

- No coding (direct modem access).

## Non-Standard Bit Rates

The SRT-141A/1045 can be utilized in many applications requiring other than the normal 375Hz bit rate. In such applications the external transmit clock input must be used. If redundancy encoding is used then the triple redundant word phase counter must be adjusted by the Trwp Modulus Registers so that it's modulus matches the 147-bit period. The least significant bit of the Trwp counter has a weight of 0.5msec (reset state of the modulus comparator register is 794 corresponding to the 147-bit period of 392msec).

## TABLE 1. Register Description

| Address | Type | Bit Field | Description |
|---------|------|-----------|-------------|
| 00h | Read/Write | | **Majority Vote Decode Threshold / Golay Correction Mode** |
| | | 0-5 | Non-unanimous vote threshold. |
| | | | If the non-unanimous vote count is less than or equal to the non-unanimous vote threshold then the UVC flag is cleared. |
| | | 6-7 | Rx. Golay correction mode: |
| | | | *00 - 0/7 (correct 0 / detect 7).* |
| | | | *01 - 1/6 (correct 1 / detect 6).* |
| | | | *10 - 2/5 (correct 2 / detect 5).* |
| | | | *11 - 3/4 (correct 3 / detect 4).* |
| | | | The Golay correction mode defines the number of acceptable corrected/detected errors. |
| | | | The reset state of this byte is 00h. |
| 01h | Read/Write | | **Acceptable Preambles** |
| | | 0 | Rx preamble 000 acceptable. |
| | | 1 | Rx preamble 001 acceptable. |
| | | 2 | Rx preamble 010 acceptable. |
| | | 3 | Rx preamble 011 acceptable. |
| | | 4 | Rx preamble 100 acceptable. |
| | | 5 | Rx preamble 101 acceptable. |
| | | 6 | Rx preamble 110 acceptable. |
| | | 7 | Rx preamble 111 acceptable. |
| | | | Each bit corresponds to an acceptable preamble. |
| | | | The reset state of this byte is 00h. |
| 02h | Read/Write | | **Acceptable Character Set / FEC Bypass Mode** |
| | | 0-1 | Acceptable character set, char 3: |
| | | | These bits define the set of acceptable characters as follows: |
| | | | *00 - Basic 38.* |
| | | | *01 - Basic 38, ignore hi-bit.* |
| | | | *10 - Expanded 64.* |
| | | | *11 - Full 128.* |
| | | 2-3 | Acceptable character set, char 2: (as char 3) |
| | | 4-5 | Acceptable character set, char 1: (as char 3) |
| | | 6-7 | FEC bypass mode: |
| | | | These bits define both the transmit and receive coding modes. |
| | | | *00 - Golay/interleave/triple redundancy (ALE/DBM).* |
| | | | *01 - Golay/interleave (DBM).* |
| | | | *10 - Golay.* |
| | | | *11 - Direct to modem.* |
| | | | The reset state of this byte is 00h. |

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| Address | Type | Bit Field | Description |
|---------|------|-----------|-------------|
| 03h | Read/Write | | **Format control** |
| | | 0 | **TX data input format:** This bit defines the format of the transmit data as written by the system processor. *0 - packed.* *1 - unpacked.* |
| | | 1 | **TX and RX data format:** This bit defines the output format of the transmit section and input format of the receive section. *0 - serial.* *1 - 3-bit parallel (tri-bit).* |
| | | 2 | **TX clock source:** This bit selects the bit clock source for the transmit section. *0 - internal.* *1 - external.* |
| | | 3-4 | **Interrupt enable:** These bits individually enable the receive and transmit interrupts. *00 - Disable interrupts.* *X1 - Enable TX interrupt.* *1X - Enable RX interrupt.* |
| | | 5 | **TX Interrupt level:** This bit defines the state of the TX FIFO which will cause the interrupt to be asserted. *0 - TX interrupt on FIFO half full, 4 or less words.* *1 - TX interrupt on FIFO empty.* |
| | | 6 | **Interrupt mode:** This bit defines the interrupt output mode for both receive and transmit interrupts. *0 - Active low level.* *1 - Active low pulse.* |
| | | 7 | **Test mode loopback:** This bit selects the input to the receive section. *0 - normal operation.* *1 - transmit section loops back to receive section.* The reset state of this byte is 00h. |
| 04h | Read/Write | | **Trwp A Value** |
| | | 0-7 | **Trwp A accept phase (ls).** Triple redundant word phase A compare value, least significant 8 bits. The reset state of this byte is 00h. |

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| Address | Type | Bit Field | Description |
|---------|------|-----------|-------------|
| 05h | Read/Write | | **Trwp A Window** |
| | | 0-1 | Trwp A accept phase (ms). |
| | | | Triple redundant word phase A compare value, most significant two bits. |
| | | 2-6 | Trwp A accept window. |
| | | | Triple redundant word phase window A: |
| | | | *00000 - +/- 0.0 mS.* |
| | | | *00001 - +/- 0.5 mS.* |
| | | | *00010 - +/- 1.0 mS.* |
| | | | . |
| | | | . |
| | | | *11110 - +/- 15.0 mS.* |
| | | | *11111 - disable TRWP A.* |
| | | 7 | Trwp A enable. |
| | | | Active high enable for TRWP A comparator. |
| | | | The reset state of this byte is 00h. |
| 06h | Read/Write | | **Trwp B Value** |
| | | 0-7 | Trwp B accept phase (ls). |
| | | | Triple redundant word phase B compare value, least significant 8 bits. |
| | | | The reset state of this byte is 00h. |
| 07h | Read/Write | | **Trwp B Window** |
| | | 0-1 | Trwp B accept phase (ms). |
| | | | Triple redundant word phase B compare value, most significant two bits. |
| | | 2-6 | Trwp B accept window. |
| | | | Triple redundant word phase window B: |
| | | | (as Trwp A) |
| | | 7 | Trwp A enable. |
| | | | Active high enable for Trwp B comparator. |
| | | | The reset state of this byte is 00h. |
| 08h | Read/Write | | **Trwp C Value** |
| | | 0-7 | Trwp C accept phase (ls). |
| | | | Triple redundant word phase C compare value, least significant 8 bits. |
| | | | The reset state of this byte is 00h. |

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| Address | Type | Bit Field | Description |
|---------|------|-----------|-------------|
| 09h | Read/Write | | **Trwp C Window** |
| | | 0-1 | Trwp C accept phase (ms). |
| | | | Triple redundant word phase C compare value, most significant two bits. |
| | | 2-6 | Trwp C accept window. |
| | | | Triple redundant word phase window C: |
| | | | (as Trwp A) |
| | | 7 | Trwp C enable. |
| | | | Active high enable for Trwp C comparator. |
| | | | The reset state of this byte is 00h. |
| 0Ah | Read/Write | | **Trwp Modulus ls** |
| | | 0-7 | Trwp modulus (ls). This byte controls the modulus of the Trwp phase measurement counter. |
| | | | The reset state of this byte is 19h. |
| 0Bh | Read/Write | | **Trwp Modulus ms** |
| | | 0-1 | Trwp modulus (ms). This byte controls the modulus of the Trwp phase measurement counter. |
| | | 2-7 | Not used. |
| | | | The reset state of this byte is 03h |
| | | | *Note: Trwp Modulus count value = 2(Trw period in msec) - 1* |
| 0Ch | Read/Write | | **MS Transmit data** |
| | | 0-7 | Tx data ms (packed mode or read). |
| | | | or |
| | | 0-2 | Tx data ms (unpacked mode write). |
| | | 3-7 | Not used (unpacked mode). |
| | | | Transmit data output FIFO (note read value is last value written). The reset state of the Transmit FIFO is all 00h. |
| 0Dh | Read/Write | | **Transmit data** |
| | | 0-7 | Tx data (packed mode or read). |
| | | | or |
| | | 0-6 | Tx data (unpacked mode write). |
| | | 7 | Not used (unpacked mode). |
| | | | Transmit data output FIFO (note read value is last value written). The reset state of the Transmit FIFO is all 00h. |

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| Address | Type | Bit Field | Description |
|---------|------|-----------|-------------|
| 0Eh | Read/Write | | **Transmit data** |
| | | 0-7 | Tx data ls (packed mode or read). |
| | | | or |
| | | 0-6 | Tx data (unpacked mode write). |
| | | 7 | Not used (unpacked mode). |
| | | | Transmit data output FIFO (note read value is last value written). The reset state of the Transmit FIFO is all 00h. |
| 0Fh | Read/Write | | **Transmit data** |
| | | 0-7 | spare (packed mode). |
| | | | or |
| | | 0-6 | Tx data ls (unpacked mode write). |
| | | 7 | Not used (unpacked mode). |
| | | | Transmit data output FIFO (note read value is last value written). The reset state of the Transmit FIFO is all 00h. |
| 10h | Read only | | **Receive status summary** |
| | | 0-2 | Preamble. |
| | | 3 | Majority threshold flag (0 - acceptance). |
| | | 4 | A and B correctable flag (0 - acceptance). |
| | | 5 | Preamble flag (0 - acceptable). |
| | | 6 | Character flag (0 - all acceptable). |
| | | 7 | TRWP flag (0 - acceptable). |
| | | | The reset state of this byte is 07h |
| 11h | Read only | | **Measured Trwp ms** |
| | | 0-7 | Measured Trwp phase (ls). |
| | | | The reset state of this byte is 00h. |
| 12h | Read only | | **Measured Trwp ls / Interrupt Status** |
| | | 0-1 | Measured Trwp phase (ms). |
| | | 2 | Tx interrupt status (0 - asserted) |
| | | 3 | Rx interrupt status (0 - asserted) |
| | | 4 | Tx FIFO half full, 4 or less words (0 - asserted). |
| | | 5 | Tx FIFO empty, 0 words (0 - asserted). |
| | | 6 | Not used. |
| | | 7 | Tx or Rx interrupt status (0 - either asserted). |
| | | | The reset state of this byte is 08h |

**13**

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| Address | Type | Bit Field | Description |
|---------|------|-----------|-------------|
| 13h | Read only | | **Majority threshold status** |
| | | 0-5 | Majority vote count. |
| | | 6 | Not used. |
| | | 7 | Majority threshold (UVC) flag (0 - acceptable UVC comparision) |
| | | | The reset state of this byte is 00h |
| 14h | Read only | | **Golay Correction status** |
| | | 0-1 | No. of errors, code word A. |
| | | 2 | Word A correctable (0 - correctable) |
| | | 3-4 | No. of errors, code word B. |
| | | 5 | Word B correctable (0 - correctable) |
| | | 6 | Words A and B correctable (0 - correctable) |
| | | 7 | Four error flag (0 - less than 4 in A & B) |
| | | | The reset state of this byte is 00h |
| 15h | Read only | | **Receive data ls** |
| | | 0-6 | Rx data (ls) |
| | | 7 | acceptable character (0 - acceptable) |
| | | | The reset state of this byte is 80h |
| 16h | Read only | | **Receive data** |
| | | 0-6 | Rx data |
| | | 7 | acceptable character (0 - acceptable) |
| | | | The reset state of this byte is 80h |
| 17h | Read only | | **Receive data ms** |
| | | 0-6 | Rx data (ms) |
| | | 7 | acceptable character (0 - acceptable) |
| | | | The reset state of this byte is 80h |
| 18h-1Fh | | | **Reserved** |
| | | | Not used. |
| | | | Reserved for future use. |

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## TABLE 2. Pin Input/Output Signal Descriptions

### (sorted alphabetically)

| Pin No. | Name | Description |
|---|---|---|
| 14-18 | A4-A0 | **Address Bus (Input; Asynchronous)**<br>The five bit address input bus is used to select the internal register to be read or written to. The selected address can be latched internally using the address strobe. The internally latched address is used to select one of the internal mode or data registers. |
| 8 | AS* | **Address Strobe (Input; Asynchronous, Active LOW)**<br>A low level on this input transfers the address value to the internal address latch when the address value is presented on the dedicated address bus. In multiplexed address/data mode this input is unused and may be left open. |
| 7 | CS* | **Chip Select (Input; Asynchronous, Active LOW)**<br>A low level on this input selects the device for read or write over the processor data bus. |
| 5 | CLKOUT | **System clock (Output)**<br>This output provides the system with a 50% duty cycle 750 kHz waveform. All device pin timings are relative to CLKOUT. |
| 19-22, 24-27 | D7-D0 | **Data Bus (Input/Output)**<br>Bi-directional port which allows transfer of data into or out of the selected internal register. The lower order 5 bits (D4-D0) can also be used to transfer the internal register address into the internal address latches, this mode of operation is selected by the interface select pins. |
| 33 | EXCLK | **External Transmit Clock (Input; Asynchronous, Edge sensitive, Active LOW)**<br>An external 375Hz clock can be supplied to this input. The transmit data will be synchronized to this input when it is selected by an internal control bit. Transmit data will be clocked out on the HIGH-to-LOW transition of this input. |
| 9 | F1 | **Data Strobe or Read Strobe (Input; Asynchronous)**<br>The function of this input pin is selected by the interface type select pins (S1-S0). The data strobe input is used in conjunction with the read/write designator to transfer data into or out of the device. The read strobe input is used to transfer data out of the device. |
| 10 | F2 | **Write strobe or Read/Write Designator (Input; Asynchronous)**<br>The function of this input pin is selected by the interface type select pins (S1-S0). The read/write designator input is used in conjunction with the data strobe input to transfer data into or out of the device. The write strobe input is used to transfer data into the device. |
| 36-38 | RX2-RX0 | **Modem Receive Data (Input; Asynchronous)**<br>This three bit bus is used to transfer data from the external modem to the device. An internal control bit selects either three bit parallel or serial input data; in serial mode input data is presented on RX2. |

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| Pin No. | Name | Description |
|---|---|---|
| 39 | RXCLK | **Modem Clock (Input; Asynchronous, Edge sensitive, Active LOW)** <br><br> The 375Hz clock input is supplied by the external modem. This clock is synchronized to the modem data, modem data is sampled on the HIGH-to-LOW transition of this input. |
| 6 | RES* | **Reset (Input; Asynchronous, Active LOW)** <br><br> This input places the device in Reset mode. In Reset mode the SRT-141A/1045 immediately terminates its present activity and enters a dormant state. All internal storage registers will be initialized. |
| 43 | RINT* | **Receive Interrupt (Output; Asynchronous, Active LOW open drain)** <br><br> When enabled by an internal control bit this output is asserted when new receive data is available. This output can be configured to supply either a continuous low level or a low pulse. The interrupt is cleared by reading the receive data register. This output is supplied as an open drain output to allow wire-OR-ing of interrupts, an external pull-up resistor must be provided. |
| 13,12 | S1,S0 | **Interface Type Select (Input; Asynchronous)** <br><br> These inputs are used to select the processor interface type. These inputs are provided with internal passive pull-up resistors. The interface function is encoded as follows: |

| S1 | S0 | Function |
|---|---|---|
| X | 0 | F1 functions as an Active LOW data strobe; F2 functions as Read/Write designator, high indicates read, low indicates write. |
| X | 1 | F1 functions as an Active LOW read strobe; F2 functions as an Active LOW write strobe. |
| 0 | X | Address is multiplexed on the lower order data bus bits. |
| 1 | X | Address is input on the dedicated address bus. |

*Note: X denotes don't care.*

| Pin No. | Name | Description |
|---|---|---|
| 42 | TEST | **Test (Input; Asynchronous, Active LOW)** <br><br> When this input is active the device is in Test mode. Test mode is used for device test only, this pin is internally pulled up and may be left open. |
| 44 | TINT* | **Transmit Interrupt (Output; Asynchronous, Active LOW open drain)** <br><br> When enabled by an internal control bit this output is asserted when the transmit data register is empty. The transmit data output register is internally double buffered to simplify contiguous transmission of data. This output can be configured to supply either a continuous low level or a low pulse. The interrupt is cleared by writing to the transmit data output register. This output is supplied as an open drain output to allow wire-OR-ing or interrupts, an external pull-up resistor must be provided. |
| 29-31 | TX2-TX0 | **Modem Transmit Data (Output; synchronous)** <br><br> This three bit output bus is used to transfer data from the device to an external Modem. An internal control bit selects either three bit parallel or serial output data, in serial output mode data is presented on TX2. |

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| Pin No. | Name | Description |
|---------|------|-------------|
| 32 | TXCLK | **Transmit Clock (Output; Synchronous, Edge sensitive, Active LOW)**<br>This 375Hz or 125Hz clock output is synchronized to the transmit data. An internal control bit selects this clock to be supplied from either an internal or external source. Internally supplied clock is 375Hz in serial output mode or 125Hz in tri-bit output mode. The HIGH-to-LOW transition of this output may be used by an external modem to sample the transmit data. |
| 12,34 | Vcc | **System Power +5 V power supply.** |
| 1,4,23 | Vss | **System Ground** |
| 2-3 | X1-X2 | **Crystal inputs**<br>X1 and X2 provide an external connection for a 6 MHz fundamental mode parallel resonant crystal for the internal crystal oscillator. X1 can interface to an external clock source instead of a crystal (if an external clock is used X2 should be left open). The 6 MHz input clock is internally divided by eight to generate the clock signal CLKOUT. |

Note: * indicates active low signal.

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## ABSOLUTE MAXIMUM RATINGS

Storage temperature . . . . . . . . . . . . . . . . . .-65C to +150C

Voltage on any pin with respect to VSS . . . . . . .-0.5 to +7.0V

*Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may
cause permananent device failure. Functionality at or above these limits is
not implied. Exposure to absolute maximum ratings for extended periods
may affect device reliability.*

## OPERATING RANGES

**Commercial (C) Devices**

Temperature . . . . . . . . . . . . . . . . . . . . . .0 to 70C

Supply Voltage . . . . . . . . . . . . . . . . . . . .+4.75V to +5.25V

**Industrial (I) Devices**

Temperature . . . . . . . . . . . . . . . . . . . . .-40C to +85C

Supply Voltage . . . . . . . . . . . . . . . . . . . .+4.5V to +5.5V

**Military (M) Devices**

Temperature . . . . . . . . . . . . . . . . . . . . .-55C to +125C

Supply Voltage . . . . . . . . . . . . . . . . . . . .+4.5V to +5.5V

*Operating ranges define those limits between which the functionality of the
device is guaranteed.*

# DC CHARACTERISTICS

**(over operating range unless otherwise specified)**

| Parameter Symbol | Parameter description | Test Conditions | Min. | Max. | Unit. |
|---|---|---|---|---|---|
| $V_{il}$ | input LOW voltage | | -0.5 | 0.8 | V |
| $V_{ih}$ | input HIGH voltage | | 2.0 | $V_{cc}+0.5$ | V |
| $V_{ol}$ | output LOW voltage | $I_{ol}=4mA$ | | 0.45V | V |
| $V_{oh}$ | output HIGH voltage | $I_{oh}=-4mA$ | 2.4 | | V |
| $I_{il}$ | input leakage current | $0.45V < V_{in} < V_{cc}-0.45V$ | | +/-10 | uA |
| $I_{lo}$ | output leakage current | $0.45V < V_{in} < V_{cc}-0.45V$ | | +/-10 | uA |
| $I_{ccop}$ | operating power-supply current | $V_{cc}=5.25$, outputs floating; reset held active. | | 250 | mA |
| $C_{in}$ | input capacitance, other than X1, X2 | | | 20 | pF |
| $C_{out}$ | output capacitance | | | 20 | pF |

# SWITCHING AND TIMING CHARACTERISTICS

**(over operating range unless otherwise specified)**

| Parameter Symbol | Parameter description | Test Conditions | Min. | Max. | Unit. |
|---|---|---|---|---|---|
| $T_{res}$ | Reset pulse width | | 100 | | nsec |
| $T_{int}$ | Interrupt pulse width | | 1.3 | | usec |
| $T_{mck}$ | Modem clock period | | 10 | | usec |
| $T_{mckl}$ | Modem clock low | | 4 | | usec |
| $T_{mckh}$ | Modem clock high | | 4 | | usec |
| $T_{mrs}$ | Modem receive data setup before modem clock. | | 20 | | nsec |
| $T_{mrh}$ | Modem receive data hold after modem clock | | 10 | | nsec |
| $T_{eck}$ | External transmit clock period | | 10 | | usec |

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| Parameter Symbol | Parameter description | Test Conditions | Min. | Max. | Unit. |
|---|---|---|---|---|---|
| $T_{eckl}$ | External transmit clock low | | 4 | | usec |
| $T_{eckh}$ | External transmit clock high | | 4 | | usec |
| $T_{mts}$ | Modem transmit data setup time before TXCLK. | | 100 | | nsec |
| $T_{mth}$ | Modem transmit data hold time after TXCLK | | 50 | | nsec |
| $T_{css}$ | Chip select setup time before address or data strobe | | 10 | | nsec |
| $T_{csh}$ | Chip select hold after data strobe | | 5 | | nsec |
| $T_{as}$ | Address setup before rising edge of address strobe or falling edge of data strobe | | 10 | | nsec |
| $T_{ah}$ | Address hold after rising edge of address strobe, data strobe, read strobe or write strobe. | | 5 | | nsec |
| $T_{rws}$ | Read/write setup before data strobe low | | 0 | | nsec |
| $T_{rwh}$ | Read/write hold after data strobe high | | 5 | | nsec |
| $T_{rd}$ | Read enable time, data strobe or read strobe to data valid | | | 20 | nsec |
| $T_{rdh}$ | Read data hold time, rising edge of data strobe or read strobe to data high impedance | | 5 | 15 | nsec |
| $T_{ad}$ | Rising edge of address strobe to falling edge of data strobe | | 0 | | nsec |
| $T_{wds}$ | Write data valid before rising edge of data strobe or write strobe | | 10 | | nsec |
| $T_{wdh}$ | Write data hold after rising edge of data strobe or write strobe | | 5 | | nsec |

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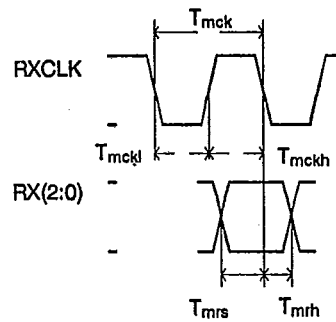| Parameter Symbol | Parameter description | Test Conditions | Min. | Max. | Unit. |
|---|---|---|---|---|---|
| $T_{rec}$ | Write recovery time, rising edge of data strobe or write strobe to start of next read or write access | | 10 | | usec |
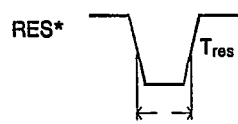


**Reset timing**
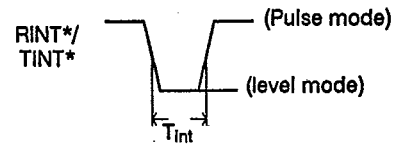


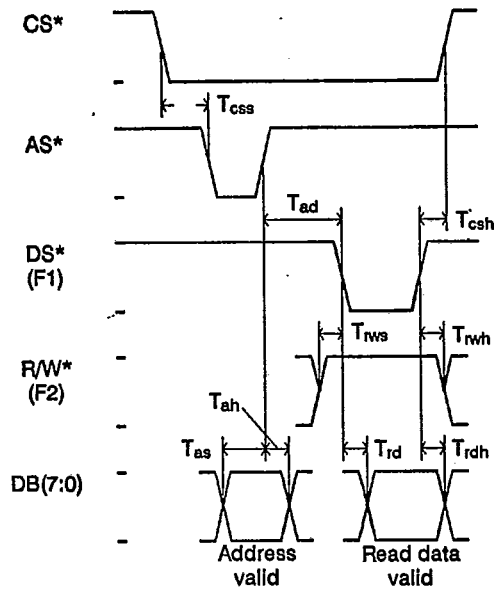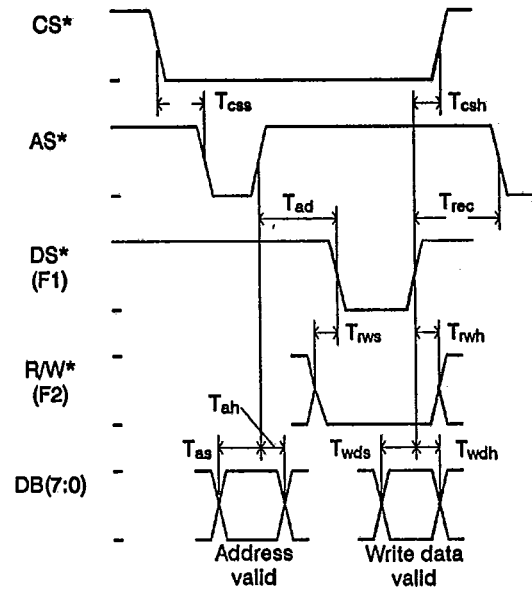**Interrupt timing**
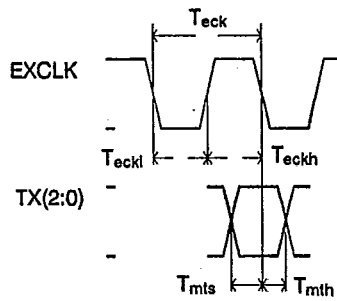


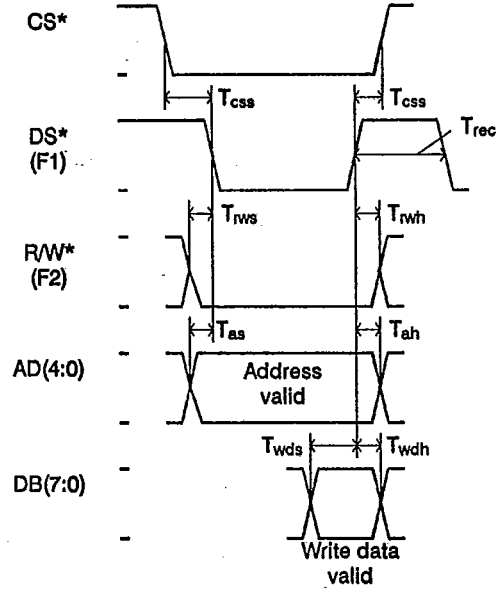**Modem transmit timing**



**Modem receive timing**

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## PROCESSOR I/O TIMING



Read timing, (S1 = 0, S0 = 0)



Write timing, (S1 = 0, S0 = 0)
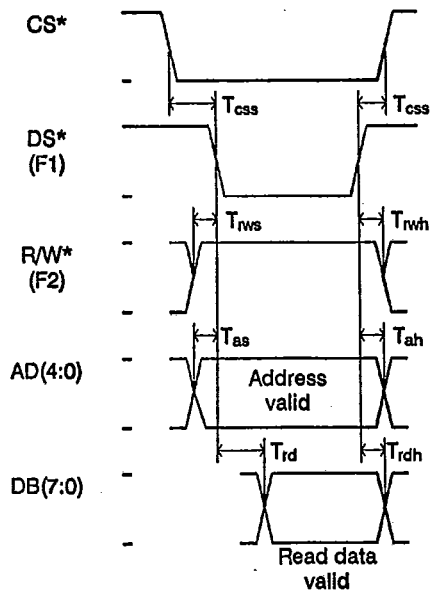


Read timing, (S1 = 1, S0 = 0)
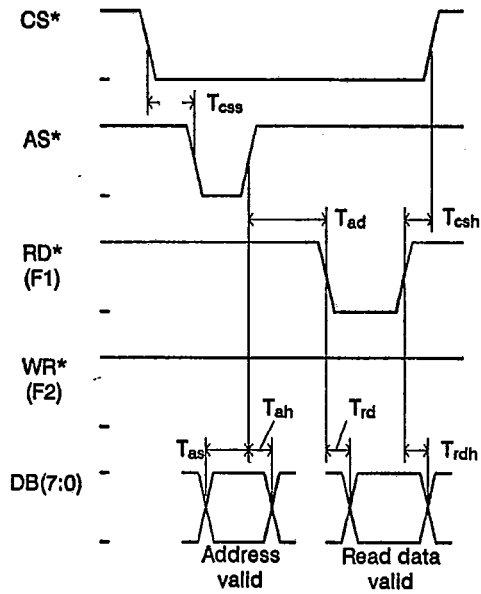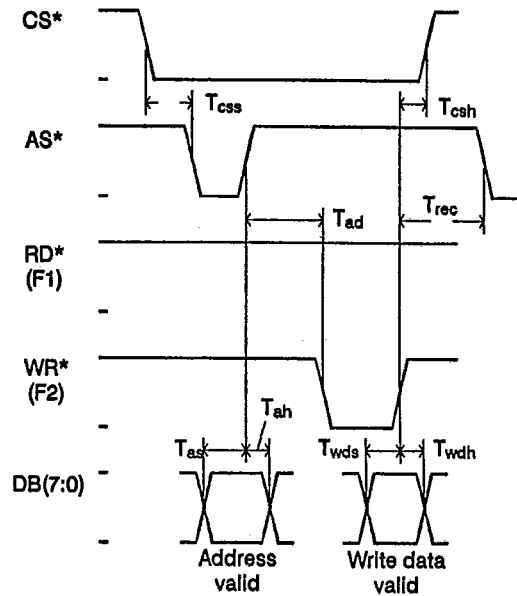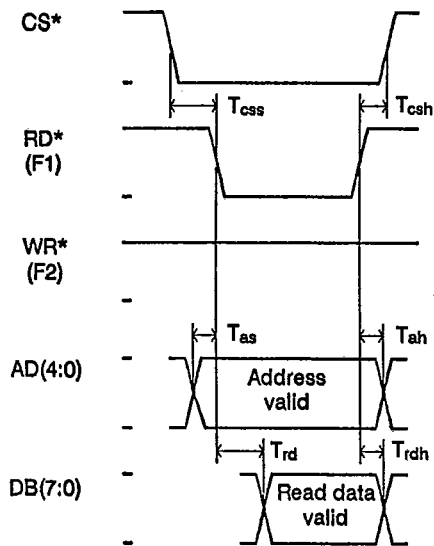


Write timing, (S1 = 1, S0 = 0)

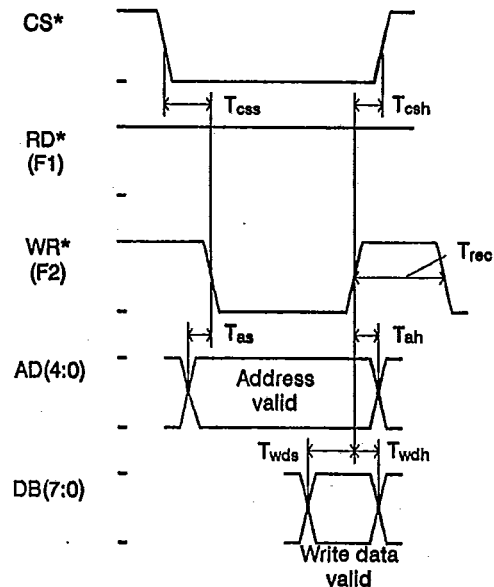## PROCESSOR I/O TIMING (continued)



Read timing, (S1 = 0, S0 = 1)



Write timing, (S1 = 0, S0 = 1)



Read timing, (S1 = 1, S0 = 1)



Write timing, (S1 = 1, S0 = 1)

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## PHYSICAL DIMENSIONS



.050 - .090"  .020"  .040"

.029 +/- .005"

.019 +/- .005"

.050 +/- .005"

CJ - 44 pin J-lead ceramic package

.650 +/- .010"  .690 +/- .010"

.062-.088"
.100-.190"

.650 +/- .010"

.690 +/- .010"



.0.20" min

.018 +/- .003"

.050 +/- .005"

PJ - 44 pin J-lead plastic package

.655 +/- .005"  .690 +/- .005"

.175 +/- .010"

.655 +/- .005"

.690 +/- .005"
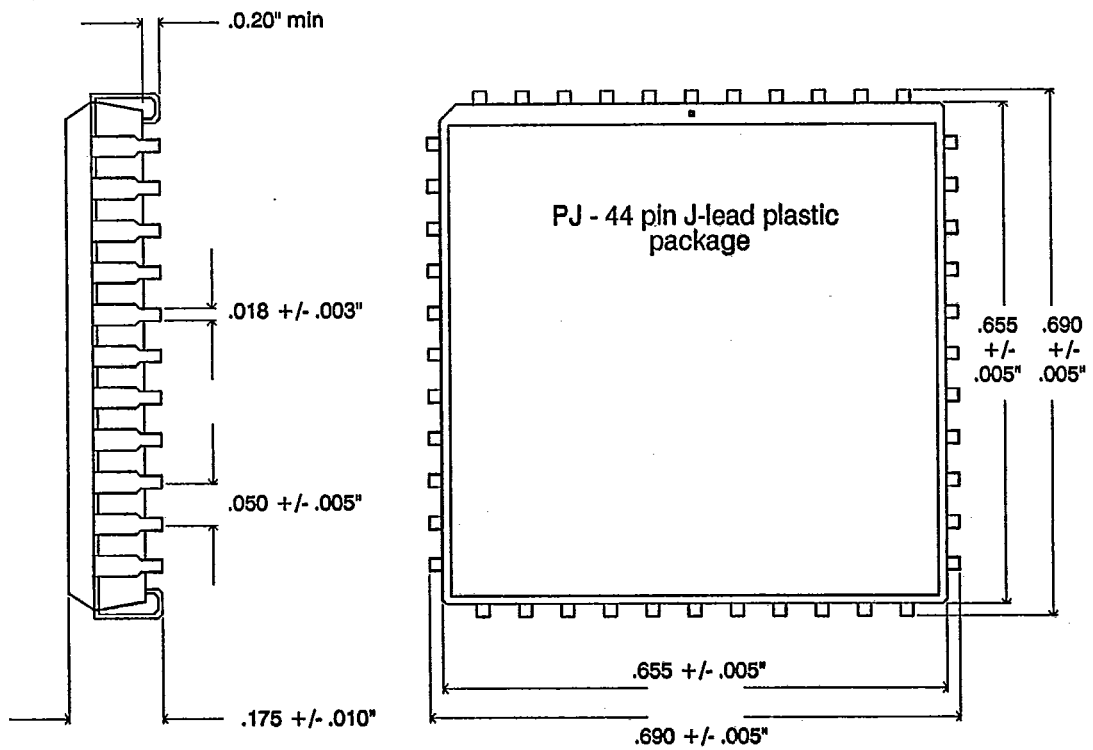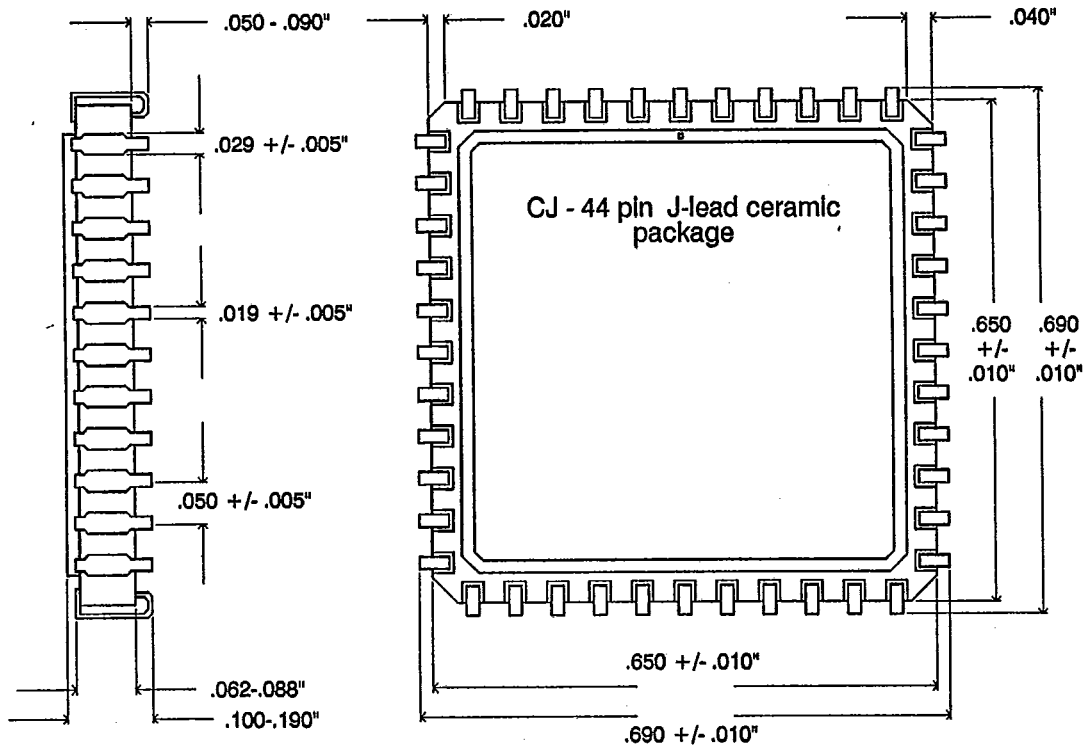
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# ORDERING INFORMATION

SRT products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

>           a. Device Number
>
>           b. Speed Option (if applicable)
>
>           c. Package Type
>
>           d. Temperature Range
>
>           e. Optional Processing

SRT-141A/1045        -6      CJ      M      883C

**e. OPTIONAL PROCESSING**

Blank = Standard processing
883C = MIL-STD-883(C), Class B compliant

**d. TEMPERATURE**

C = Commercial (0C to +70C)
I = Industrial (-40C to +85C)
M = Military (-55C to +125C)

**c. PACKAGE**

PJ = 44-pin plastic J-lead
CJ = 44-pin ceramic J-lead
Other packages available - contact SRT.

**b. SPEED OPTION**

-6 = 6MHz

**a. DEVICE NUMBER/DESCRIPTION**

SRT-141A/1045
FEC Encoder/Decoder