

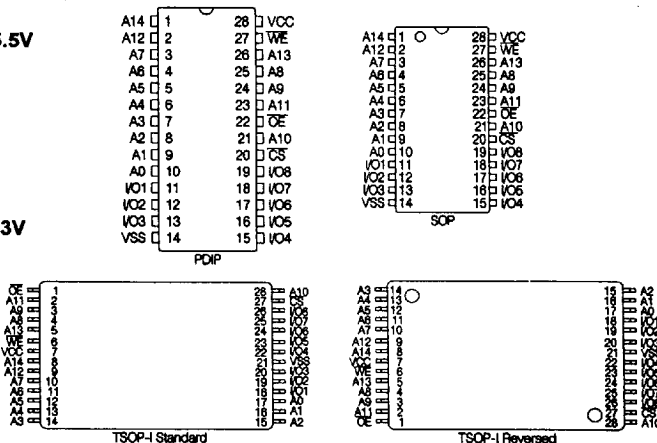
DESCRIPTION

The HY62V256 is a high-speed, low power and 32,768 x 8-bits CMOS static RAM fabricated using Hyundai's high performance twin tub CMOS process technology. The HY62V256 has a data retention mode that guarantees data to remain valid at a minimum power supply voltage of 2.0 volt. Using CMOS technology, supply voltages from 2.0 to 5.5 volt have little effect on supply current in data retention mode. The HY62V256 is suitable for use in low voltage (3.0V - 5.5V) operation and battery back-up applications.

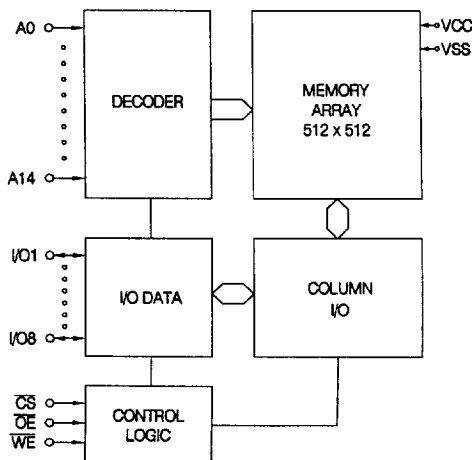
FEATURES

- Extended operating voltage : 3.0V - 5.5V
- High speed
 - 55/70/85/100ns at 5V
 - 100/120/150ns at 3.3V
- Low power consumption
 - Operating : 150mW (typ.) at 5V
 - 29.7mW (typ.) at 3.3V
 - Standby (CMOS) : 10 μ W (typ.) at 5V
 - 3.3 μ W (typ.) at 3.3V
- Battery backup
 - 2.0V (min.) data retention
- Fully static operation
 - No clock or refresh required
- TTL compatible inputs and outputs
- Tri-state output
- Standard pin configuration
 - 28 pin 600 mil PDIP
 - 28 pin 330 mil SOP
 - 28 pin 8x13.4 mm TSOP-I

PIN CONNECTION



BLOCK DIAGRAM



PIN DESCRIPTION

Pin Name	Pin Function
CS	Chip Select
WE	Write Enable
OE	Output Enable
A0-A14	Address Inputs
I/O1-I/O8	Data Input/Output
Vcc	Power(3.0V-5.5V)
Vss	Ground

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ABSOLUTE MAXIMUM RATINGS⁽¹⁾

SYMBOL	PARAMETER	RATING	UNIT
VCC, VIN, VOUT	Power Supply, Input/Output Voltage	-0.5 to 7.0	V
TA	Operating Temperature	0 to 70	°C
TBIAS	Temperature Under Bias	-10 to 125	°C
TSTG	Storage Temperature	-65 to 150	°C
PD	Power Dissipation	1.0	W
IOUT	Data Output Current	50	mA
TSDR	Lead Soldering Temperature & Time	260 • 10	°C • sec

Note:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is stress rating only and functional operation of the device at these or any other condition above those indicated in the operational of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(TA= 0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
VCC	Power Supply Voltage	3.0	3.3	5.5	V
VIH	Input High Voltage	2.2	-	VCC+0.5	V
VIL	Input Low Voltage	-0.5 ⁽¹⁾	-	0.4	V

Note:

1. VIL = -3.0V for pulse width less than 50ns

TRUTH TABLE

MODE	I/O OPERATION	CS	WE	OE
Standby	High-Z	H	X	X
Output Disabled	High-Z	L	H	H
Read	Data Out	L	H	L
Write	Data in	L	L	X

Note:

1. H=VIH, L=VIL, X=Don't Care

DC CHARACTERISTICS

(TA = 0°C to 70°C, unless otherwise specified.)

SYMBOL	PARAMETER	TEST CONDITIONS	POWER	MIN.	TYP.	MAX.	UNIT
ILI	Input Leakage Current	$V_{SS} \leq V_{IN} \leq V_{CC}$		-1	-	1	μA
ILO	Output Leakage Current	$V_{SS} \leq V_{OUT} \leq V_{CC}$, $\overline{CS} = V_{IH}$ or $OE = V_{IH}$ or $WE = V_{IL}$		-1	-	1	μA
ICC	Operating Power Supply Current	$\overline{CS} = V_{IL}$ $V_{IN} = V_{IH}$ or V_{IL} , $I_{IO} = 0mA$	5V	-	30	50	mA
			3.3V	-	9	25	mA
ICC1	Average Operating Current	$\overline{CS} = V_{IL}$, $I_{IO} = 0mA$ Min. Duty Cycle=100%	5V	-	40	70	mA
			3.3V	-	10	35	mA
ISB	TTL Standby Current (TTL Inputs)	$\overline{CS} = V_{IH}$	5V	-	0.4	2	mA
			3.3V	-	-	0.5	mA
ISB1	CMOS Standby Current (CMOS Inputs)	$CS \geq V_{CC} - 0.2V$	5V	-	2	25	μA
			3.3V	-	1	15	μA
VOL	Output Low Voltage	$I_{OL} = 2.1mA$		-	-	0.4	V
VOH	Output High Voltage	$I_{OH} = -1.0mA$	5V	2.4	-	-	V
			3.3V	2.2	-	-	V

NOTE:

1. Typical values are at TA=25°C

AC CHARACTERISTICS

(TA=0°C to 70°C, VCC=5V ±10%, unless otherwise noted.)

#	SYMBOL	PARAMETER	-55		-70		-85		-10		UNIT
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
READ CYCLE											
1	tRC	Read Cycle Time	55	-	70	-	85	-	100	-	ns
2	tAA	Address Access Time	-	55	-	70	-	85	-	100	ns
3	tACS	Chip Select Access Time	-	55	-	70	-	85	-	100	ns
4	tOE	Output Enable to Output Valid	-	30	-	35	-	45	-	50	ns
5	tCLZ	Chip Select to Low -Z Output	5	-	5	-	5	-	5	-	ns
6	tOLZ	Output Enable to Low-Z Output	5	-	5	-	5	-	5	-	ns
7	tCHZ	Chip Disable to High -Z Output	0	20	0	30	0	30	0	35	ns
8	tOHZ	Output Disable to High -Z Output	0	20	0	30	0	30	0	35	ns
9	tOH	Output Hold from Address Change	5	-	5	-	5	-	5	-	ns
WRITE CYCLE											
10	tWC	Write Cycle Time	55	-	70	-	85	-	100	-	ns
11	tCW	Chip Select to End of Write	50	-	65	-	75	-	80	-	ns
12	tAW	Address Valid to End of Write	50	-	65	-	75	-	80	-	ns
13	tAS	Address Set-up Time	0	-	0	-	0	-	0	-	ns
14	tWP	Write Pluse Width	40	-	50	-	60	-	70	-	ns
15	tWR	Write Recovery Time	0	-	0	-	0	-	0	-	ns
16	tWHZ	Write to High-Z Output	0	20	0	30	0	30	0	35	ns
17	tdW	Data to Write Time Overlap	25	-	35	-	40	-	40	-	ns
18	tdH	Data Hold from Write Time	0	-	0	-	0	-	0	-	ns
19	tOW	Output Active from End of Write	5	-	5	-	5	-	5	-	ns

AC CHARACTERISTICS

(TA=0°C to 70°C, VCC=3.3V ±10%, unless otherwise noted.)

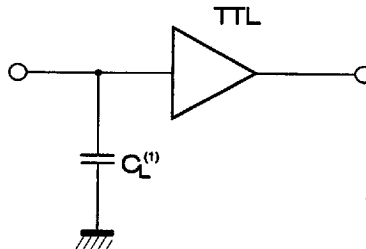
#	SYMBOL	PARAMETER	-10		-12		-15		UNIT
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
READ CYCLE									
1	t _{RC}	Read Cycle Time	100	-	120	-	150	-	ns
2	t _{AA}	Address Access Time	-	100	-	120	-	150	ns
3	t _{ACS}	Chip Select Access Time	-	100	-	120	-	150	ns
4	t _{OE}	Output Enable to Output Valid	-	50	-	55	-	75	ns
5	t _{CLZ}	Chip Select to Low -Z Output	10	-	10	-	10	-	ns
6	t _{OLZ}	Output Enable to Low-Z Output	10	-	10	-	10	-	ns
7	t _{CHZ}	Chip Disable to High -Z Output	0	35	0	40	0	50	ns
8	t _{OHZ}	Output Disable to High -Z Output	0	35	0	40	0	50	ns
9	t _{OH}	Output Hold from Address Change	10	-	20	-	20	-	ns
WRITE CYCLE									
10	t _{WC}	Write Cycle Time	100	-	120	-	150	-	ns
11	t _{CW}	Chip Select to End of Write	100	-	110	-	120	-	ns
12	t _{AW}	Address Valid to End of Write	100	-	110	-	120	-	ns
13	t _{AS}	Address Set-up Time	0	-	0	-	0	-	ns
14	t _{WP}	Write Pluse Width	60	-	70	-	100	-	ns
15	t _{WR}	Write Recovery Time	0	-	0	-	0	-	ns
16	t _{WHZ}	Write to High-Z Output	0	35	0	40	0	50	ns
17	t _{DW}	Data to Write Time Overlap	45	-	50	-	50	-	ns
18	t _{DH}	Data Hold from Write Time	0	-	0	-	0	-	ns
19	t _{OW}	Output Active from End of Write	20	-	20	-	20	-	ns

AC TEST CONDITIONS

(TA=0°C to 70°C, unless otherwise specified.)

PARAMETER	VOLTAGE	VALUE
Input Pulse Level	5V	0.8V to 2.4V
	3.3V	0.4V to 2.2V
Input Rise and Fall Time		5ns
Input and Output Timing Reference levels		1.5V
Output Load	100/120/150ns	CL=100pF + 1TTL Load

AC TEST LOADS



NOTE:

1. Including jig and scope capacitance.

CAPACITANCE

(TA=25°C, f= 1MHz)

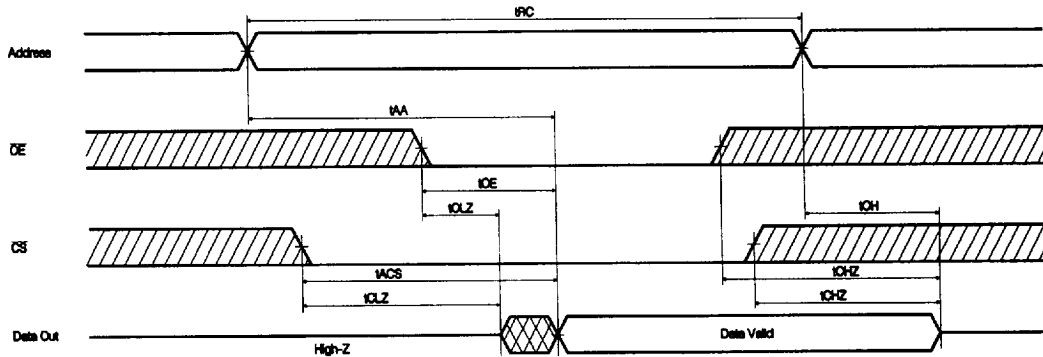
SYMBOL	PARAMETER	CONDITION	MAX.	UNIT
C _{IN}	Input Capacitance	V _{IN} =0V	6	pF
C _{IO}	Input/Output Capacitance	V _{IO} =0V	8	pF

Note:

1. This parameter is sampled and not 100% tested.

TIMING DIAGRAM

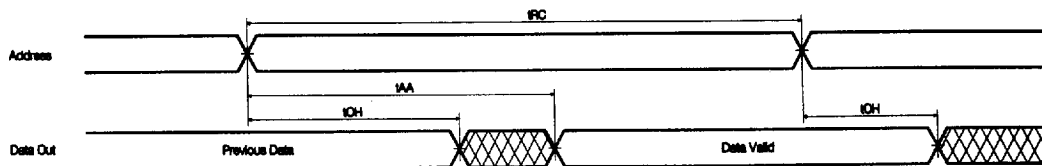
READ CYCLE 1



Note (READ CYCLE):

1. t_{CHZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, t_{CHZ} max. is less than t_{CLZ} min. both for a given device and from device to device.
3. $\overline{WE}$ is high for read cycle.

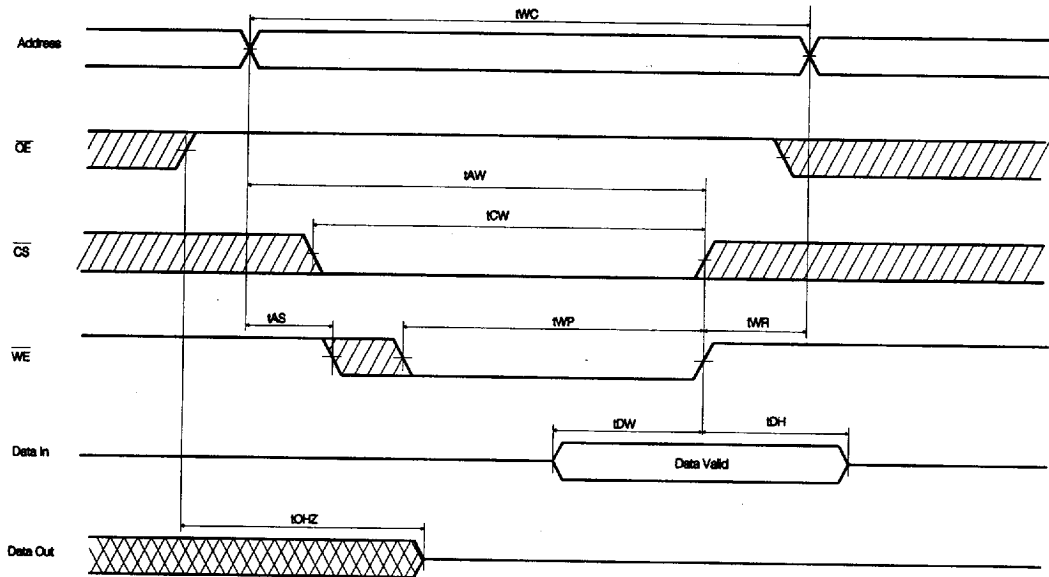
READ CYCLE 2



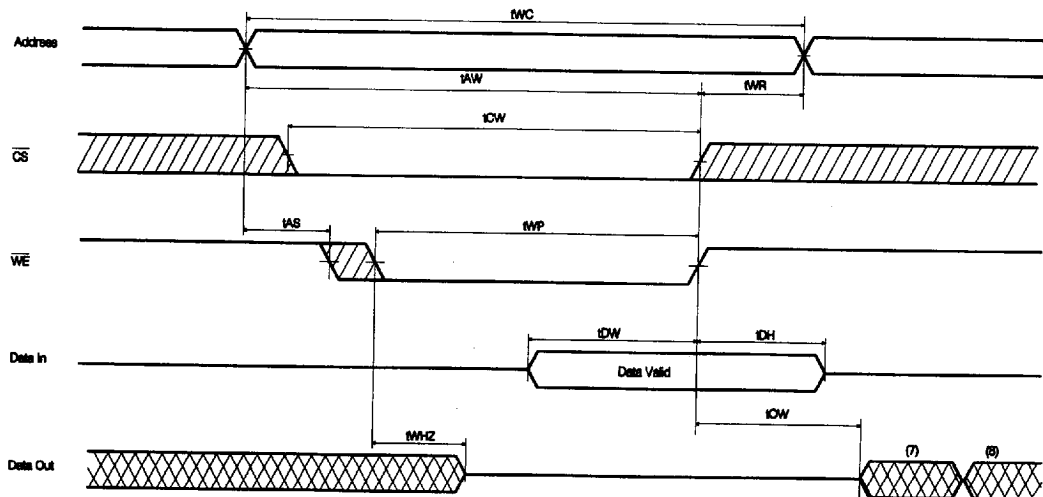
Note(READ CYCLE):

1. $\overline{WE}$ is high for read cycle.
2. Device is continuously selected $\overline{CS}=V_{IL}$.
3. $OE=V_{IL}$.

WRITE CYCLE 1 ($\overline{OE}$ Clocked)



WRITE CYCLE 2 ($\overline{OE}$ Low Fixed)



Note (WRITE CYCLE):

1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS}$ going low, and $\overline{WE}$ going low. A write ends at the earliest transition among $\overline{CS}$ going high $\overline{WE}$ going high. t_{wp} is measured from the beginning of write to the end of write.
2. t_{cw} is measured from the later of $\overline{CS}$ going low to end of write.
3. t_{as} is measured from the address valid to the beginning of write.
4. t_{wr} is measured from the end of write to the address change. t_{wr} applied in case a write ends as $\overline{CS}$, or $\overline{WE}$ going high.
5. If $\overline{OE}$ and $\overline{WE}$ are in the read mode during this period, the I/O pins are in the output low-Z state, inputs of opposite phase of the output must not be applied because bus contention can occur.
6. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high impedance state.
7. $DOUT$ is the same phase of latest written data in this write cycle.
8. $DOUT$ is the read data of the new address.

DATA RETENTION CHARACTERISTICS

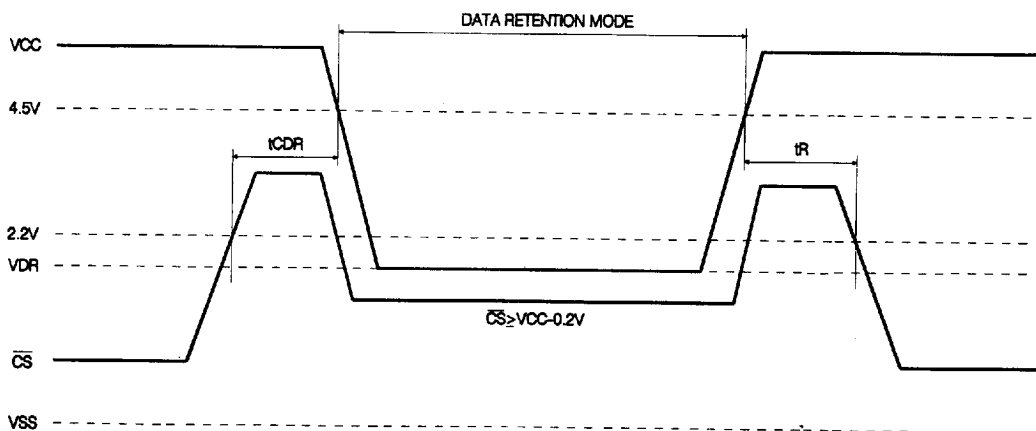
(TA=0°C to 70°C)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX	UNIT
VDR	Vcc for Data Retention	$\overline{CS} \geq V_{CC} - 0.2V, V_{SS} \leq V_{IN} \leq V_{CC}$	2.0	-	-	V
IccDR	Data Retention Current	VCC=3.0V $\overline{CS} \geq V_{CC} - 0.2V, V_{SS} \leq V_{IN} \leq V_{CC}$	-	1	15 ⁽²⁾	μA
tCDR	Chip Disable to Data Retention Time	See Data Retention Timing Diagram	0	-	-	ns
tR	Operating Recovery Time		tRC ⁽³⁾	-	-	ns

Notes :

1. Typical values are at the condition of TA=25°C.
2. 3μA max. at TA=0°C to 40°C
3. tRC is read cycle time.

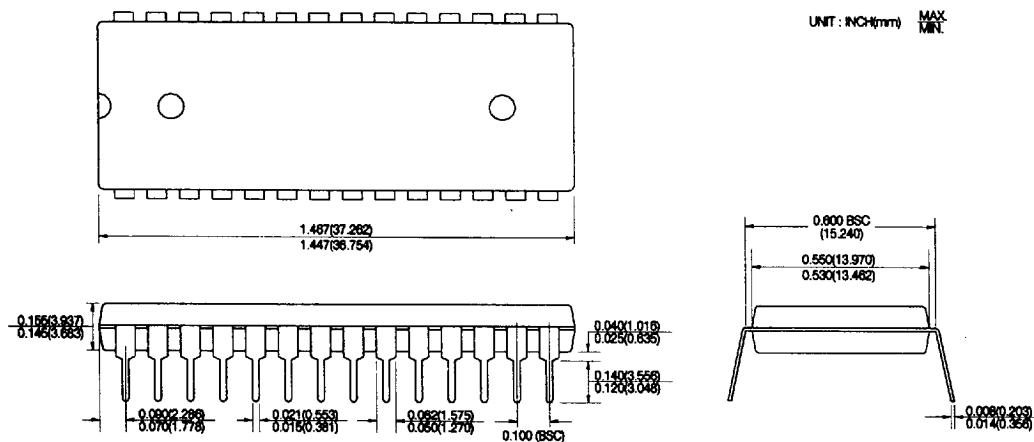
DATA RETENTION TIMING DIAGRAM 1



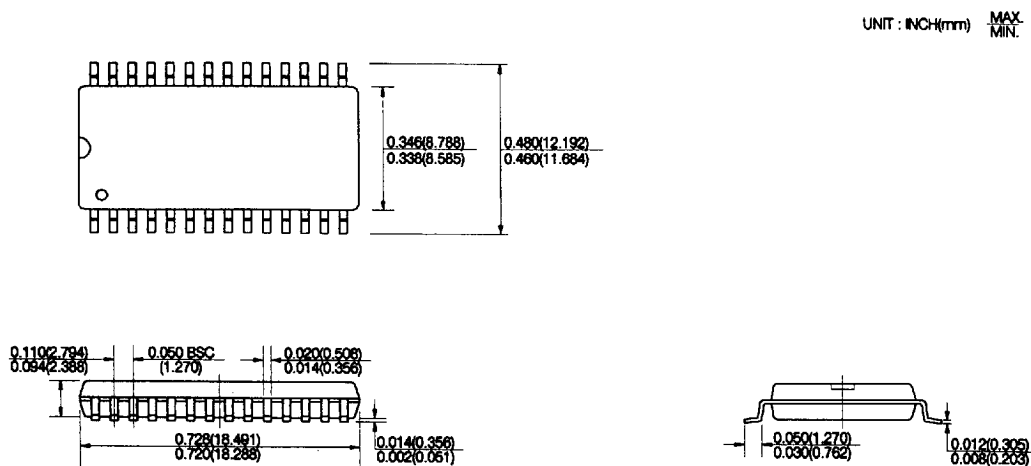
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PACKAGE INFORMATION

600 mil 28 pin Dual In-line Package(P)

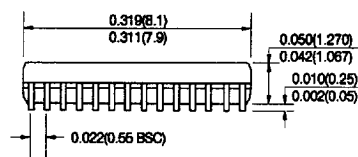
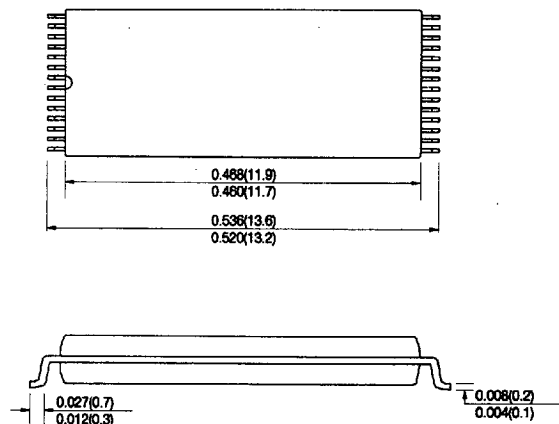


330mil 28 pin Small Outline Package (J)



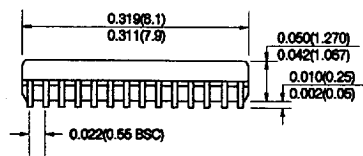
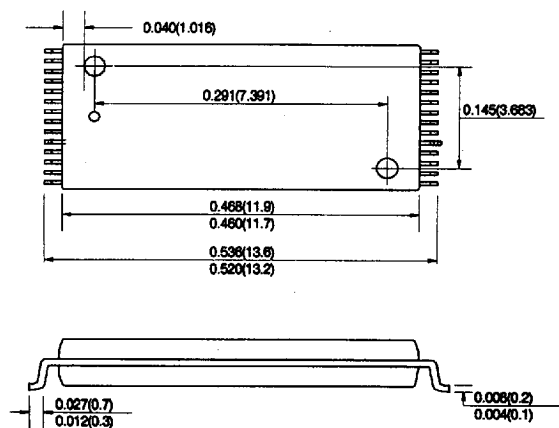
28 pin Plastic Thin Small Out Line Package(T1)

UNIT : INCH(mm) MAX
MIN



28 pin Thin Small Out Line Package(RI)

UNIT : INCH(mm) MAX
MIN



ORDERING INFORMATION

PART NO.	SPEED	POWER	PACKAGE
HY62V256LP	100/120/150	3.0V to 5.5V	PDIP
HY62V256LJ	100/120/150	3.0V to 5.5V	SOP
HY62V256LT1	100/120/150	3.0V to 5.5V	TSOP-I Standard
HY62V256LR1	100/120/150	3.0V to 5.5V	TSOP-I Reversed

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