

## DESCRIPTION

This family is a 4M bit dynamic RAM organized 1,048,576 x 4-bit configuration with Extended Data Out mode CMOS DRAMs. Extended data out mode is a kind of page mode which is useful for the read operation. The circuit and process design allow this device to achieve high performance and low power dissipation. Optional features are access time(50, 60 or 70ns) and package type(SOJ or TSOP-II) and power consumption (Normal or Low power with self refresh). Hyundai's advanced circuit design and process technology allow this device to achieve high bandwidth, low power consumption and high reliability.

## FEATURES

- Fast Page Mode operation
- Read-modify-write Capability
- TTL compatible inputs and outputs
- /CAS-before-/RAS, /RAS-only, Hidden and Self refresh capability
- Max. Active power dissipation
- JEDEC standard pinout
- 20/26-pin SOJ (300mil)  
20/26-pin TSOP-II (300mil)
- Single power supply of  $5V \pm 10\%$
- Early Write or output enable controlled write
- Fast access time and cycle time

| Speed | Power |
|-------|-------|
| 50    | 550mW |
| 60    | 495mW |
| 70    | 440mW |

| Speed | tRAC | tCAC | tPC  |
|-------|------|------|------|
| 50    | 50ns | 15ns | 35ns |
| 60    | 60ns | 15ns | 40ns |
| 70    | 70ns | 20ns | 45ns |

- Refresh cycle

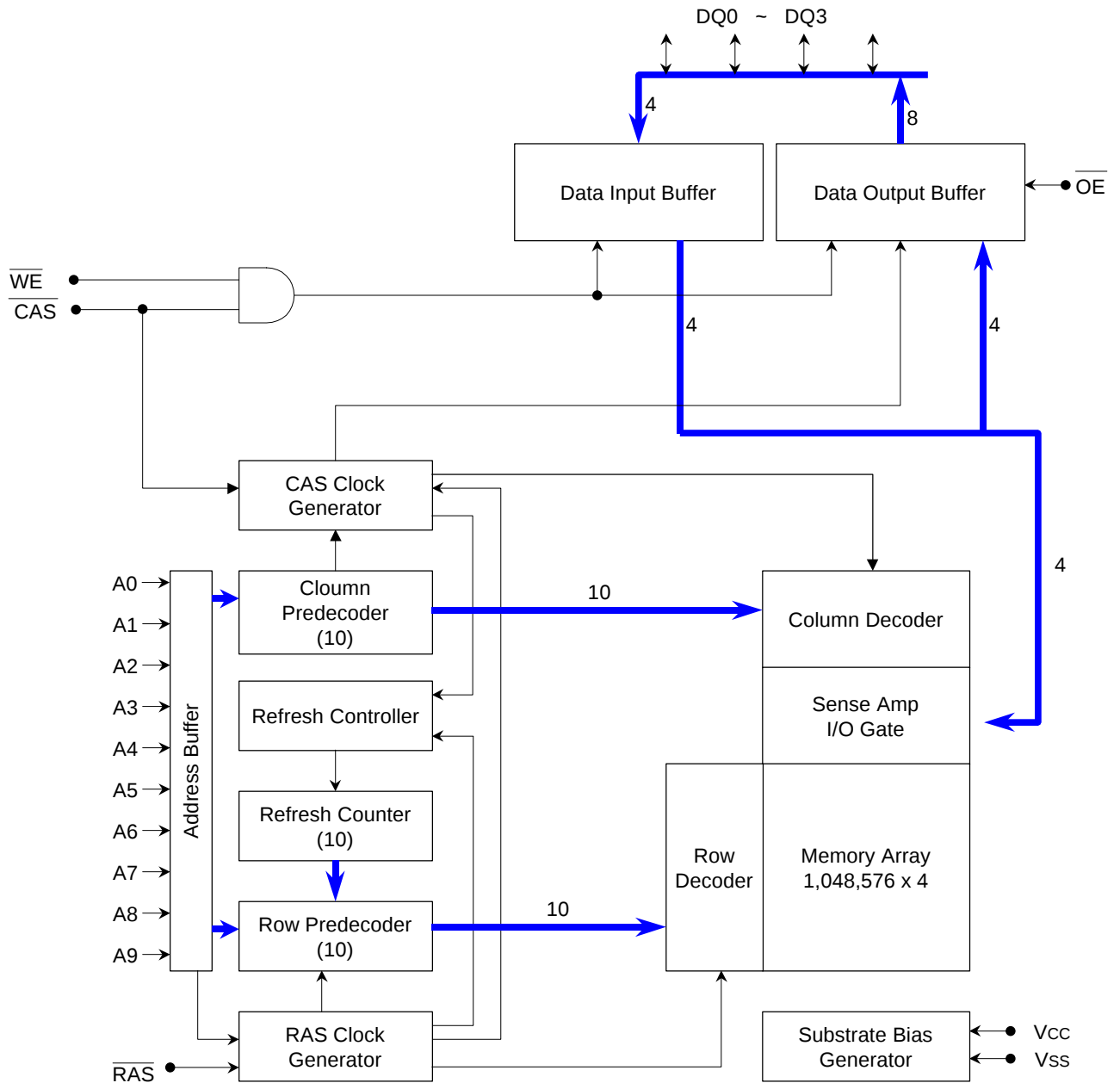
| Part number | Refresh | Normal | SL-part |
|-------------|---------|--------|---------|
| HY514400B   | 1K      | 16ms   | 128ms   |

## ORDERING INFORMATION

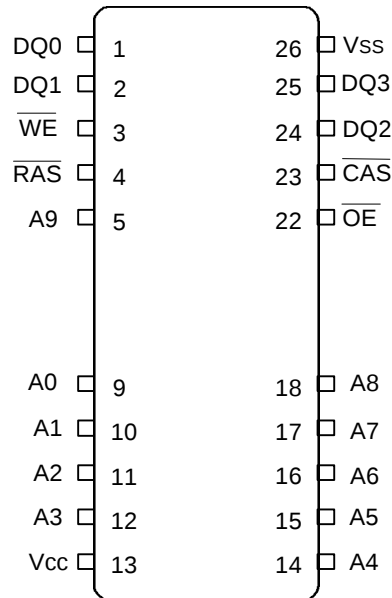
| Part Name    | Refresh | Power   | Package          |
|--------------|---------|---------|------------------|
| HY514400BJ   | 1K      |         | 20/26Pin SOJ     |
| HY514400BLJ  | 1K      | L-part  | 20/26Pin SOJ     |
| HY514400BSLJ | 1K      | SL-part | 20/26Pin SOJ     |
| HY514400BT   | 1K      |         | 20/26Pin TSOP-II |
| HY514400BLT  | 1K      | L-part  | 20/26Pin TSOP-II |
| HY514400BSLT | 1K      | SL-part | 20/26Pin TSOP-II |

\*SL : Low power with self refresh

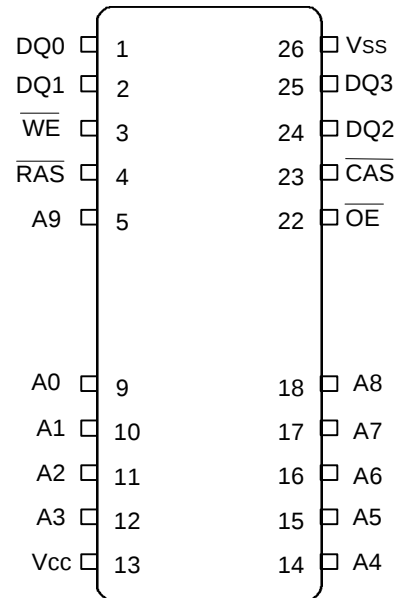
## FUNCTIONAL BLOCK DIAGRAM



### PIN CONFIGURATION (Marking Side)



20/26 Pin Plastic SOJ (300mil)



20/26 Pin Plastic TSOP- II (300mil)

### PIN DESCRIPTION

| Pin Name | Parameter             |
|----------|-----------------------|
| /RAS     | Row Address Strobe    |
| /CAS     | Column Address Strobe |
| /WE      | Write Enable          |
| /OE      | Output Enable         |
| A0~A9    | Address Input         |
| DQ0~DQ3  | Data In/Out           |
| Vcc      | Power (5V)            |
| Vss      | Ground                |

## ABSOLUTE MAXIMUM RATINGS

| Symbol                             | Parameter                                              | Rating      | Unit     |
|------------------------------------|--------------------------------------------------------|-------------|----------|
| T <sub>A</sub>                     | Ambient Temperature                                    | 0 to 70     | °C       |
| T <sub>STG</sub>                   | Storage Temperature                                    | -55 to 150  | °C       |
| V <sub>IN</sub> , V <sub>OUT</sub> | Voltage on Any Pin relative to V <sub>SS</sub>         | -1.0 to 7.0 | V        |
| V <sub>CC</sub>                    | Voltage on V <sub>CC</sub> relative to V <sub>SS</sub> | -1.0 to 7.0 | V        |
| I <sub>OS</sub>                    | Short Circuit Output Current                           | 50          | mA       |
| P <sub>D</sub>                     | Power Dissipation                                      | 0.9         | W        |
| T <sub>SOLDER</sub>                | Soldering Temperature • Time                           | 260 • 10    | °C • sec |

**Note** : Operation at or above Absolute Maximum Ratings can adversely affect device reliability

## RECOMMENDED DC OPERATING CONDITIONS

(T<sub>A</sub> = 0°C to 70°C)

| Symbol          | Parameter            | Min  | Typ | Max                  | UNIT |
|-----------------|----------------------|------|-----|----------------------|------|
| V <sub>CC</sub> | Power Supply Voltage | 4.5  | 5.0 | 5.5                  | V    |
| V <sub>IH</sub> | Input High Voltage   | 2.4  | -   | V <sub>CC</sub> +1.0 | V    |
| V <sub>IL</sub> | Input Low Voltage    | -1.0 | -   | 0.8                  | V    |

**Note** : All voltages are referenced to V<sub>SS</sub>.

## DC OPERATING CHARACTERISTICS

| Symbol          | Parameter                             | Test condition                                                                                               | Min | Max | Unit |
|-----------------|---------------------------------------|--------------------------------------------------------------------------------------------------------------|-----|-----|------|
| I <sub>LI</sub> | Input Leakage Current<br>(Any input)  | V <sub>SS</sub> ≤ V <sub>IN</sub> ≤ V <sub>CC</sub> + 1.0<br>All other pins not under test = V <sub>SS</sub> | -10 | 10  | μA   |
| I <sub>LO</sub> | Output Leakage Current<br>(Any input) | V <sub>SS</sub> ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub><br>/RAS & /CAS at V <sub>IH</sub>                       | -10 | 10  | μA   |
| V <sub>OL</sub> | Output Low Voltage                    | I <sub>OL</sub> = 4.2mA                                                                                      | -   | 0.4 | V    |
| V <sub>OH</sub> | Output High Voltage                   | I <sub>OH</sub> = -5.0mA                                                                                     | 2.4 | -   | V    |

## DC CHARACTERISTICS

(TA = 0°C to 70°C, VCC = 5V ± 10%, VSS = 0V, unless otherwise noted.)

| Symbol | Parameter                         | Test condition                                                                                                                     | Speed          | Max.            | Unit     |
|--------|-----------------------------------|------------------------------------------------------------------------------------------------------------------------------------|----------------|-----------------|----------|
| Icc1   | Operating Current                 | /RAS, /CAS Cycling<br>tRC = tRC(min)                                                                                               | 50<br>60<br>70 | 100<br>90<br>80 | mA       |
| Icc2   | TTL Standby Current               | /RAS, /CAS ≥ VIH(min)<br>Other inputs ≥ VSS                                                                                        |                | 2               | mA       |
| Icc3   | /RAS-only Refresh Current         | /RAS Cycling, /CAS = VIH<br>tRC = tRC(min)                                                                                         | 50<br>60<br>70 | 100<br>90<br>80 | mA       |
| Icc4   | Fast Page mode Current            | /CAS Cycling, /RAS = VIL<br>tHPC = tHPC(min)                                                                                       | 50<br>60<br>70 | 70<br>60<br>50  | mA       |
| Icc5   | CMOS Standby Current              | /RAS = /CAS ≥ VCC - 0.2V                                                                                                           | SL-part        | 1<br>200        | mA<br>μA |
| Icc6   | /CAS-before-/RAS Refresh Current  | /RAS & /CAS = 0.2V<br>tRC = tRC(min.)                                                                                              | 50<br>60<br>70 | 100<br>90<br>80 | mA       |
| Icc7   | Battery Back-up Current (SL-part) | tRC=125μs<br>/CAS = CBR cycling or 0.2V<br>/OE & /WE = VCC - 0.2V<br>Address = VCC-0.2V or 0.2V<br>DQ0~DQ3 = VCC-0.2, 0.2V or Open |                | 300             | μA       |
| Icc8   | Self Refresh Current (SL-part)    | /RAS & /CAS = 0.2V<br>Other pins are same as Icc7                                                                                  |                | 200             | μA       |

### Note

- Icc1, Icc3, Icc4 and Icc6 depend on output loading and cycle rates(tRC and tPC).
- Specified values are obtained with output unloaded.
- Icc is specified as an average current. In Icc1, Icc3, Icc6, address can be changed only once while /RAS=VIL. In Icc4, address can be changed maximum once while /CAS=VIH within one cycle time tPC.
- Only tRAS(max) = 1μs is applied to refresh of battery backup but tRAS(max) = 10μs is to applied to normal functional operation.
- Icc5(max.), Icc7 and Icc8 are applied to SL-part only.

## AC CHARACTERISTICS

(T<sub>A</sub> = 0 °C to 70 °C, V<sub>CC</sub> = 5V ± 10% , V<sub>SS</sub> = 0V, unless otherwise noted.)

| Symbol            | Parameter                                   | 50ns |      | 60ns |      | 70ns |      | Unit | Note   |
|-------------------|---------------------------------------------|------|------|------|------|------|------|------|--------|
|                   |                                             | Min  | Max  | Min  | Max  | Min  | Max  |      |        |
| t <sub>RC</sub>   | Random read or write cycle time             | 90   | -    | 110  | -    | 130  | -    | ns   |        |
| t <sub>RWC</sub>  | Read-modify-write cycle time                | 130  | -    | 155  | -    | 185  | -    | ns   |        |
| t <sub>PC</sub>   | Fast Page mode cycle time                   | 35   | -    | 40   | -    | 45   | -    | ns   |        |
| t <sub>PRWC</sub> | Fast Page mode read-modify-write cycle time | 75   | -    | 80   | -    | 95   | -    | ns   |        |
| t <sub>RAC</sub>  | Access time from /RAS                       | -    | 50   | -    | 60   | -    | 70   | ns   | 4,9,10 |
| t <sub>CAC</sub>  | Access time from /CAS                       | -    | 15   | -    | 15   | -    | 20   | ns   | 4,9    |
| t <sub>AA</sub>   | Access time from column address             | -    | 25   | -    | 30   | -    | 35   | ns   | 4,10   |
| t <sub>CPA</sub>  | Access time from /CAS precharge             | -    | 30   | -    | 35   | -    | 40   | ns   | 4,15   |
| t <sub>CLZ</sub>  | /CAS to output low impedance                | 0    | -    | 0    | -    | 0    | -    | ns   | 4      |
| t <sub>T</sub>    | Transition time(rise and fall)              | 3    | 50   | 3    | 50   | 3    | 50   | ns   | 3      |
| t <sub>RP</sub>   | /RAS precharge time                         | 30   | -    | 40   | -    | 50   | -    | ns   |        |
| t <sub>RAS</sub>  | /RAS pulse width                            | 50   | 10K  | 60   | 10K  | 70   | 10K  | ns   |        |
| t <sub>RASP</sub> | /RAS pulse width(FP mode)                   | 50   | 200K | 60   | 200K | 70   | 200K | ns   |        |
| t <sub>RSH</sub>  | /RAS hold time                              | 15   | -    | 15   | -    | 20   | -    | ns   |        |
| t <sub>CSH</sub>  | /CAS hold time                              | 50   | -    | 60   | -    | 70   | -    | ns   |        |
| t <sub>CAS</sub>  | /CAS pulse width                            | 15   | 10K  | 15   | 10K  | 20   | 10K  | ns   |        |
| t <sub>RCD</sub>  | /RAS to /CAS delay time                     | 15   | 35   | 20   | 45   | 20   | 50   | ns   | 9      |
| t <sub>RAD</sub>  | /RAS to column address delay time           | 10   | 25   | 15   | 30   | 15   | 35   | ns   | 10     |
| t <sub>CRP</sub>  | /CAS to /RAS precharge time                 | 5    | -    | 5    | -    | 5    | -    | ns   | 15     |
| t <sub>CP</sub>   | /CAS precharge time                         | 10   | -    | 10   | -    | 10   | -    | ns   | 17     |
| t <sub>ASR</sub>  | Row address set-up time                     | 0    | -    | 0    | -    | 0    | -    | ns   |        |
| t <sub>RAH</sub>  | Row address hold time                       | 8    | -    | 10   | -    | 10   | -    | ns   |        |
| t <sub>ASC</sub>  | Column address set-up time                  | 0    | -    | 0    | -    | 0    | -    | ns   | 14     |
| t <sub>CAH</sub>  | Column address hold time                    | 15   | -    | 15   | -    | 15   | -    | ns   | 14     |
| t <sub>AR</sub>   | Column address hold time from /CAS          | 40   | -    | 50   | -    | 55   | -    | ns   |        |
| t <sub>RAL</sub>  | Column address to /RAS lead time            | 25   | -    | 30   | -    | 35   | -    | ns   |        |
| t <sub>RCS</sub>  | Read command set-up time                    | 0    | -    | 0    | -    | 0    | -    | ns   | 14     |
| t <sub>RCH</sub>  | Read command hold time referenced to /CAS   | 0    | -    | 0    | -    | 0    | -    | ns   | 6,14   |
| t <sub>RRH</sub>  | Read command hold time referenced to /RAS   | 0    | -    | 0    | -    | 0    | -    | ns   | 6      |
| t <sub>WCH</sub>  | Write command hold time                     | 10   | -    | 10   | -    | 15   | -    | ns   | 14     |
| t <sub>WCR</sub>  | Write command hold time from /RAS           | 40   | -    | 45   | -    | 55   | -    | ns   |        |
| t <sub>WP</sub>   | Write command pulse width                   | 10   | -    | 10   | -    | 15   | -    | ns   |        |
| t <sub>RWL</sub>  | Write command to /RAS lead time             | 15   | -    | 15   | -    | 20   | -    | ns   |        |

## AC CHARACTERISTICS

Continued

| Symbol | Parameter                                  | 50ns |     | 60ns |     | 70ns |     | Unit | Note |
|--------|--------------------------------------------|------|-----|------|-----|------|-----|------|------|
|        |                                            | Min  | Max | Min  | Max | Min  | Max |      |      |
| tcWL   | Write command to /CAS lead time            | 15   | -   | 15   | -   | 20   | -   | ns   | 16   |
| tDS    | Data-in set-up time                        | 0    | -   | 0    | -   | 0    | -   | ns   | 7    |
| tDH    | Data-in hold time                          | 15   | -   | 15   | -   | 15   | -   | ns   | 7    |
| tDHR   | Data-in hold time Referenced to /RAS       | 40   | -   | 45   | -   | 55   | -   | ns   |      |
| tREF   | Refresh period(1024 cycles)                | 16   | -   | 16   | -   | 16   | -   | ms   | 12   |
|        | Refresh period(SL-part)                    | 128  | -   | 128  | -   | 128  | -   | ms   | 11   |
| twCS   | Write command set-up time                  | 0    | -   | 0    | -   | 0    | -   | ns   | 84   |
| tcWD   | /CAS to /WE delay time                     | 35   | -   | 40   | -   | 50   | -   | ns   | 8    |
| trWD   | /RAS to /WE delay time                     | 70   | -   | 85   | -   | 100  | -   | ns   | 8    |
| tAWD   | Column address to /WE delay time           | 45   | -   | 55   | -   | 65   | -   | ns   | 8    |
| tCSR   | /CAS set-up time(CBR cycle)                | 5    | -   | 5    | -   | 5    | -   | ns   | 14   |
| tCHR   | /CAS hold time(CBR cycle)                  | 10   | -   | 10   | -   | 10   | -   | ns   | 15   |
| trPC   | /RAS to /CAS precharge time                | 5    | -   | 5    | -   | 5    | -   | ns   | 14   |
| tcPT   | /CAS precharge time(CBR counter test)      | 20   | -   | 20   | -   | 25   | -   | ns   | 17   |
| tROH   | /RAS hold time referenced to /OE           | 10   | -   | 10   | -   | 10   | -   | ns   |      |
| toEA   | /OE access time                            | -    | 15  | -    | 15  | -    | 20  | ns   |      |
| toED   | /OE to data delay                          | 15   | -   | 15   | -   | 20   | -   | ns   |      |
| toEZ   | Output buffer turn-off delay time from /OE | 0    | 15  | 0    | 15  | 0    | 20  | ns   | 5    |
| toEH   | /OE command hold time                      | 15   | -   | 15   | -   | 20   | -   | ns   |      |
| tcPWD  | /WE delay time from /CAS precharge         | 50   | -   | 55   | -   | 65   | -   | ns   | 8    |
| trHCP  | /RAS hold time from /CAS precharge         | 30   | -   | 35   | -   | 40   | -   | ns   |      |
| trASS  | /RAS pulse width(self refresh)             | 100  | -   | 100  | -   | 100  | -   | ns   |      |
| trPS   | /RAS Precharge Time (Self refresh)         | 120  | -   | 130  | -   | 150  | -   | ns   |      |
| tCHS   | /CAS Hold Time (Self refresh)              | -50  | -   | -50  | -   | -50  | -   | ns   |      |
| tWRP   | /WE to /RAS Precharge time (CBR cycle)     | 10   | -   | 10   | -   | 10   | -   | ns   |      |
| tWRH   | /WE to /RAS Hold time (CBR cycle)          | 10   | -   | 10   | -   | 10   | -   | ns   |      |
| twTS   | Write Command Set-up time (Test Mode In)   | 10   | -   | 10   | -   | 10   | -   | ns   |      |
| twTH   | Write Command Hole time (test Mode In)     | 10   | -   | 10   | -   | 10   | -   | ns   |      |

### NOTE

1. An initial pause of 200 $\mu$ s is required after power-up followed by 8 /RAS only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 CBR refresh cycles instead of 8 /RAS-only refresh cycles are required.
2. If /RAS=Vss during power-up, the HY514400B could begin an active cycle. This condition results in higher current than necessary current which is demanded from the power supply during power-up. It is recommended that /RAS and /CAS track with Vcc during power-up or be held at a valid VIH in other to minimize the power-up current.
3. VIH(min.) and VIL(max.) are reference levels for measuring timing of input signals. Transition times are measured between VIH(min.) and VIL(max.), and are assumed to be 5ns for all inputs.
4. Measured at VOH=2.0V and VOL=0.8V with a load equivalent to 2TTL loads and 100pF.
5. tOFF(max.) and tOEZ define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. Either tRCH or tRRH must be satisfied for a read cycle.
7. tCEZ and tOEZ define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
8. twCS, trWD, tcWD, tAWD and tcpWD are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If twCS  $\geq$  twCS(min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle. If trWD  $\geq$  trWD(min.), tcWD  $\geq$  tcWD(min.), tAWD  $\geq$  tAWD(min), and tcpWD  $\geq$  tcpWD(min.), the cycle is a read-modify-write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
9. Operation within the trCD(max.) limit ensures that trAC(max.) can be met. trCD(max.) is specified as a reference point only. If trCD is greater than the specified trCD(max.) limit, then access time is controlled by tCAC.
10. Operation within the tRAD(max.) limit ensures that trAC(max.) can be met. tRAD(max.) is specified as a reference point only. If tRAD is greater than the specified tRAD(max.) limit, then access time is controlled by tAA.
11. tREF(max.)=128ms is applied to SL-parts only.
12. A burst of 1024 CBR refresh cycles must be executed within 16ms (128ms for SL-part) after exiting self refresh.
13. When CAS goes low at the same time, 4bits data are written into the device.
14. These parameters are determined by the earlier falling edge of /CAS.
15. These parameters are determined by the later rising edge of /CAS.
16. tCWL must be satisfied by /CAS for 4bits access cycle.
17. tCP and tCPT are measured when /CAS and is high state.

### CAPACITANCE

(TA = 25°C, VCC = 5V  $\pm$  10%, VSS = 0V and f=1MHz, unless otherwise noted.)

| Symbol | Parameter                                 | Typ. | Max | Unit |
|--------|-------------------------------------------|------|-----|------|
| CIN1   | Input Capacitance (A0~A9)                 | -    | 5   | pF   |
| CIN2   | Input Capacitance (/RAS, /CAS, /WE, /OE)  | -    | 7   | pF   |
| CDQ    | Data Input / Output Capacitance (DQ0~DQ3) | -    | 7   | pF   |