CY62128

128K x 8 Static RAM

Features

- **4.5V – 5.5V operation**
- **CMOS for optimum speed/power**
- **Low active power (70 ns, LL version)**
  - **— 330 mW (max.) (60 mA)**
- **Low standby power (70 ns, LL version)**
  - **— 110 μW (max.) (20 μA)**
- **Automatic power-down when deselected**
- **TTL-compatible inputs and outputs**
- **Easy memory expansion with $\overline{CE}_1$, CE_2, and $\overline{OE}$ options**

Functional Description

The CY62128 is a high-performance CMOS static RAM organized as 131,072 words by 8 bits. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}_1$), an active HIGH chip enable (CE_2), an active LOW output enable ($\overline{OE}$), and three-state drivers. This device has an automatic power-down feature that reduces power consumption by more than 75% when deselected.

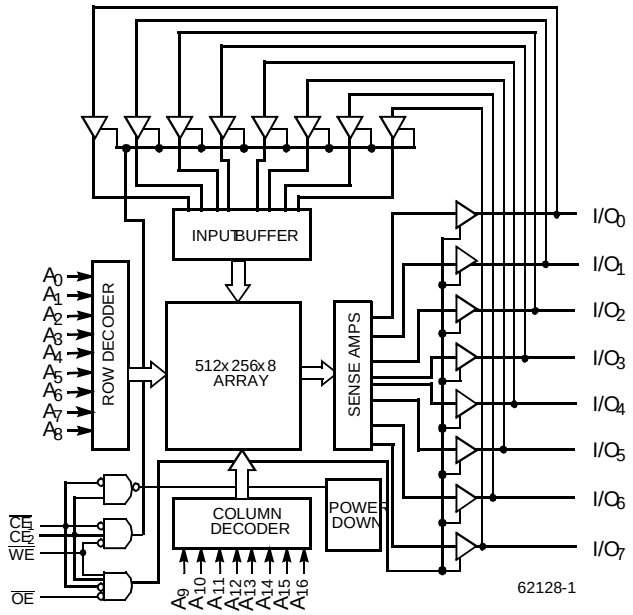
Writing to the device is accomplished by taking chip enable one ($\overline{CE}_1$) and write enable ($\overline{WE}$) inputs LOW and chip enable two (CE_2) input HIGH. Data on the eight I/O pins (I/O_0 through I/O_7) is then written into the location specified on the address pins (A_0 through A_{16}).

Reading from the device is accomplished by taking chip enable one ($\overline{CE}_1$) and output enable ($\overline{OE}$) LOW while forcing write enable ($\overline{WE}$) and chip enable two (CE_2) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input/output pins (I/O_0 through I/O_7) are placed in a high-impedance state when the device is deselected ($\overline{CE}_1$ HIGH or CE_2 LOW), the outputs are disabled ($\overline{OE}$ HIGH), or during a write operation ($\overline{CE}_1$ LOW, CE_2 HIGH, and $\overline{WE}$ LOW).

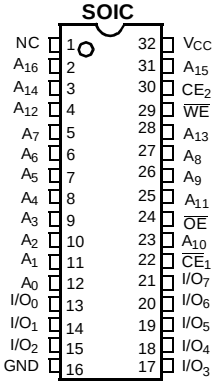
The CY62128 is available in a standard 450-mil-wide SOIC, 32-pin TSOP type I and STSOP packages.

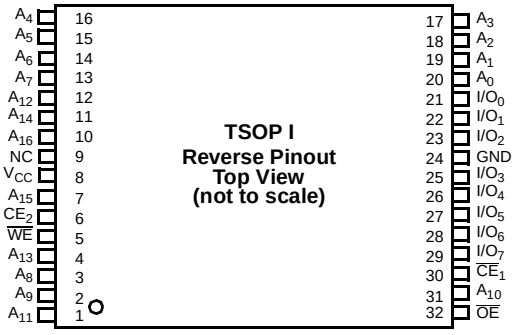
Logic Block Diagram

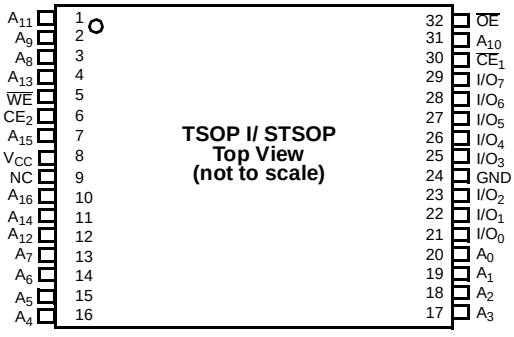


Pin Configurations

Top View
SOIC







62128-2 62128-2

Selection Guide

			CY62128-55	CY62128-70
Maximum Access Time (ns)			55	70
Maximum Operating Current	Commercial	L	50	40
		LL	50	40
Maximum CMOS Standby Current	Commercial	L	80	80
		LL	15	15

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage on V_{CC} to Relative GND[1] .... –0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State[1] ..... –0.5V to V_{CC} + 0.5V

DC Input Voltage[1] ..... –0.5V to V_{CC} + 0.5V

Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current..... >200 mA

Operating Range

Range	Ambient Temperature[2]	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	–40°C to +85°C	5V ± 10%

Notes:

1. V_{IL} (min.) = –2.0V for pulse durations of less than 20 ns.
2. T_A is the "instant on" case temperature.

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions			62128–55			62128–70			Unit
					Min.	Typ[3]	Max.	Min.	Typ[3]	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –1.0 mA			2.4			2.4			V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 2.1mA					0.4			0.4	V
V_{IH}	Input HIGH Voltage				2.2		V_{CC} + 0.3	2.2		V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage[1]				–0.3		0.8	–0.3		0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}			–1		+1	–1		+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled			+1		+1	+1		+1	µA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND					–300			–300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$	Com'l			40	115		40	110	mA
				L		30	70		30	60	mA
				LL		30	70		30	60	mA
			Ind.'l			40	115		40	110	mA
				L		30	70		30	70	mA
				LL		30	70		30	70	mA
I_{SB1}	Automatic CE Power-Down Current —TTL Inputs	Max. V_{CC}, $\overline{CE}_1 \geq V_{IH}$ or $CE_2 \leq V_{IL}$, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, f = f_{MAX}	Com'l			0.3	25		0.3	1	mA
				L		0.15	3		0.15	1	mA
				LL		0.1	2		0.1	1	mA
			Ind.'l			0.3	25		0.3	1	mA
				L		0.15	3		0.15	1	mA
				LL		0.1	2		0.1	1	mA
I_{SB2}	Automatic CE Power-Down Current —CMOS Inputs	Max. V_{CC}, $\overline{CE}_1 \geq V_{CC}$ – 0.3V, or $CE_2 \leq$ 0.3V, $V_{IN} \geq V_{CC}$ – 0.3V, or $V_{IN} \leq$ 0.3V, f=0	Com'l			0.4	500		0.4	500	µA
				L			100			100	µA
				LL			20			20	µA
			Ind			0.4	500		0.4	500	µA
				L			100			100	µA
				LL			40			40	µA

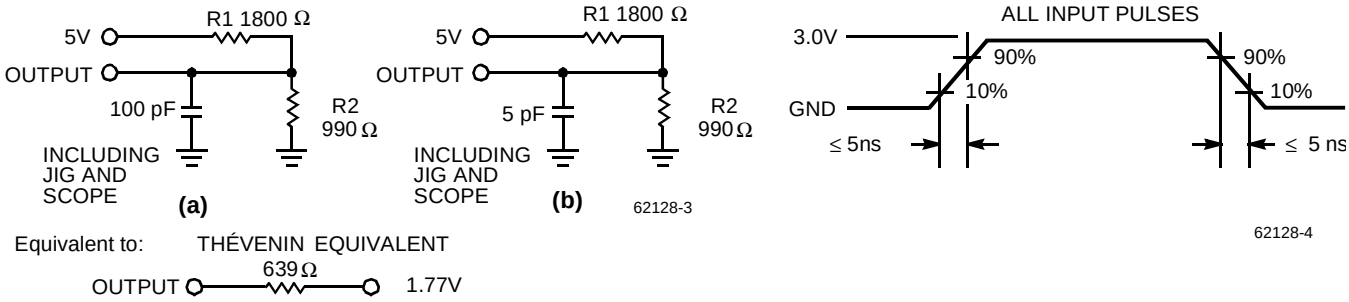
Capacitance[5]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	9	pF
C_{OUT}	Output Capacitance		9	pF

Notes:

3. Typical values are included for reference only and are not tested or guaranteed. Typical values are an average of the distribution across normal production variations as measured at V_{CC} = 5.0V, T_A = 25°C, and t_{AA}=70ns
4. Not more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
5. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



Switching Characteristics[6] Over the Operating Range

Parameter	Description	62128–55		62128–70		Unit
		Min.	Max.	Min.	Max.	
READ CYCLE						
t_{RC}	Read Cycle Time	55		70		ns
t_{AA}	Address to Data Valid		55		70	ns
t_{OHA}	Data Hold from Address Change	5		5		ns
t_{ACE}	$\overline{CE}_1$ LOW to Data Valid, CE_2 HIGH to Data Valid		55		70	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		20		35	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[7,8]		20		25	ns
t_{LZCE}	$\overline{CE}_1$ LOW to Low Z, CE_2 HIGH to Low Z[8]	5		5		ns
t_{HZCE}	$\overline{CE}_1$ HIGH to High Z, CE_2 LOW to High Z[7,8]		20		25	ns
t_{PU}	$\overline{CE}_1$ LOW to Power-Up, CE_2 HIGH to Power-Up	0		0		ns
t_{PD}	$\overline{CE}_1$ HIGH to Power-Down, CE_2 LOW to Power-Down		55		70	ns
WRITE CYCLE[9]						
t_{WC}	Write Cycle Time	55		70		ns
t_{SCE}	$\overline{CE}_1$ LOW to Write End, CE_2 HIGH to Write End	45		60		ns
t_{AW}	Address Set-Up to Write End	45		60		ns
t_{HA}	Address Hold from Write End	0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	45		50		ns
t_{SD}	Data Set-Up to Write End	25		30		ns
t_{HD}	Data Hold from Write End	0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[8]	5		5		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[7, 8]		20		25	ns

Notes:

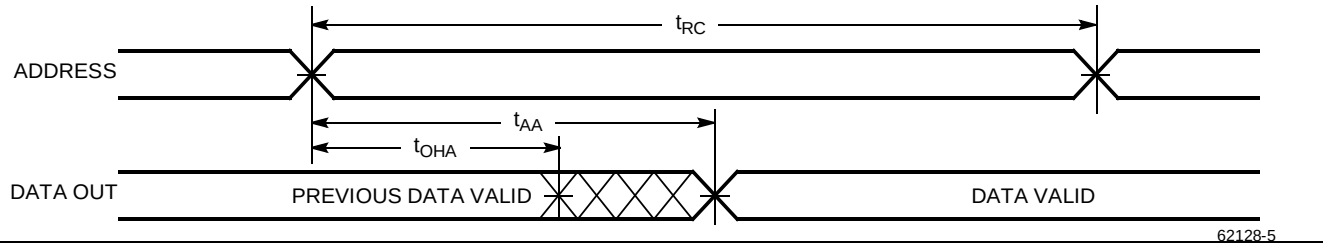
6. Test conditions assume signal transition time of 5ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 100pF load capacitance.
7. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
8. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
9. The internal write time of the memory is defined by the overlap of $\overline{CE}_1$ LOW, CE_2 HIGH, and $\overline{WE}$ LOW. $\overline{CE}_1$ and $\overline{WE}$ must be LOW and CE_2 HIGH to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.

Data Retention Characteristics (Over the Operating Range for "L" and "LL" version only)

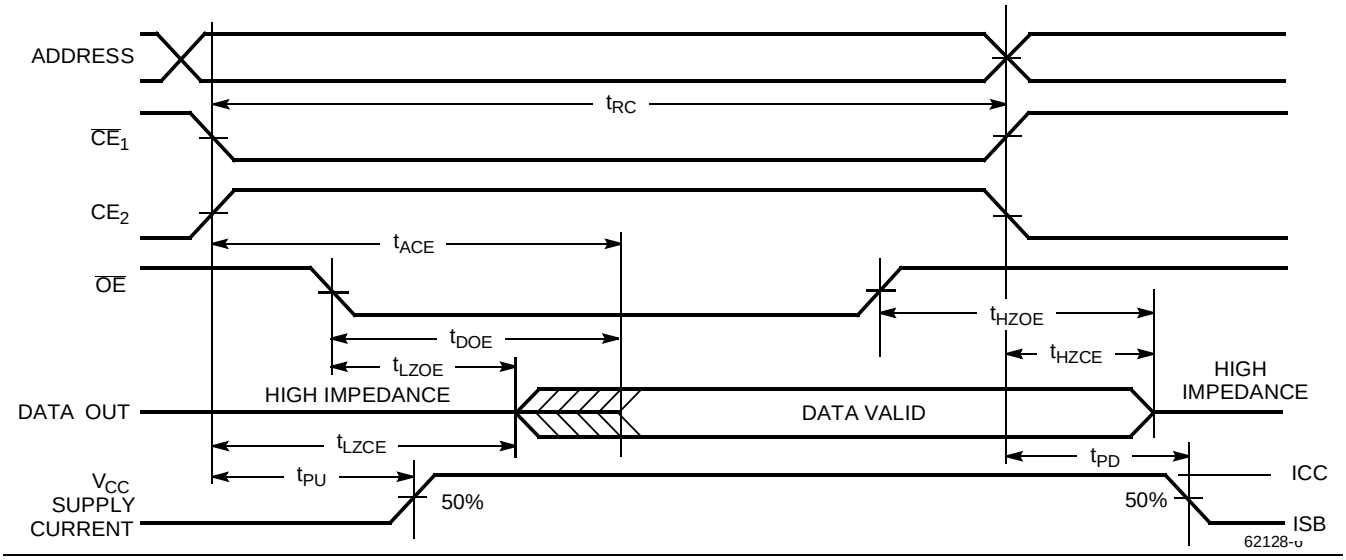
Parameter	Description			Conditions[10]	Min.	Typ.	Max.	Unit
V_{DR}	VCC for Data Retention				2.0			V
I_{CCDR}	Data Retention Current	Coml.	L	V_{CC}=V_{DR}=3.0V, $\overline{CE} \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$ or, $V_{IN} \leq 0.3V$		0.4	100	µA
			LL				20	µA
		Indl.	L				100	µA
			LL				20	µA
t_{CDR}[3]	Chip Deselect to Data Retention Time				0			ns
t_R[3]	Operation Recovery Time				t_{RC}			ns

Switching Waveforms

Read Cycle No.1[11,12]



Read Cycle No. 2 ($\overline{OE}$ Controlled)[12,13]

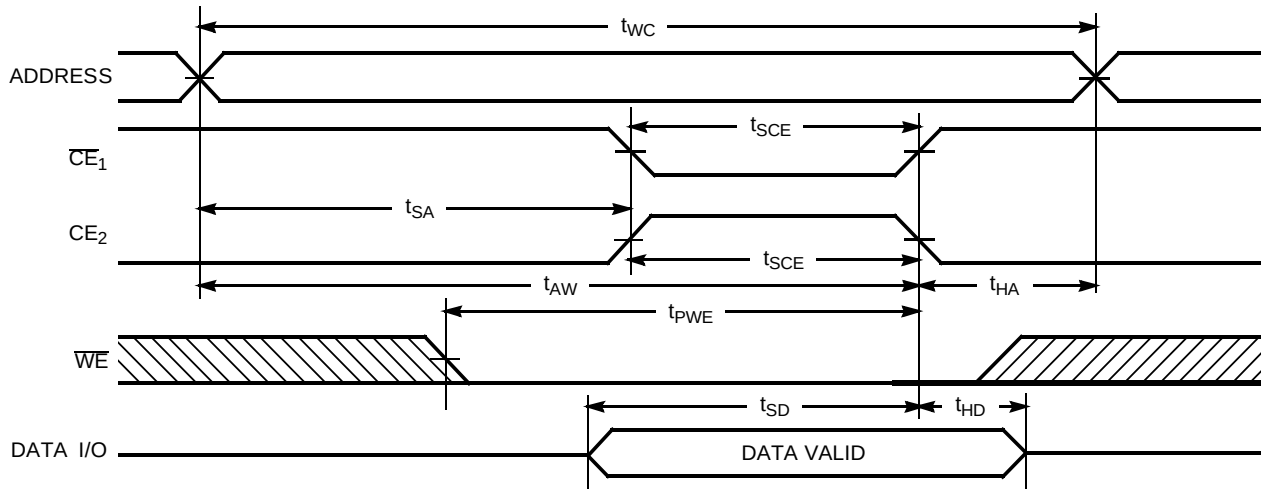


Notes:

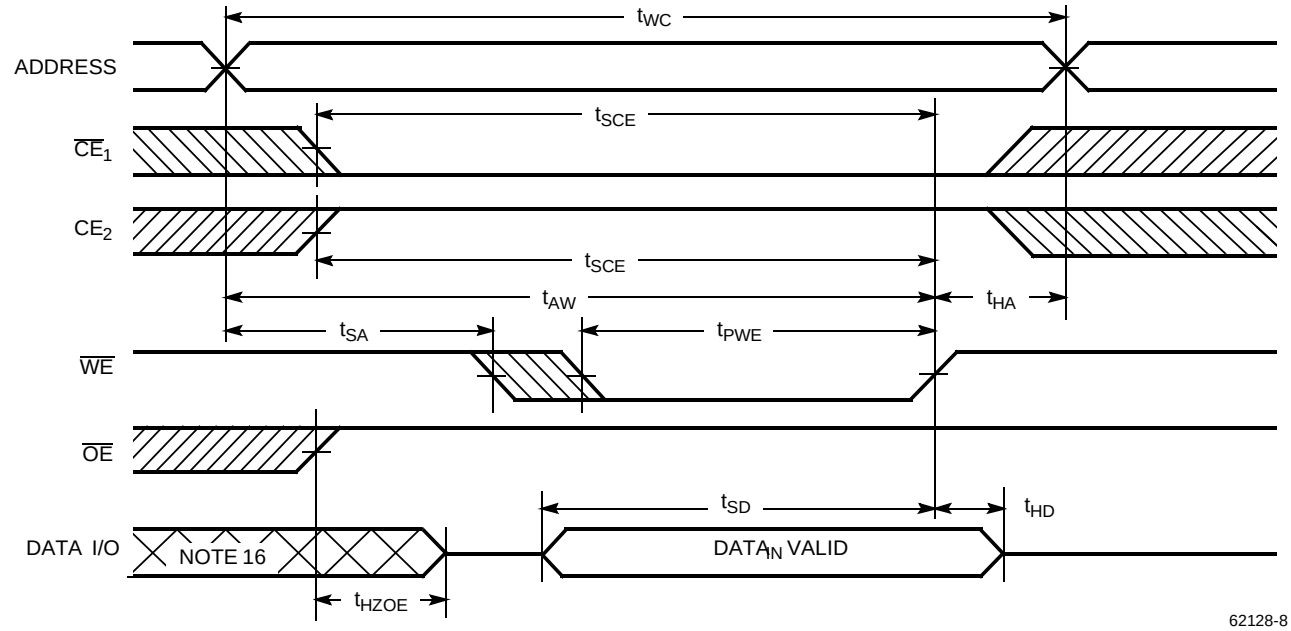
10. No input may exceed V_{CC} + 0.5V.
11. Device is continuously selected. $\overline{OE}$, $\overline{CE}_1$ = V_{IL}, CE_2 = V_{IH}.
12. $\overline{WE}$ is HIGH for read cycle.
13. Address valid prior to or coincident with $\overline{CE}_1$ transition LOW and CE_2 transition HIGH.

Switching Waveforms (continued)

Write Cycle No. 1 ($\overline{CE_1}$ or CE_2 Controlled)[14,15]



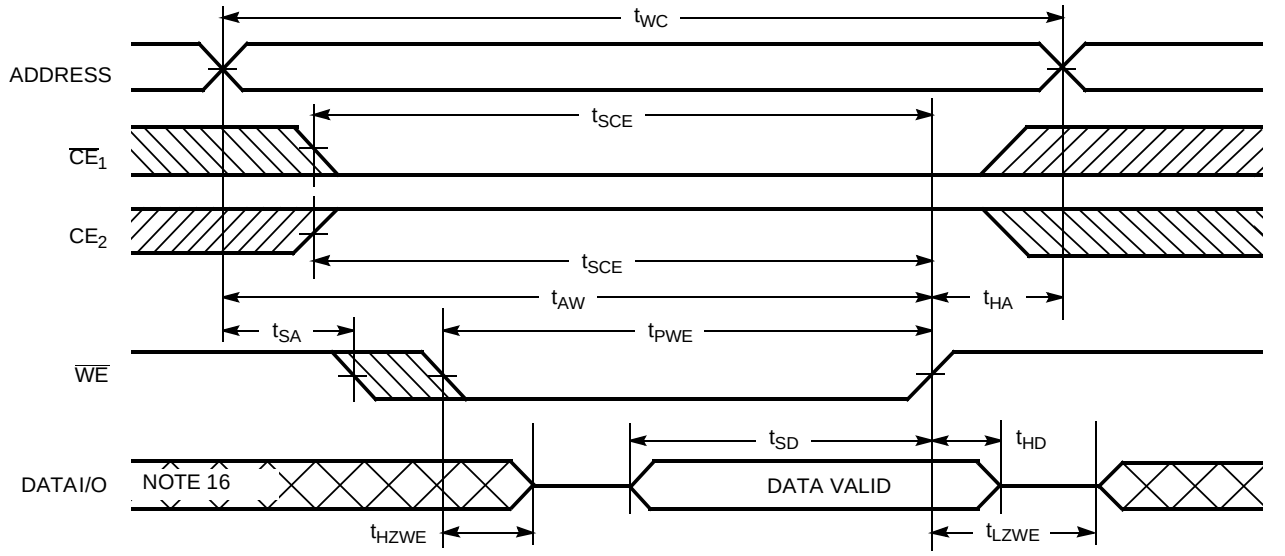
Write Cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ HIGH During Write)[14,15]



Notes:
14. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
15. If $\overline{CE_1}$ goes HIGH or CE_2 goes LOW simultaneously with $\overline{WE}$ going HIGH, the output remains in a high-impedance state.
16. During this period the I/Os are in the output state and input signals should not be applied.

Switching Waveforms (continued)

Write Cycle No.3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)[14,15]



Truth Table

$\overline{CE_1}$	CE_2	$\overline{OE}$	$\overline{WE}$	$I/O_0 - I/O_7$	Mode	Power
H	X	X	X	High Z	Power-Down	Standby (I_{SB})
X	L	X	X	High Z	Power-Down	Standby (I_{SB})
L	H	L	H	Data Out	Read	Active (I_{CC})
L	H	X	L	Data In	Write	Active (I_{CC})
L	H	H	H	High Z	Selected, Outputs Disabled	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
55	CY62128–55SC	S34	32-Lead 450-Mil SOIC	Commercial
	CY62128-55ZC	Z32	32-Lead TSOP Type I	
	CY62128–55ZAC	ZA32	32-Lead STSOP Type I	
70	CY62128–70SC	S34	32-Lead 450-Mil SOIC	Commercial
	CY62128–70ZC	Z32	32-Lead TSOP Type I	
	CY62128-70ZAC	ZA32	32-Lead STSOP Type I	
	CY62128-70ZRC	ZR32	32-Lead Reverse TSOP Type I	
	CY62128–70SI	S34	32-Lead 450-Mil SOIC	Industrial
	CY62128–70ZI	Z32	32-Lead TSOP Type I	
	CY62128-70ZAI	ZA32	32-Lead STSOP Type I	
	CY62128-70ZRI	ZR32	32-Lead Reverse TSOP Type I	
	CY62128L–70SC	S34	32-Lead 450-Mil SOIC	Commercial
	CY62128L–70ZC	Z32	32-Lead TSOP Type I	
	CY62128L-70ZAC	ZA32	32-Lead STSOP Type I	
	CY62128L-70ZRC	ZR32	32-Lead Reverse TSOP Type I	
	CY62128L–70SI	S34	32-Lead 450-Mil SOIC	Industrial
	CY62128L–70ZI	Z32	32-Lead TSOP Type I	
	CY62128L-70ZAI	ZA32	32-Lead STSOP Type I	
	CY62128L-70ZRI	ZR32	32-Lead Reverse TSOP Type I	
	CY62128LL–70SC	S34	32-Lead 450-Mil SOIC	Commercial
	CY62128LL–70ZC	Z32	32-Lead TSOP Type I	
	CY62128LL-70ZAC	ZA32	32-Lead STSOP Type I	
	CY62128LL-70ZRC	ZR32	32-Lead Reverse TSOP Type I	
	CY62128LL–70SI	Z32	32-Lead 450-Mil Type I	Industrial
	CY62128LL-70ZI	Z32	32-Lead TSOP Type I	
	CY62128LL-70ZAI	Z32	32-Lead STSOP Type I	
	CY62128LL-70ZRI	ZR32	32-Lead Reverse TSOP Type I	

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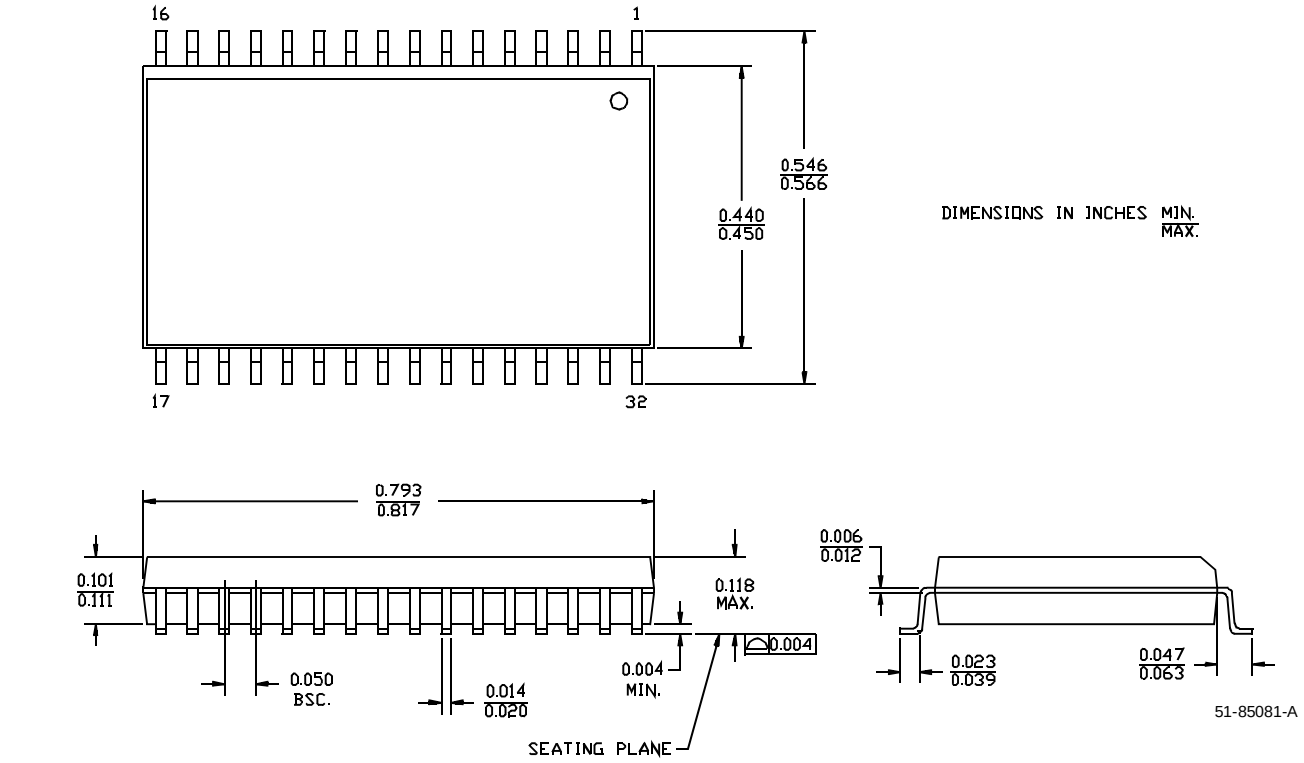
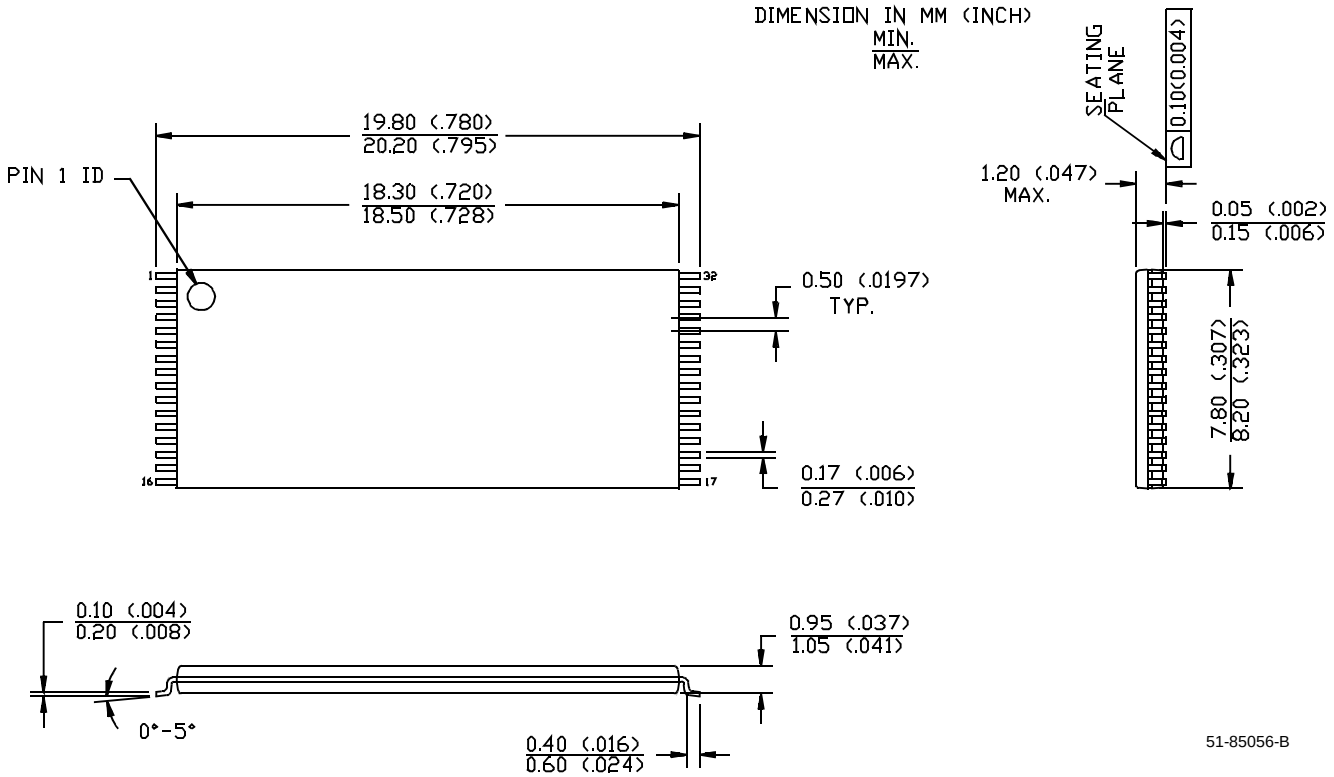
Package Diagrams

32-Lead (450 MIL) Molded SOIC S34

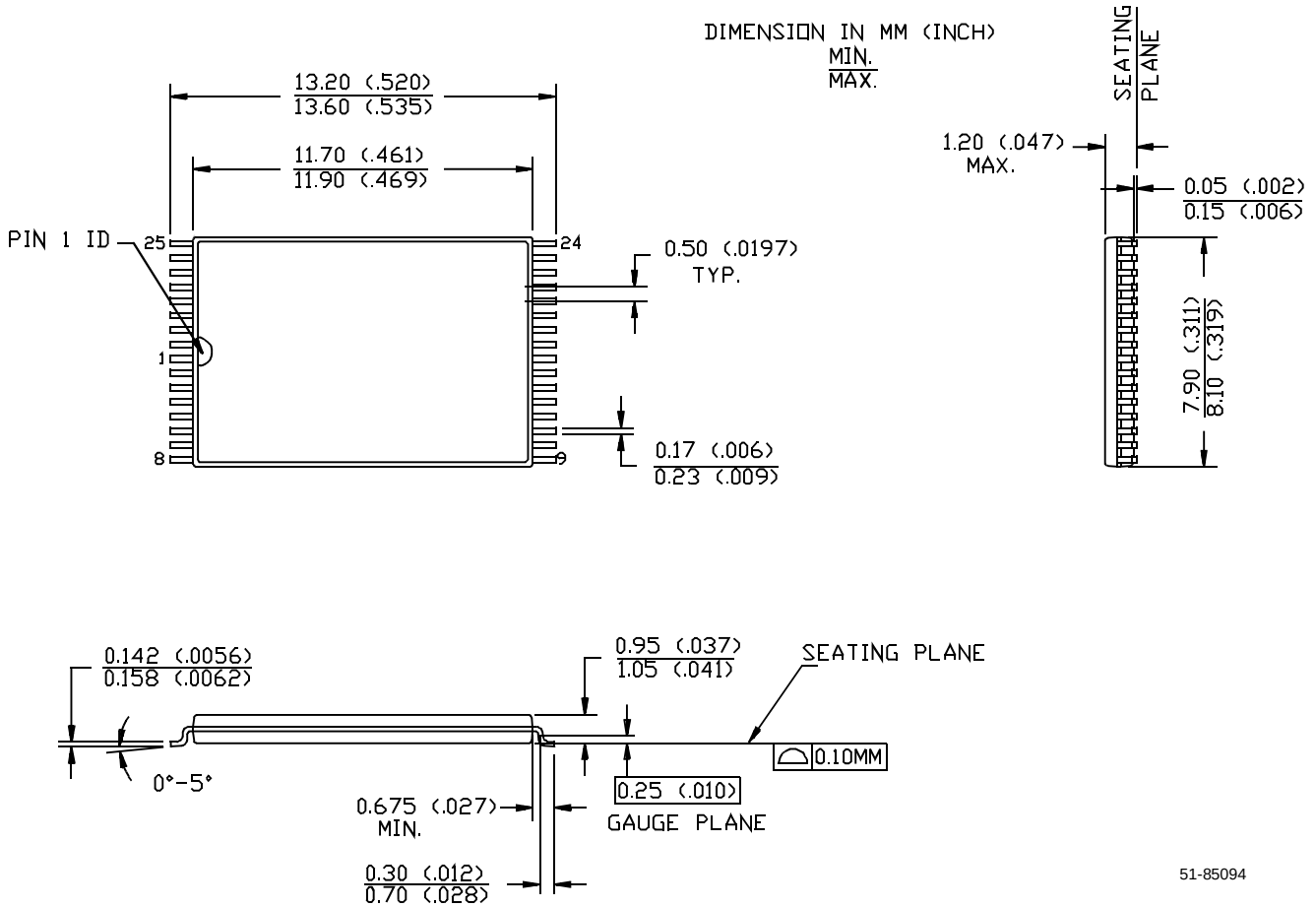


32-Lead Thin Small Outline Package Z32



Package Diagrams (continued)

32-Lead Shrunk Thin Small Outline Package ZA32



32-Lead Reverse Thin Small Outline Package ZR32