PRELIMINARY

CY2274A

Pentium Pro™ and Pentium II™ Clock Synthesizer/Driver for the 82440FX Chipset

Features

- **Mixed 2.5V and 3.3V operation**
- **Complete clock solution to meet requirements of Pentium Pro™ and Pentium II™ motherboards including dual-processor designs**
  - **— Four CPU clocks at 2.5V**
  - **— Eight 3.3V synchronous PCI clocks**
  - **— Two 3.3V USB clocks at 48 MHz**
  - **— One 3.3V IO clock at 24 MHz**
  - **— One 2.5V IOAPIC clock at 14.318 MHz**
  - **— Three 3.3V Ref. clocks at 14.318 MHz**
- **1 ns–4 ns CPU-PCI delay, factory-EPROM programmable**
- **Factory-EPROM programmable output drive and slew rate for optimal EMI control. Improved output drivers are designed for low EMI.**
- **Factory-EPROM programmable CPU, PCI, and USB/IO clock frequencies for custom configurations**
- **Individual Powerdown, CPU stop, and PCI stop pins for power management**
- **Low CPU clock jitter ≤ 250 ps cycle-cycle.**
- **Low skew outputs**
- **Intel Test Mode support**
- **Available in space-saving 48-pin SSOP package**

Functional Description

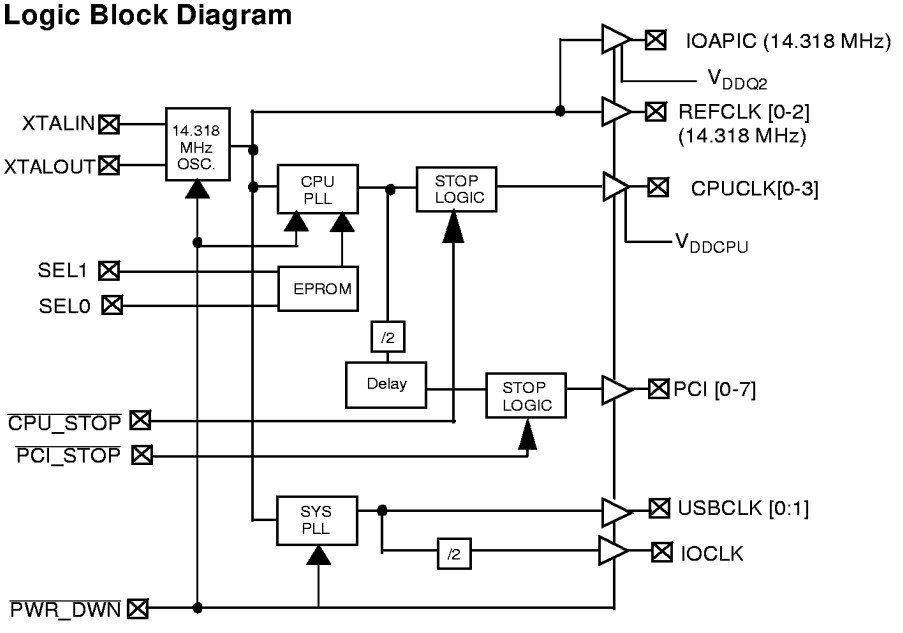
The CY2274A is a Clock Synthesizer/Driver chip for a Pentium Pro, or Pentium II-based PC using the 82440FX or other similar core-logic chipsets.

The CY2274A outputs four CPU clocks at 2.5V. There are eight PCI clocks, running at one half the CPU clock frequency. Additionally, the part outputs two 3.3V USB clocks at 48 MHz, one 3.3V IO clock at 24 MHz, one 2.5V IOAPIC clock at 14.318 MHz, and three 3.3V reference clocks at 14.318 MHz. All output clocks meet Intel's drive strength, rise/fall time, jitter, accuracy, and skew requirements. The CPU, PCI, USB, and IO clock frequencies are factory-EPROM programmable for easy customization with fast turnaround times.

The part possesses dedicated powerdown, CPU stop, and PCI stop pins for power management control. These inputs are synchronized on-chip, and ensure glitch-free output transitions. When the $\overline{\text{CPU\_STOP}}$ input is asserted, the CPU clock outputs are driven LOW. When the $\overline{\text{PCI\_STOP}}$ input is asserted, the PCI clock outputs are driven LOW. Finally, when the $\overline{\text{PWR\_DWN}}$ pin is asserted, the reference oscillator and the PLLs are shut down, and all outputs are driven LOW.

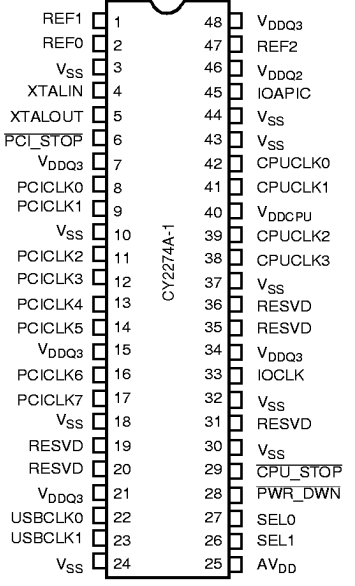
The CY2274A clock outputs are designed for low EMI emissions. Controlled rise and fall times, unique output driver circuits, and innovative circuit layout techniques enable the CY2274A to have lower EMI than clock devices from other manufacturers. Additionally, factory-EPROM programmable output drive and slew-rate control enable optimal configurations for EMI control.

Logic Block Diagram



Pin Configuration

SSOP
Top View



Pin Summary

Name	Pins	Description
V_{DDQ3}	7, 15, 21, 34, 48	3.3V Digital voltage supply
V_{DDQ2}	46	IOAPIC Digital voltage supply, 2.5V
V_{DDCPU}	40	CPU Digital voltage supply, 2.5V
AV_{DD}	25	Analog voltage supply, 3.3V
V_{SS}	3, 10, 18, 24, 30, 32, 37, 43, 44	Ground
XTALIN[1]	4	Reference crystal input
XTALOUT[1]	5	Reference crystal feedback
$\overline{\text{PCI\_STOP}}$	6	Control input to disable PCI clocks, active low
$\overline{\text{PWR\_DWN}}$	28	Control input to put device in power down state, active low
$\overline{\text{CPU\_STOP}}$	29	Control input to disable CPU clocks, active low
SEL1	26	CPU frequency select input, bit 1 (See function table below)
SEL0	27	CPU frequency select input, bit 0 (See function table below)
CPUCLK [0:3]	42, 41, 39, 38	CPU clock outputs
PCICLK [0:7]	8, 9, 11, 12, 13, 14, 16, 17	PCI clock outputs
IOAPIC	45	IOAPIC clock output
REF [0:2]	1, 2, 47	Reference clock outputs, 14.318 MHz. REF0 drives 45 pF load
USBCLK [0:1]	22, 23	USB clock outputs (48 MHz)
IOCLK	33	IO clock outputs (24 MHz)
RESVD	19, 20, 31, 35, 36	Reserved pins, connect to V_{SS}

Function Table, Factory-EPROM Programmable

SEL1	SEL0	XTALIN	CPUCLK [0:3]	PCICLK [0:7]	REF [0:2] IOAPIC	USBCLK	IOCLK
0	0	14.318 MHz	High-Z	High-Z	High-Z	High-Z	High-Z
0	1	14.318 MHz	60.0 MHz	30.0 MHz	14.318 MHz	48.0 MHz	24.0 MHz
1	0	14.318 MHz	66.67 MHz	33.33 MHz	14.318 MHz	48.0 MHz	24.0 MHz
1	1	TCLK[2]	TCLK/2	TCLK/4	TCLK	TCLK/2	TCLK/4

Actual Clock Frequency Values

Clock Output	Target Frequency (MHz)	Actual Frequency (MHz)	PPM
CPUCLK	66.67	66.654	–195
CPUCLK	60.0	60.0	0
USBCLK[3]	48.0	48.008	167
IOCLK	24.0	24.004	167

Notes:
1. For best accuracy, use a parallel-resonant crystal, C_{LOAD} = 18 pF.
2. TCLK is a Test Clock driven in on the XTALIN input in Test Mode.
3. Meets Intel USB clock requirements.

CPU and PCI Clock Driver Strengths

- Matched impedances on both rising and falling edges on the output drivers
- Output impedance: 25Ω (typical) measured at 1.5V.

Power Management Logic

$\overline{\text{CPU\_STOP}}$	$\overline{\text{PCI\_STOP}}$	$\overline{\text{PWR\_DWN}}$	CPUCLK	PCICLK	Other Clocks	Osc.	PLLs
X	X	0	Low	Low	Stopped	Off	Off
0	0	1	Low	Low	Running	Running	Running
0	1	1	Low	33/30 MHz	Running	Running	Running
1	0	1	66/60 MHz	Low	Running	Running	Running
1	1	1	66/60 MHz	33/30 MHz	Running	Running	Running

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage ..... –0.5 to +7.0V

Input Voltage ..... –0.5V to V_{DD}+0.5

Storage Temperature (Non-Condensing) ... –65°C to +150°C

Max. Soldering Temperature (10 sec) ..... +260°C

Junction Temperature ..... +150°C

Package Power Dissipation 1W

Static Discharge Voltage ..... >2000V (per MIL-STD-883, Method 3015)

Operating Conditions[4]

Parameter	Description	Min.	Max.	Unit
AV_{DD}, V_{DDQ3}	Analog and Digital Supply Voltage	3.135	3.465	V
V_{DDCPU}	CPU Supply Voltage	2.375	2.9	V
V_{DDQ2}	IOAPIC Supply Voltage	2.375	2.9	V
T_A	Operating Temperature, Ambient	0	70	°C
C_L	Max. Capacitive Load on CPUCLK, USBCLK, IOCLK, REF1, REF2, IOAPIC PCICLK REF0	 10 30 20	 20 30 45	pF
$f_{(REF)}$	Reference Frequency, Oscillator Nominal Value	14.318	14.318	MHz

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions			Min.	Max.	Unit
V_{IH}	High-level Input Voltage	Except Crystal Inputs			2.0		V
V_{IL}	Low-level Input Voltage	Except Crystal Inputs				0.8	V
V_{OH}	High-level Output Voltage	V_{DDCPU}, V_{DDQ2} = 2.375V	I_{OH} = 16 mA	CPUCLK	2.0		V
			I_{OH} = 18 mA	IOAPIC			
V_{OL}	Low-level Output Voltage	V_{DDCPU}, V_{DDQ2} = 2.375V	I_{OL} = 27 mA	CPUCLK		0.4	V
			I_{OL} = 29 mA	IOAPIC			
V_{OH}	High-level Output Voltage	V_{DDQ3}, AV_{DD} = 3.135V	I_{OH} = 32 mA	PCICLK	2.4		V
			I_{OH} = 26 mA	USBCLK			
			I_{OH} = 26 mA	IOCLK			
			I_{OH} = 36 mA	REF0			
			I_{OH} = 26 mA	REF[1:2]			
V_{OL}	Low-level Output Voltage	V_{DDQ3}, AV_{DD} = 3.135V	I_{OL} = 26 mA	PCICLK		0.4	V
			I_{OL} = 21 mA	USBCLK			
			I_{OL} = 21 mA	IOCLK			
			I_{OL} = 29 mA	REF0			
			I_{OL} = 21 mA	REF[1:2]			
I_{IH}	Input High Current	$V_{IH} = V_{DD}$			–5	+5	µA
I_{IL}	Input Low Current	V_{IL} = 0V				5	µA
I_{OZ}	Output Leakage Current	Three-state			–10	+10	µA
I_{DD}	Power Supply Current[5]	V_{DD} = 3.465V, V_{IN} = 0 or V_{DD}, Loaded Outputs, CPU clocks = 66.67 MHz				250	mA
I_{DD}	Power Supply Current[5]	V_{DD} = 3.465V, V_{IN} = 0 or V_{DD}, Unloaded Outputs				100	mA
I_{DDS}	Power-down Current	Current draw in power-down state				50	µA

Notes:

4. Electrical parameters are guaranteed with these operating conditions.
5. Power supply current will vary with number of outputs which are running. Therefore, power supply current can be calculated with the following formula: TBD

Switching Characteristics[6]

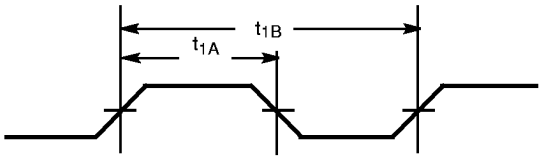
Parameter	Output	Description	Test Conditions	Min.	Typ.	Max.	Unit
t_1	All	Output Duty Cycle[7]	$t_1 = t_{1A} \div t_{1B}$	45	50	55	%
t_2	CPUCLK, IOAPIC	CPU and IOAPIC Clock Rising and Falling Edge Rate	Between 0.4V and 2.0V, V_{DDCPU} = 2.5V	1.0		4.0	V/ns
t_2	PCICLK, USBCLK, IOCLK, REF0	PCI, USB, I/O, REF0 Clock Rising and Falling Edge Rate	Between 0.4V and 2.4V	1.0		4.0	V/ns
t_2	REF1 REF2	REF [1:2] Rising and Falling Edge Rate	Between 0.4V and 2.4V	0.5		2.0	V/ns
t_3	CPUCLK	CPU Clock Rise Time	Between 0.4V and 2.0V, V_{DDCPU} = 2.5V	0.4		1.6	ns
t_3	USBCLK, IOCLK	USB Clock and I/O Clock Rise Time	Between 0.4V and 2.4V			2.0	ns
t_4	CPUCLK	CPU Clock Fall Time	Between 2.0V and 0.4V, V_{DDCPU} = 2.5V	0.4		1.6	ns
t_4	USBCLK, IOCLK	USB Clock and I/O Clock Fall Time	Between 2.4V and 0.4V			2.0	ns
t_5	CPUCLK	CPU-CPU Clock Skew	Measured at 1.25V, V_{DDCPU} = 2.5V		100	250	ps
t_6	CPUCLK, PCICLK	CPU-PCI Clock Skew	Measured at 1.25V for 2.5V clocks, and at 1.5V for 3.3V clocks	1.0	2.0	4.0	ns
t_7	CPUCLK	Cycle-Cycle Clock Jitter	Measured at 1.25V for 2.5V clocks			250	ps
t_8	USBCLK, IOCLK, PCICLK	Cycle-Cycle Clock Jitter	Measured at 1.5V			500	ps
t_9	CPUCLK, PCICLK,	Power-up Time	CPU, PCI clock stabilization from power-up			3	ms

Notes:

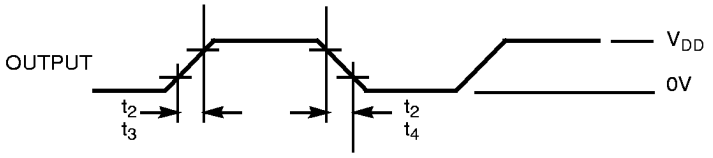
6. All parameters specified with loaded outputs.
7. Duty cycle is measured at 1.5V when V_{DD} = 3.3V. When V_{DDCPU} = 2.5V, CPUCLK duty cycle is measured at 1.25V.

Switching Waveforms

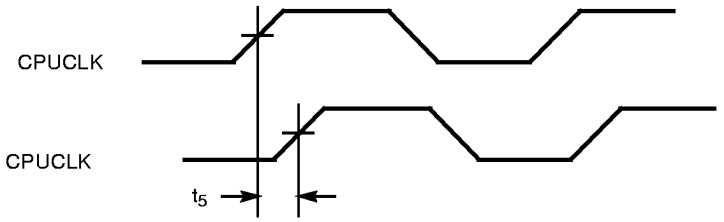
Duty Cycle Timing



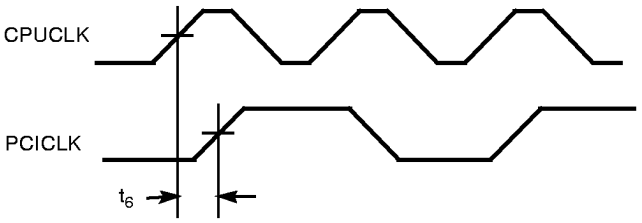
All Outputs Rise/Fall Time



Clock Skew

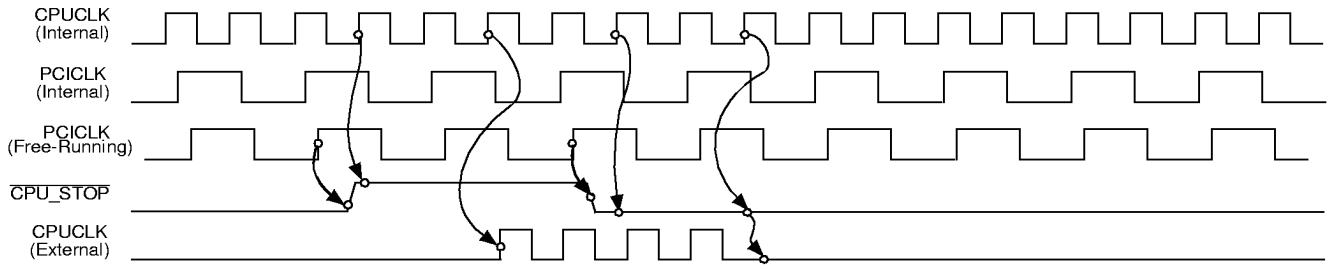


CPU-PCI Clock Skew

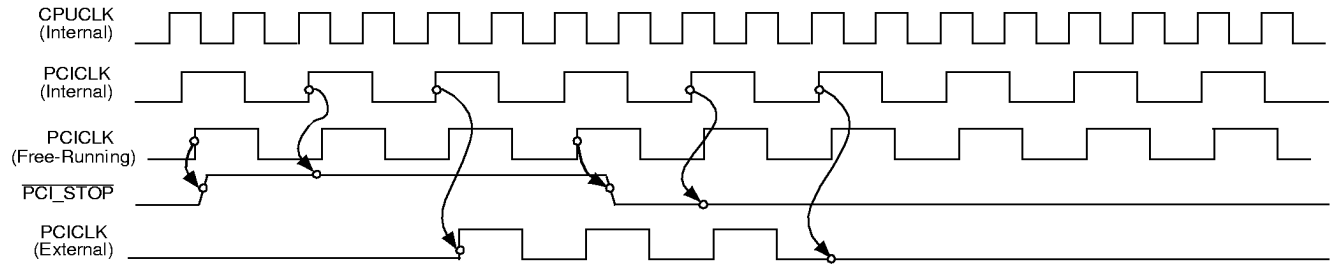


Switching Waveforms (continued)

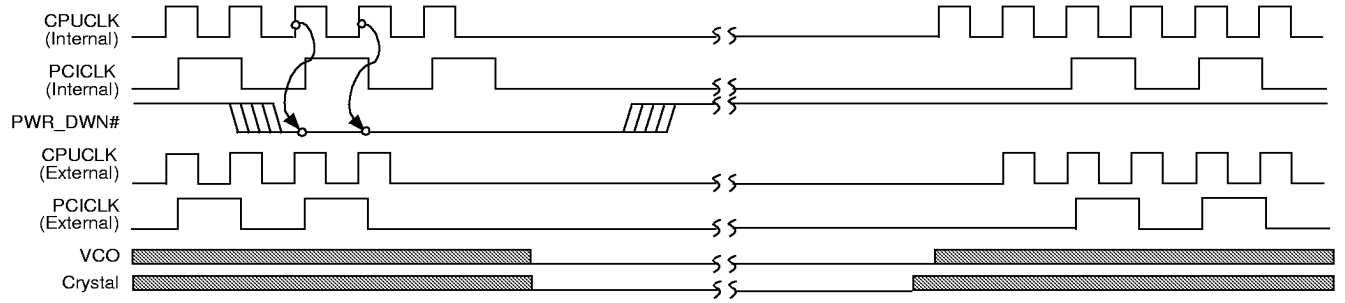
CPU_STOP [8, 9]



PCI_STOP [10, 11]



PWR_DOWN



Shaded section on the VCO and Crystal waveforms indicates that the VCO and crystal oscillator are active, and there is a valid clock.

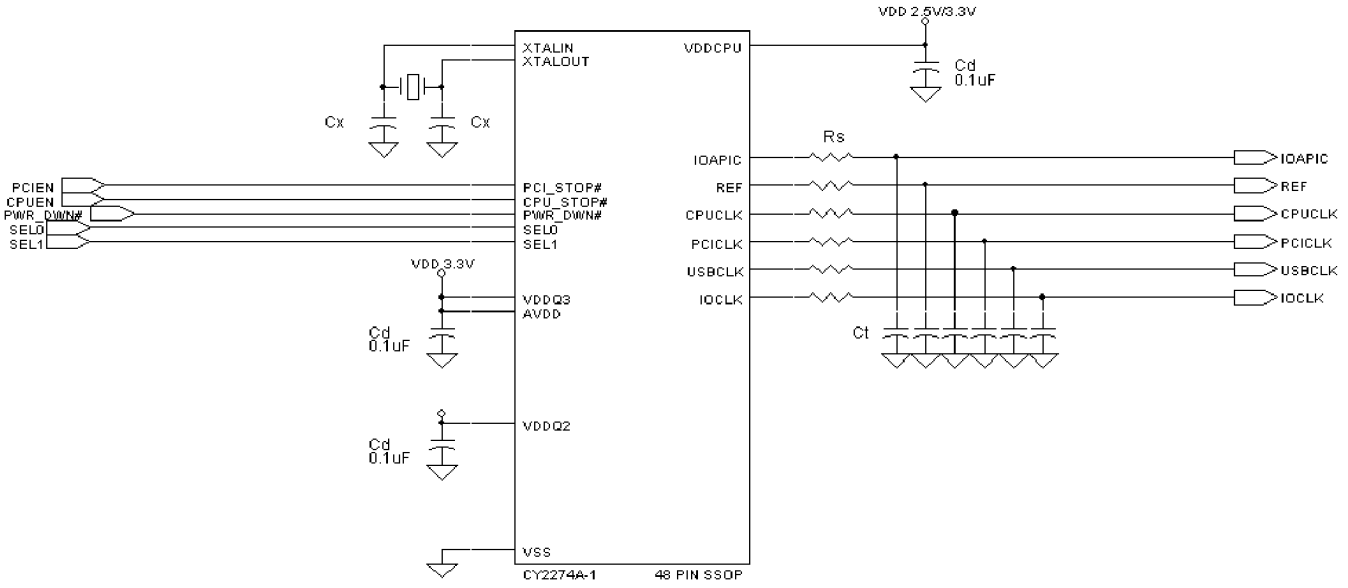
Notes:

8. CPUCLK on and CPUCLK off latency is 2 or 3 CPUCLK cycles.
9. CPU_STOP may be applied asynchronously. It is synchronized internally.
10. PCICLK on and PCICLK off latency is 1 rising edge of the external PCICLK.
11. PCI_STOP may be applied asynchronously. It is synchronized internally.

Application Information

Clock traces must be terminated with either series or parallel termination, as they are normally done.

Application Circuit



Cd = DECOUPLING CAPACITORS

Ct = OPTIONAL EMI-REDUCING CAPACITORS

Cx = OPTIONAL LOAD MATCHING CAPACITOR

Rs = SERIES TERMINATING RESISTORS

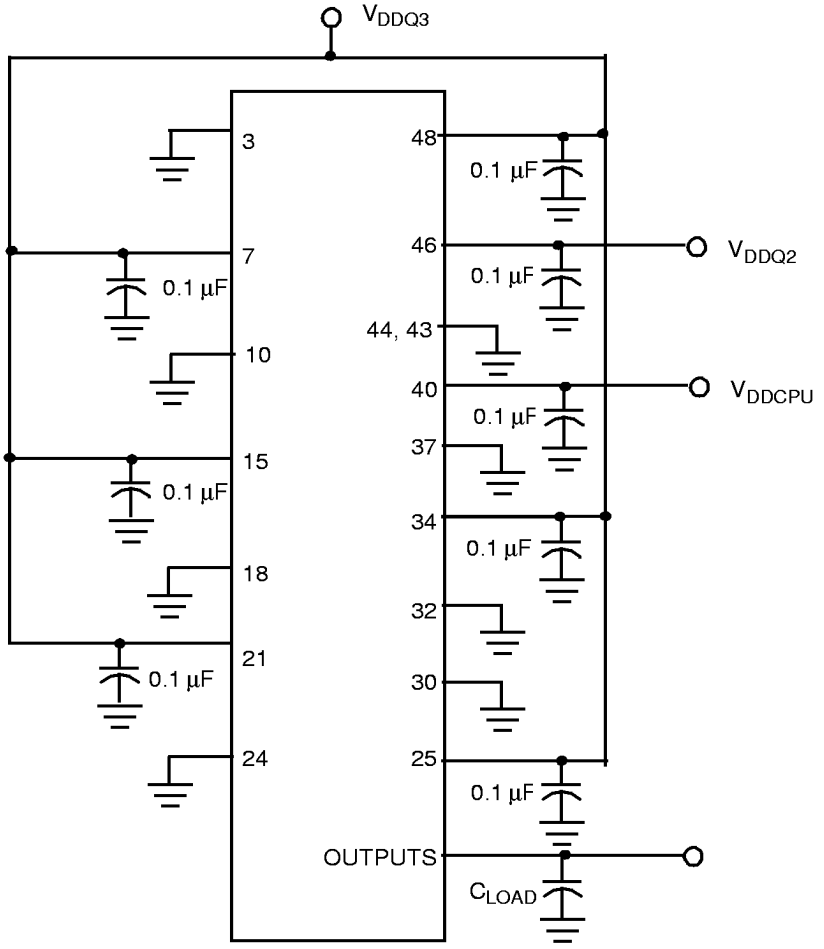
Summary

- A parallel-resonant crystal should be used as the reference to the clock generator. The operating frequency and C_{LOAD} of this crystal should be as specified in the data sheet. Optional trimming capacitors may be needed if a crystal with a different C_{LOAD} is used. Footprints must be laid out for flexibility.
- Surface mount, low-ESR, ceramic capacitors should be used for filtering. Typically, these capacitors have a value of 0.1 µF. In some cases, smaller value capacitors may be required.
- The value of the series terminating resistor satisfies the following equation, where R_{trace} is the loaded characteristic impedance of the trace, R_{out} is the output impedance of the clock generator (specified in the data sheet), and R_{series} is the series terminating resistor.

  $$R_{series} \geq R_{trace} - R_{out}$$

- Footprints must be laid out for optional EMI-reducing capacitors, which should be placed as close to the terminating resistor as is physically possible. Typical values of these capacitors range from 4.7 pF to 22 pF.
- A Ferrite Bead **may** be used to isolate the Board V_{DD} from the clock generator V_{DD} island. Ensure that the Ferrite Bead offers greater than 50Ω impedance at the clock frequency, under loaded DC conditions. Please refer to the application note “Layout and Termination Techniques for Cypress Clock Generators” for more details.
- If a Ferrite Bead is used, a 10 µF– 22 µF tantalum bypass capacitor should be placed close to the Ferrite Bead. This capacitor prevents power supply droop during current surges.

Test Circuit



Note: All capacitors should be placed as close to each pin as possible.

Ordering Information

Ordering Code	Package Name	Package Type	Operating Range
CY2274APVC–1	O48	48-Pin SSOP	Commercial

Document #: 38–00616

Package Diagram

48-Lead Shrunk Small Outline Package O48