AS7C256L
AS7C256LL

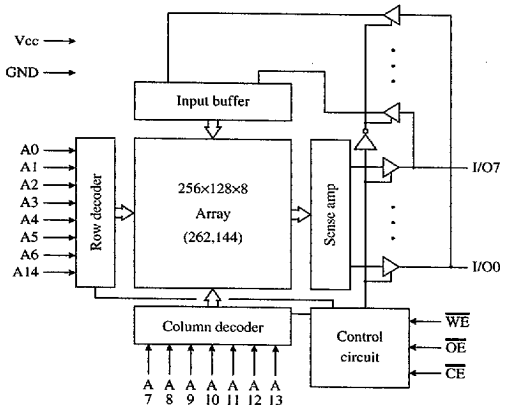
Low power 32K×8 CMOS SRAM

Advance information

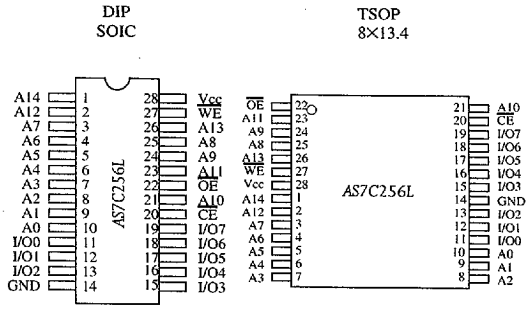
Features

- Organization: 32,768 words × 8 bits
- High speed
  - 55/70 ns address access time
  - 30/35 ns output enable access time
- Low power consumption
  - Active: 385 mW max (10 ns cycle)
  - Standby: 550 µW max, CMOS I/O, L version
    138 µW max, CMOS I/O, LL version
  - Very low DC component in active power
- 2.0V data retention
- Ultra low power in standby mode
- Equal access and cycle times
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ inputs
- TTL-compatible, three-state I/O
- 28-pin JEDEC standard packages
  - 600 mil PDIP
  - 330 mil SOIC
  - 8×13.4 TSOP
- 5V power supply

Logic block diagram



Pin arrangement



Selection guide

	7C256L-55	7C256L-70	Unit
Maximum address access time	55	70	ns
Maximum output enable access time	30	35	ns
Maximum operating current	70	70	mA
Maximum CMOS standby current	100	100	µA

Functional description

The AS7C256L is a low power CMOS 262,144-bit Static Random Access Memory (SRAM) organized as 32,768 words × 8 bits.

Equal address access and cycle times (t_{AA}, t_{RC}, t_{WC}) of 55/70 ns with output enable access times (t_{OE}) of 30/35 ns are ideal for high performance applications. A chip enable ($\overline{CE}$) input permits easy memory expansion with multiple-bank memory organizations.

When $\overline{CE}$ is HIGH the device enters standby mode. The standard AS7C256L is guaranteed not to exceed 550 µW, and typically requires only 300 µW. It also offers 2.0V data retention, with maximum power consumption in this mode of 100 µW.

A write cycle is accomplished by asserting chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) LOW. Data on the input pins I/O0-I/O7 is written on the rising edge of $\overline{WE}$ (write cycle 1) or $\overline{CE}$ (write cycle 2). To avoid bus contention, external devices should drive I/O pins only after outputs have been disabled with output enable ($\overline{OE}$) or write enable ($\overline{WE}$).

A read cycle is accomplished by asserting chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) LOW, with write enable ($\overline{WE}$) HIGH. The chip drives I/O pins with the data word referenced by the input address. When chip enable or output enable is HIGH, or write enable is LOW, output drivers stay in high-impedance mode.

All chip inputs and outputs are TTL-compatible, and operation is from a single 5V supply. The AS7C256L is packaged in high volume industry standard packages.

Absolute maximum ratings

Parameter	Symbol	Min	Max	Unit
Voltage on any pin relative to GND	V_t	−0.5	+7.0	V
Power dissipation	P_D	–	1.0	W
Storage temperature (plastic)	T_{stg}	−55	+150	°C
Temperature under bias	T_{bias}	−10	+85	°C
DC output current	I_{out}	–	20	mA

Stresses greater than those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Truth table

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Data	Mode
H	X	X	High Z	Standby (I_{SB}, I_{SB1})
L	H	H	High Z	Output disable
L	H	L	D_{out}	Read
L	L	X	D_{in}	Write

Key: X = Don't Care, L = LOW, H = HIGH

Recommended operating conditions

(T_a = 0°C to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0.0	0.0	0.0	V
Input voltage	V_{IH}	2.2	–	V_{CC}+0.3	V
	V_{IL}	−0.3†	–	0.8	V

†V_{IL} min = −3.0V for pulse width less than $t_{RC}/2$.

DC operating characteristics[1]

(V_{CC} = 5V ± 0.5V, GND = 0V, T_a = 0°C to +70°C)

Parameter	Symbol	Test conditions	L versions Min	L versions Max	LL versions Min	LL versions Max	Unit
Input leakage current	$\|I_{LI}\|$	V_{CC} = Max, V_{in} = GND to V_{CC}	–	1	–	1	µA
Output leakage current	$\|I_{LO}\|$	$\overline{CE}$ = V_{IH}, V_{CC} = Max, V_{out} = GND to V_{CC}	–	1	–	1	µA
Operating power supply current	I_{CC1}	$\overline{CE}$ = V_{IL}, f = f_{max}, I_{out} = 0 mA	–	70	–	70	mA
	I_{CC2}	$\overline{CE}$ ≤ 0.2V, f = 1MHz, V_{IL} ≤ 0.2V, V_{IH} ≥ V_{CC} - 0.2V, I_{out} = 0 mA	–	15	–	15	mA
Standby power supply current	I_{SB}	$\overline{CE}$ = V_{IH}, f = f_{max}	–	3	–	2	mA
	I_{SB1}	$\overline{CE}$ > V_{CC}–0.2V, f = 0, V_{in} ≤ 0.2V or V_{in} ≥ V_{CC}–0.2V	–	100	–	25	µA
Output voltage	V_{OL}	I_{OL} = 2.1 mA, V_{CC} = Min	–	0.4	–	0.4	V
	V_{OH}	I_{OH} = -1.0 mA, V_{CC} = Min	2.4	–	2.4	–	V

Capacitance[2]

(f = 1 MHz, T_a = Room temperature, V_{CC} = 5V)

Parameter	Symbol	Signals	Test conditions	Max	Unit
Input capacitance	C_{IN}	A, $\overline{CE}$, $\overline{WE}$, $\overline{OE}$	V_{in} = 0V	5	pF
I/O capacitance	$C_{I/O}$	I/O	V_{in} = V_{out} = 0V	7	pF

Key to switching waveforms

Rising input | Falling input | Undefined output/don't care

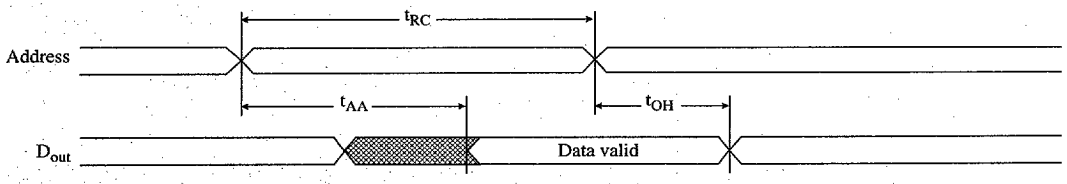
Read cycle[3,9]

(V_{CC} = 5V±0.5V, GND = 0V, T_a = 0°C to +70°C)

		-55		-70			
Parameter	*Symbol*	*Min*	*Max*	*Min*	*Max*	*Unit*	*Notes*
Read cycle time	t_{RC}	55	–	70	–	ns	
Address access time	t_{AA}	55	–	70	–	ns	3
Chip enable ($\overline{CE}$) access time	t_{ACE}	55	–	70	–	ns	3
Output enable ($\overline{OE}$) access time	t_{OE}	30	–	35	–	ns	
Output hold from address change	t_{OH}	5	–	5	–	ns	5
$\overline{CE}$ LOW to output in Low Z	t_{CLZ}	10	–	10	–	ns	4, 5
$\overline{CE}$ HIGH to output in High Z	t_{CHZ}	20	–	25	–	ns	4, 5
$\overline{OE}$ LOW to output in Low Z	t_{OLZ}	5	–	5	–	ns	4, 5
$\overline{OE}$ HIGH to output in High Z	t_{OHZ}	20	–	25	–	ns	4, 5

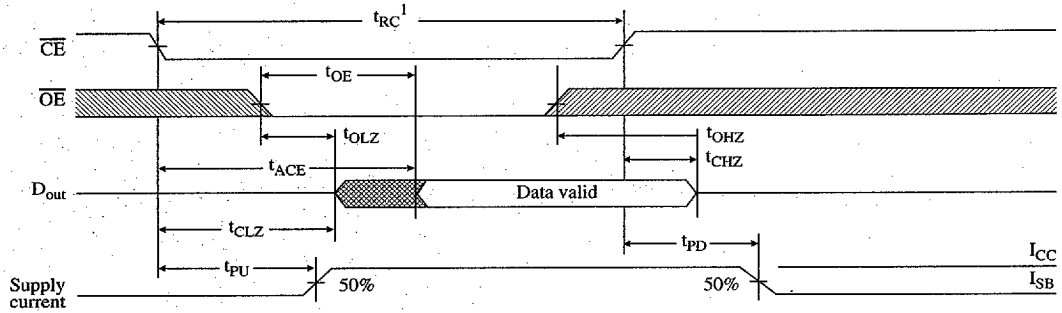
Read waveform 1[3,6,7,9]

(Address controlled)



Read waveform 2[3,6,8,9]

($\overline{CE}$ controlled)



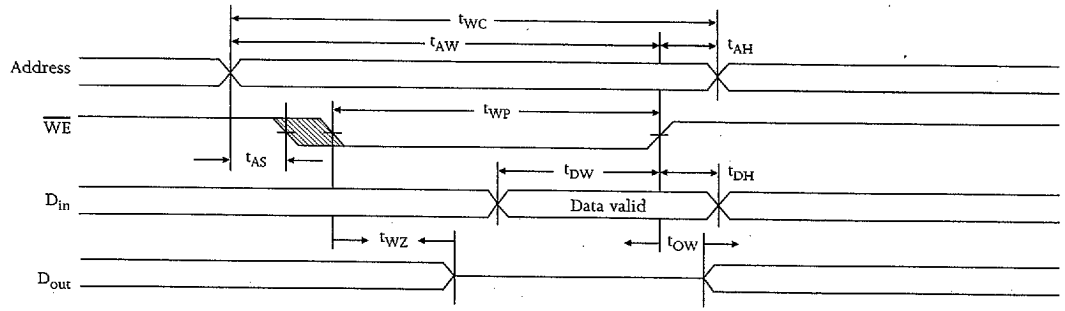
Write cycle [11]

(V_{CC} = 5V±0.5V, GND = 0V, T_a = 0°C to +70°C)

Parameter	Symbol	-55 Min	-55 Max	-70 Min	-70 Max	Unit	Notes
Write cycle time	t_{WC}	55	–	70	–	ns	
Chip enable to write end	t_{CW}	55	–	60	–	ns	
Address setup to write end	t_{AW}	50	–	60	–	ns	
Address setup time	t_{AS}	0	–	0	–	ns	
Write pulse width	t_{WP}	40	–	50	–	ns	
Address hold from end of write	t_{AH}	0	–	0	–	ns	
Data valid to write end	t_{DW}	25	–	30	–	ns	
Data hold time	t_{DH}	0	–	0	–	ns	4, 5
Write enable to output in High Z	t_{WZ}	–	25	–	30	ns	4, 5
Output active from write end	t_{OW}	35	–	5	–	ns	4, 5

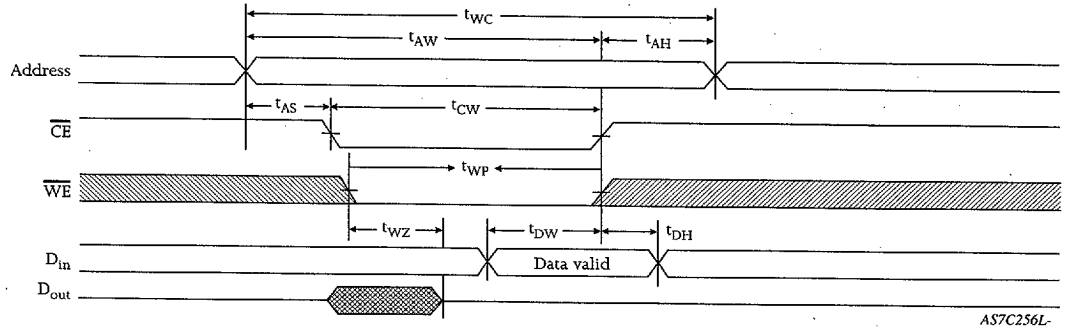
Write waveform 1 [10,11]

($\overline{WE}$ controlled)



Write waveform 2 [10,11]

($\overline{CE}$ controlled)



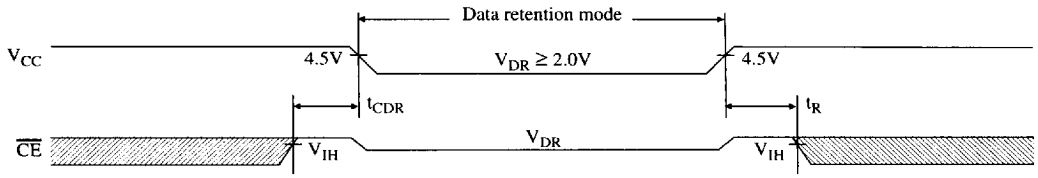
AS7C256L-

SRAM

Data retention characteristics

Parameter		Symbol	Test conditions	Min	Max	Unit
V_{CC} for data retention		V_{DR}	V_{CC} = 2.0V	2.0	5.5	V
Data retention current	L	I_{CCDR}	$\overline{CE} \geq V_{CC}-0.2V$	–	50	µA
	LL			–	10	µA
Chip enable to data retention time		t_{CDR}	$V_{in} \geq V_{CC}-0.2V$ or $V_{in} \leq 0.2V$	0	–	ns
Operation recovery time		t_R		5	–	ms

Data retention waveform



AC test conditions

- Output load: see Figure B, except for t_{CLZ} and t_{CHZ} see Figure C.
- Input pulse level: GND to 3.0V. See Figure A.
- Input rise and fall times: 5 ns. See Figure A.
- Input and output timing reference levels: 1.5V.

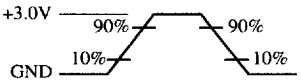


Figure A: Input waveform

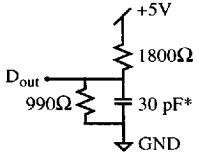


Figure B: Output load

Thevenin Equivalent:

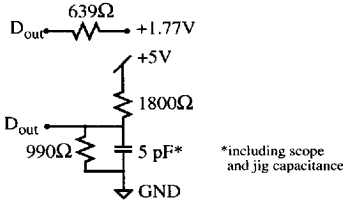


Figure C: Output load for t_{CLZ}, t_{CHZ}

Notes

1 During V_{CC} power-up, a pull-up resistor to V_{CC} on $\overline{CE}$ is required to meet I_{SB} specification.
2 This parameter is sampled and not 100% tested.
3 For test conditions, see *AC Test Conditions*, Figures A, B, C.
4 t_{CLZ} and t_{CHZ} are specified with CL = 5pF as in Figure C. Transition is measured ±500mV from steady-state voltage.
5 This parameter is guaranteed but not tested.
6 $\overline{WE}$ is HIGH for read cycle.
7 $\overline{CE}$ and $\overline{OE}$ are LOW for read cycle.
8 Address valid prior to or coincident with $\overline{CE}$ transition LOW.
9 All read cycle timings are referenced from the last valid address to the first transitioning address.
10 $\overline{CE}$ or $\overline{WE}$ must be HIGH during address transitions.
11 All write cycle timings are referenced from the last valid address to the first transitioning address.

AS7C256L(L) ordering codes

Package / Access time	55 ns	70 ns
Plastic DIP, 600 mil	AS7C256L-55PC AS7C256LL-55PC	AS7C256L-70PC AS7C256LL-70PC
Plastic SOIC, 330 mil	AS7C256L-55SC AS7C256LL-55SC	AS7C256L-70SC AS7C256LL-70SC
TSOP 8×13.4	AS7C256L-55TC AS7C256LL-55TC	AS7C256L-70TC AS7C256LL-70TC

Shaded areas indicate advance information.

AS7C256L(L) part numbering system

AS7C	256	X	–XX	X	C
SRAM prefix	Device number	L = Low power L L = Very low power	Access time	Package: P = PDIP 300 mil S = SOIC 330 mil T = TSOP 8×14	Commercial temperature range, 0°C to 70 °C