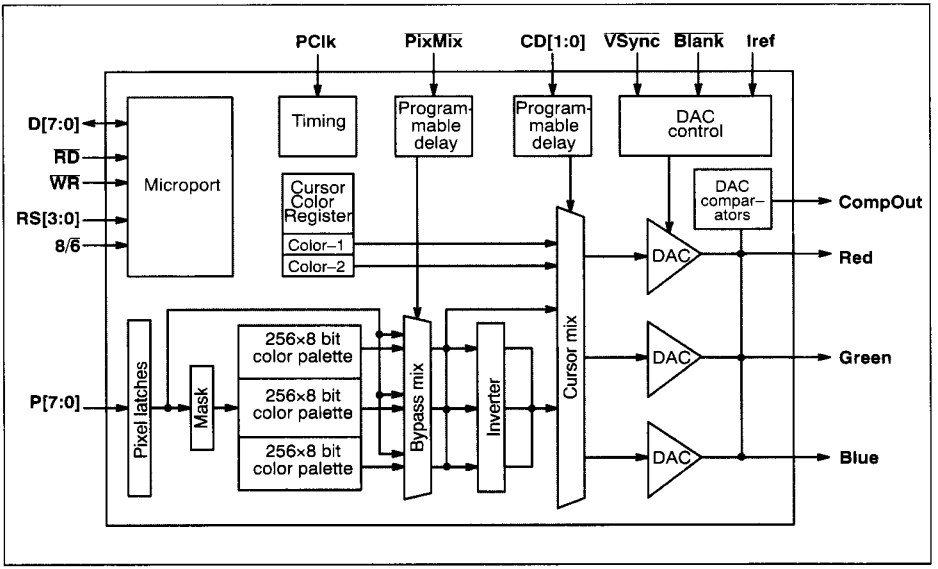
IMS G174

TRUE COLOR PALETTE-DAC WITH PixMix™

PRELIMINARY INFORMATION



FEATURES

- Compatible with VGA standard IMS G171/176
- Compatible with Sierra SC1148x family
- Pixel rates up to 85MHz
- Single or double edge latching high color modes
- 16-bit 5:5:5, 5:6:5, 6:6:4 and Select:5:5:5 true color formats supported
- 24-bit true/full color 8:8:8 format supported
- Synchronous PixMix pseudo/true color switching on pixel boundaries (in hardware or software)
- XGA compatible micro port option
- XGA compatible cursor palette
- Triple 6 or 8-bit DACs with output comparators

FEATURES

- DAC gain and auto-fade under register control
- DAC uses external current reference (**Iref**). For Advance Information on Iref/Vref version refer to page 91.
- 256×24 palette RAM with anti-sparkle
- 44-pin PLCC package

APPLICATIONS

- Leading edge VGA with high color
- XGA compatible systems
- TARGA format add-in boards
- Low-cost multimedia systems
- Low-cost 24-bit full color applications

TABLE OF CONTENTS

6.1 Description

The IMS G174 is a backwards compatible superset of the IMS G171/173/176 series of SGS-THOMSON palette-DACs. It provides a number of additional features to enable support of enhanced VGA, XGA, true color and multimedia applications.

A standard VGA pseudo color mode is supported, offering simultaneous display of 256 colors from a choice of 256K if used in 6-bit DAC mode, or from a choice of 16M colors in 8-bit DAC mode.

The IMS G174 also supports high color modes with an extensive range of pixel formats to generate true color displays. This is achieved in a low pin-count device by assembling successive bytes on the pixel port into larger pixel words. 16-bit pixel formats supported include 5:5:5 TARGA format, 5:6:5 XGA format, 6:6:4 i860 format and Select:5:5:5 mixed file format. Also supported is a 24-bit 8:8:8 format. These modes and formats can be controlled asynchronously in software through control registers. The Select:5:5:5 format allows the synchronous switching of pixel formats by software on a pixel-by-pixel basis.

Additionally the high color modes can be enabled and disabled synchronously using the **PixMix** pin. The IMS G174 can be used to switch pixel formats on a pixel-by-pixel basis, and therefore display mixed pseudo and true color images on the same screen. This offers the "picture-in-picture" capability required by many multimedia and windowing applications. Palette integrity is maintained while switching, so no re-writing of the palette is required when displaying mixed format images simultaneously.

The IMS G174 is fully compatible with existing high color features available on some graphics system controllers. It is also pin and software compatible with the Sierra SC1148x family of high color palette-DACs, though offering significant extra functionality.

An XGA compatible cursor palette has been added to make overlay or cursor generation easy and powerful.

The IMS G174 is easy to use within an XGA system due to its interface being fully compatible with the IBM XGA standard. As a result, the IMS G174 supports the use of interrupts by making the state of the micro port fully available to be examined and specified. This is particularly significant when interrupting color palette accesses which can be performed as a series of block writes or reads.

Circuitry has been added to the DACs to provide controllable gain and automatic fading, enabling smooth fading of the display under register control without changing the display memory contents. On-chip comparators provide additional information for software interaction and board level debugging.

6.2 Pin function reference guide

6.2.1 Pixel interface

Signal	I/O	Pin(s)	Signal name	Description
PClk	I	40	Pixel Clock	The rising edge of the Pixel Clock controls the sampling of values on the synchronous interface (the Pixel Data, Cursor Data, PixMix, VSync and Blank inputs). (NB: High Color Mode 1 references to both edges of the pixel clock, see Section 6.4.3.)
P[7:0]	I	39, 38, 37, 36, 35, 34, 33, 32	Pixel port	In pseudo color mode the values latched at this port are used as addresses to point to an entry in the Color Palette. The data at this port may, for example, be supplied by an existing VGA display controller. The data at the pixel port is also affected by the Pixel Select Function, enabled whenever the **$\overline{\text{PixMix}}$** pin is latched Low or the Pixel Select Bit is set to a logical "1". In such a case, the value of the Pixel Command register may allow the pixel data value to form a true color pixel which then bypasses the palette and is applied directly to the DACs. (The control of this data and its use is described in Section 6.4, *Pixel Interface Operation.*)
$\overline{\text{PixMix}}$	I	20	Pixel Mixing	This pin is inverted and logical ORed with the Pixel Select Bit (bit 7 of the Pixel Command Register) to enable the high color modes on a pixel by pixel basis. When the high color modes are inactive, **P[7:0]** is used as an address to the Color Palette. When the high color modes are enabled for a particular pixel, data other than straight VGA data from input pins **P[7:0]** is used to generate a display pixel. The high color mode used and pixel format enabled are determined by the contents of the pixel command register. (Refer to Section 6.4, *Pixel Interface Operation* for a full explanation.)
CD[1:0]	I	42, 41	Cursor Data	Values latched at these pins are used to enable the display of the hardware cursor palette at an individual pixel. (Refer to Section 6.5, *Cursor Data Inputs* for a full explanation.)
$\overline{\text{Blank}}$	I	7	Blank	A latched low value causes a color value of zero to be applied to the DACs' input regardless of the present pixel color.
$\overline{\text{VSync}}$	I	5	Vertical Sync	The falling edge of Vertical Sync decrements the Frame Counter to facilitate the fading of the DAC outputs. This pin does not add any sync pedestal to the analogue outputs. It may be held to Gnd if the DAC fade feature is not required.

6.2.2 Micro port

Signal	I/O	Pin(s)	Signal name	Description
RD	I	6	Read Enable	Read Enable controls the timing of the asynchronous microprocessor interface during a read operation. The Read Enable pin latches **RS[3:0]** on its falling edge and immediately accesses the selected register. The selected data is driven out from Program Data pins **D[7:0]** before a maximum specified time has elapsed. When the Read Enable pin has been taken high again the data on **D[7:0]** is held for a specified time before the pins are tri-stated.
WR	I	16	Write Enable	Write Enable controls the timing of the asynchronous microprocessor interface during a write operation. The Write Enable pin latches **RS[3:0]** on its falling edge and writes the data present on the Program Data Bus sampled by the rising edge of the Write Enable signal to the specified register.
RS[3:0]	I	21, 19, 18,17	Register Select	The values on these inputs are sampled on the falling edge of Read and Write Enable and are used to specify the register to be accessed. (Refer to Section 6.3, *Internal Register Description* for a full description of the function of these registers.)
D[7:0]	I/O	15, 14, 13, 12, 11, 10, 9, 8	Program Data	Data is transferred between the 8-bit wide bidirectional Program Data bus and the registers within the IMS G174 under control of the active enable signals.
8/6	I	2	8/6-bit mode select	When this pin is held high, 8-bit DAC resolution is provided. When this bit is held low, 6-bit DAC resolution is provided and all color data written or read from the IMS G174 is given in 6-bit form. If XGA mode is enabled, data is transferred to/from the upper 6 bits of **D[7:0]**. If it is disabled, data is transferred to/from the lower 6 bits.

6.2.3 Analogue interface

Signal	I/O	Pin(s)	Signal name	Description
Red, Green, Blue	O	25, 26, 27	Red, Green, Blue	8-bit DAC video outputs (drive into a doubly terminated 75Ω load). Internal compensation ensures correct full-scale output is maintained, regardless of 6 or 8-bit operation.
Iref	I	28	Current Reference	The reference current drawn from **AVdd** via the **Iref** pin determines the current sourced by each DAC. See Chapter 10 for details on the design of an external current reference circuit.
Comp-Out	O	1	Comparator Output	An analogue pin which provides the result of the on-chip DAC comparators. **CompOut** is a logical zero if one or more of the DAC outputs exceeds the internal reference (typically 335mV at 5V supply voltage, independent of **Iref** current).

6.2.4 Power supply

Signal	Signal name	Pin	Description
Vdd	Digital Supply	4	Digital logic is supplied via **Vdd**
AVdd	Analogue Supply	22	Analogue circuitry, including DACs and reference circuitry, is supplied through the **AVdd** pin. Digital and Analogue power to the IMS G174 is supplied on separate pins to provide maximum noise immunity. **These two pins should both be connected to the same power supply immediately outside the IMS G174.**
Gnd	Ground	3,24	All ground pins must be connected.
NC		23, 29, 30, 31	These pins are not used by the current IMS G173/4. Links that are required for other manufacturer's devices will not affect the operation of the IMS G173/4.
NC or **hold to Gnd**		43, 44	

6.3 Internal register description

The IMS G174 internal registers are addressed in two different ways. The first method (direct access) gives access to a number of registers directly addressed by the **RS[3:0]** pins. One of two register address maps is used depending on whether the XGA or VGA operating mode of the IMS G174 has been enabled. The direct access registers are described in Section 6.3.1.

The second method (indexed access) gives access to a number of additional indexed registers, indirectly addressed through the XGA Index Register when the IMS G174 is in XGA mode. These registers map according to the XGA specification and may only be accessed when the IMS G174 is in XGA mode, although their contents may affect the display when in VGA mode (for example cursor color). Indexed access registers are described in Section 6.3.2 (page 73).

On power-on the micro port is fully compatible with the IMS G176 industry standard VGA device. To maintain hardware compatibility, where the additional **RS[3:2]** signals are not available, both XGA and high color modes can be selected in software by specific read sequences to the Pixel Mask Register (see the XGA Enable Register and Pixel Command Register descriptions).

All bits of all registers (with the exception of the Color Value Register in 6-bit mode) can be read and written, and will return the last written data when read. All Reserved register bits must be written as "0" and will be read back as "0". In 6-bit mode the two most significant bits of the Color Value Register are ignored on write and return "00" on read. This can be useful in indicating that 6-bit mode is in operation.

6.3.1 Direct Access I/O Registers

The direct access registers of the IMS G174 are divided into three main groups:

1 **Standard VGA registers.** Four registers which can be used to program the IMS G174 in exactly the same way as the industry standard IMS G171 and G176. These registers are only available if the IMS G174 is in VGA mode (enabled by the XGA Enable Register or on power-up). In this condition multiple RS addresses give access to the VGA Registers, and the XGA Index and Data Registers are not available. This feature provides compatibility with some XGA chip sets which decode the VGA registers to locations #X8, #9, #X6 and #X7, and also with existing IMS G176 systems which would only supply **RS[3:2]** (pins 21,19) with Vdd and Gnd, thereby using IMS G174 register locations #X8, #X9, #XA, and #XB.

2 **XGA registers.** Three registers, the XGA Enable Register and XGA Index and Data Registers, which implement the XGA style of access to the device. The XGA enable register selects the XGA or VGA operating mode of the IMS G174 (and is accessible in either mode). The XGA Index and Data Registers are used to access the IMS G174 indexed registers when XGA mode has been enabled (see Section 6.3.2).

3 **Hardware control registers.** Four registers, which can be directly accessed in XGA and VGA modes, responsible for the configuration of the IMS G174. These control such features as the pixel format, the DAC gain and fade control and the programmable delays on the Pixel Select and Cursor Data input paths.

The **RS** address map for the IMS G174 in both VGA and XGA modes is shown in Table 6.1.

Hex Address	RS[3:0]	Address map in VGA mode	Address map in XGA mode	Register Type	See page
0	0000	XGA Enable	XGA Enable	XGA	66
1	0001	Reserved	Reserved		
2	0010	Reserved	Reserved		
3	0011	Reserved	Reserved		
4	0100	Address (write mode)	Reserved	VGA	67
5	0101	Color Value	Reserved	VGA	67
6	0110	Pixel Mask	Reserved	VGA	67
7	0111	Address (read mode)	Reserved	VGA	67
8	1000	Address (write mode)	Reserved	VGA	67
9	1001	Color Value	Reserved	VGA	67
A	1010	Pixel Mask		VGA	67
			XGA Index	XGA	72
B	1011	Address (read mode)		VGA	67
			XGA Data	XGA	72
C	1100	DAC Fade	DAC Fade	Hardware	68
D	1101	DAC Gain	DAC Gain	Hardware	69
E	1110	Pixel Command	Pixel Command	Hardware	70
F	1111	Hardware Delay	Hardware Delay	Hardware	72

Table 6.1 RS Address Map in VGA and XGA Modes

XGA Enable Register (#X0)

The contents of the XGA Enable Register sets the IMS G174 to be in either VGA or XGA operating mode.

When in VGA mode, the device may be controlled through the standard VGA registers described earlier.

When XGA mode is enabled, the indexed registers may then be accessed by performing *Indexed Accesses* through the XGA Index Register and XGA Data Register. The XGA Enable Register is available in both VGA and XGA modes.

To enable access to the features of the XGA Enable Register by existing VGA hardware designs where the **RS[3:2]** signals are not provided, eight successive reads of the Pixel Mask Register will set an internal flag which will allow the next read or write access to the pixel mask to be directed to the XGA Enable Register. Any other access at any time will reset this flag operation. Where possible, it is recommended that the additional **RS** pin inputs be exercised to access this register in the normal way.

Bit	R/W	Value	Function
7:4	R/W		Reserved, write as "0"
3	R/W	X	No effect
2:0	R/W	0XX	VGA Mode Enable
		100	XGA Mode Enable
		101	Reserved
		110	Reserved
		111	Reserved

Table 6.2 XGA Enable Register (#X0)

Address Registers (#X4, #X7, #X8 and #XB)

These registers are identical to those in a standard IMS G171 or G176 device. Loading a value into the Address Register (write mode) points to a palette location which is written to when additional writes to the Color Value Register are performed. Similarly, when a value is written to the Address Register (read mode), a read from the palette is performed which makes the palette data for that specified address available to be read through the Color Value Register. (This could also be described as a *Prefetch* operation, which will be referred to when the XGA Registers are described.) Block accesses are allowed to the color palette by the Address Register incrementing to point to the next location, after three consecutive writes to the Color Value Register on write cycles. On read cycles the Address Register is automatically incremented **before** every block of three reads from the Color Value Register.

Bit	R/W	Function
7:0	R/W	Palette Address

Color Value Register (#X5 and #X9)

Data may be transferred to and from the color palette via successive accesses to the 8-bit Color Value Register.

If 6-bit operation is selected by the **8/$\overline{6}$** pin being taken low, only the 6 least significant bits of this register are used to update the color palette, maintaining compatibility with the VGA standard. When displayed, this data is presented to the upper bits of the DAC, with the two least significant bits held to zero. The IMS G174 internally compensates for 8 or 6-bit modes of operation, maintaining the correct full scale output in each case.

Mode	Bit	R/W	Function
8-bit VGA	7:0	R/W	Palette Data
6-bit VGA	7:6 5:0	R R/W	Ignored on write, 00 on read. Palette Data

Pixel Mask Register (#X6 and #XA)

The Palette Mask provides a bitwise AND function of the Palette Address entered through the synchronous VGA pixel port. True color pixels compiled from multiple bytes of VGA data are not interpreted as palette addresses and therefore are not affected by the Pixel Mask Register. Accesses through the micro port are not affected by the Pixel Mask. Access to the true color and XGA features of the IMS G174 may be obtained in software by specific read/write sequences to the Pixel Mask Register (see Pixel Command Register and XGA Enable Register Descriptions).

Bit	R/W	Function
7:0	R/W	Palette Address Mask

DAC Fade Register (#XC)

A fade facility has been provided whereby the DAC output intensity is automatically adjusted in order to achieve a smooth fade in or out of a picture. This effect is achieved without changing the contents of the display memory or the palette, releasing the processor or display controller of this compute-intensive task.

The DACs can be manually set to a fraction of their normal display intensity and can be faded from that intensity out to zero, or from zero up to that desired intensity. The automatic fade can be synchronized to the frame rate via the **VSync** pin, so that after initialization of parameters the fade in/out is achieved with just a single write operation.

The DAC Gain Register holds the two main values which control the fade: the upper end point of the DAC intensity and the speed of the fade measured in units of "frames displayed at each intensity level".

A Manual Mode is provided to enable manual control of the DAC Gain regardless of the state of a fade in/out.

An overall Gain Disable bit forces the DAC value to its normal intensity, thereby ignoring all the DAC Fade facilities.

A fade is initiated whenever the value of the Fade In/Out bit changes from one display frame to the next. A change of value from "1" to "0", for example will set the current Frame Counter value to the DAC Gain Value and initiate the start of a fade out procedure.

The length of a fade operation is the product of the DAC Gain value and the Fade Rate value. If all intensity levels are used, and each is held for a maximum of 30 frames, a maximum fade in/out period of approximately 8 seconds is possible with standard frame rates. An indication can be gained of the progress of a fade in software by reading the Current Frame Counter value. This counter always counts down from the DAC Gain Value to zero, decrementing on each falling edge of **VSync**, irrespective of whether a fade in or fade out is taking place. A low value of the Current Frame Counter therefore indicates the imminent conclusion of a fade operation.

When Manual mode has been selected, a fade request still initiates the counters to count frames, and the Current Frame Counter value still counts down to zero, although being in manual mode means that the DAC outputs will always obey the current DAC Gain value.

Bit[4] can be read as a single bit indication that the fade has been completed.

Bit	R/W	Value	Function
7	R/W	0	Gain Control Disabled (DACs at normal intensity)
		1	Gain Control Enabled (DACs at fraction of normal intensity
6	R/W	0	Automatic DAC Fading (DACs obey Frame Counter)
		1	Manual DAC Fading (DACs ignore Frame Counter)
5	R/W	0	Fade Out
		1	Fade In
4	R	0	Frame counting finished
		1	Frame counting still in progress
3:0	R		Current Frame Counter Value

Table 6.3 DAC Fade Register (#XC)

DAC Gain Register (#XD)

This register specifies the relative DAC intensity when DAC Gain Control has been enabled and the Fade Rate during a fade in or fade out.

Because of the non-linear nature of perceived intensity on a display screen, levels of fractional DAC intensity have been provided which give a *perceived* linear result. This will vary only slightly from one monitor to another due to common gamma values found in most monitors. Sixteen intensity levels have been provided including a zero level, approximating a square law behavior. The values of DAC Gain are guaranteed to be monotonic, although the absolute values may vary from device to device.

All display pixels are scaled by the specified factor to give a fraction of their normally specified intensity.

The Fade Rate has been specified as the upper four binary bits of a five bit value. The value of zero would have no meaning as a fade rate, so this defaults to the lowest allowed fade rate value of TWO frames per intensity level.

Bit	R/W	Value	DAC Gain Value
3:0	R/W	0000	DACs blanked
		0001	DACs 0.005 normal intensity, 1/15th perceived intensity
		0010	DACs 0.02 normal intensity, 2/15th perceived intensity
		0011	DACs 0.04 normal intensity, 3/15th perceived intensity
		0100	DACs 0.07 normal intensity, 4/15th perceived intensity
		0101	DACs 0.11 normal intensity, 5/15th perceived intensity
		0110	DACs 0.17 normal intensity, 6/15th perceived intensity
		0111	DACs 0.22 normal intensity, 7/15th perceived intensity
		1000	DACs 0.30 normal intensity, 8/15th perceived intensity
		1001	DACs 0.36 normal intensity, 9/15th perceived intensity
		1010	DACs 0.44 normal intensity, 10/15th perceived intensity
		1011	DACs 0.57 normal intensity, 11/15th perceived intensity
		1100	DACs 0.67 normal intensity, 12/15th perceived intensity
		1101	DACs 0.75 normal intensity, 13/15th perceived intensity
		1110	DACs 0.87 normal intensity, 14/15th perceived intensity
		1111	DACs at normal intensity
			Fade Rate Value
7:4	R/W	0000	Each intensity for TWO frames
		0001	Each intensity for TWO frames
		0010	Each intensity for FOUR frames
		0011	Each intensity for SIX frames
			. . . . .
		1111	Each intensity for THIRTY Frames

Table 6.4 DAC Gain Register (#XD)

Pixel Command Register (#XE)

The Pixel Command Register configures the Pixel Interface of the IMS G174, controlling the interpretation of Pixel Data supplied to the pixel port **P[7:0]**.

The **PixMix** pin is inverted and logical ORed with the Pixel Select bit to enable the high color modes on a pixel by pixel basis.

When the high color modes are disabled, pixel data **P[7:0]** is used unconditionally as an address to the color palette. When the high color modes are enabled for a particular pixel, data other than straight VGA data from input pins **P[7:0]** is used to generate a display pixel with the options described below. Color integrity of the palette is maintained during high color mode operation, so no rewriting of palette locations is required when switching between pseudo and true color modes.

When the **PixMix** pin is used to enable or disable the high color modes, a pixel by pixel capability is possible, allowing many VGA and true color displays on the same monitor screen. Due to the unsynchronized nature of a microprocessor access, this is not possible if software control alone is used.

To enable the features of the Pixel Command Register to be accessed by existing VGA hardware designs where **RS[3:2]** signals are not provided, four successive reads of the Pixel Mask Register will set an internal flag which will allow the next read or write access to the pixel mask to be directed to the Pixel Command Register. Any other access at any time will reset this flag operation. Where possible it is recommended that the additional RS pin inputs be exercised to access this register in the normal way.

True color formats

Once a pixel word has been assembled it may be interpreted as one of four true color RGB formats or a mixed file format. The true color format at any one time is determined by bits 3, 6 and 4 of the Pixel Command Register. The Mixed File format enables VGA and 15-bit true color data to be mixed in the same file and displayed conditionally on the status of bit[15] of the data field, giving a PixMix effect through software.

The specification of this register is backwards compatible with that provided on other high color devices which only specify register bits [7:5] in the command register, with all other bits reserved. In such a case, where bits [4:3] are written as zero, bit [6] (Pixel Format bit 1) becomes a selector bit between 5:6:5 and 5:5:5 true color formats.

High color modes

High color modes allow the creation of greater pixel depth by allowing multiple byte pixels to be constructed from successive bytes latched onto the pixel port pins **P[7:0]**. A full description of the two modes available and their operation is given in Section 6.4.3. Bit [0] of the Pixel Command Register is also explained in Section 6.4.3.

Cursor enable

The XGA cursor specification defines a transparent cursor to be the result of **CD[1:0]** = #X2. If the **CD[1:0]** pins have been held to Gnd, then the XGA cursor enable bit should be set to zero, making the cursor transparent irrespective of the state of the **CD[1:0]** inputs.

Bit	R/W	Value	Function
0	R/W	0	Pixel interface timing determined by High Color mode
		1	Force modified pixel sampling (High Color Mode 1 sampling specification)
1	R/W		Reserved, write as "0"
2	R/W	0	Disable XGA cursor
		1	Enable XGA cursor
3	R/W	0	Pixel Format bit 2 (see Table 6.4.3)
4	R/W		Pixel Format bit 0 (see Table 6.4.3)
5	R/W	0	High Color Mode 1
		1	High Color Mode 2
6	R/W		Pixel Format bit 1 (see Table 6.4.3)
7	R/W		Pixel Select Bit
		0	If the **PixMix** pin is latched as a logical "1", high color modes are disabled. If the **PixMix** pin is latched as a logical "0", they are enabled.
		1	Enable high color modes irrespective of the **PixMix** pin.

Table 6.5 Pixel Command Register (#XE)

Pixel Format bits [2:0]	Function
000	True color data is 5R 5G 5B
001	True color data is 8R 8G 8B
010	True color data is 5R 6G 5B
011	True color data is 6R 6G 4B
100	Mixed File Format for software PixMix (Select, 5R 5G 5B)
101	Reserved
110	Reserved
111	Reserved

Table 6.6 Interpretation of Pixel Format bits

Hardware Delay Register (#XF)

This register contains two delay values which determine the delay of the Pixel Mixing and Cursor Data paths. Having the ability to control these path delays independently in software makes synchronizing of data streams and designing with the IMS G174 easier and more tolerant of graphics system hardware design.

The Bypass delay contains the value of the programmable delay operating on the Pixel Mixing (**PIxMIx**) input path. The Cursor Data delay contains the value of the programmable delay operating on the Cursor Data (**CD[1:0]**) input path.

The default options assume that to be displayed on the same screen pixel, corresponding VGA, Pixel Mixing and Cursor Data must be latched at the inputs of the IMS G174 on the same **PCIk** cycle. Other values refer to how early or late data needs to be at their respective inputs relative to the VGA Pixel Port data in order to reference the same display pixel.

Bit	R/W	Value	Function
2:0	R/W		Cursor Data Delay
		000	Cursor Data Delay with respect to Pixel Port data = 0
		100	**CD[1:0]** TWO PCIks before **P[7:0]** to reference the same display pixel.
		101	**CD[1:0]** ONE PCIk before **P[7:0]** to reference the same display pixel.
		110	**CD[1:0]** ONE PCIk after **P[7:0]** to reference the same display pixel.
		111	**CD[1:0]** TWO PCIks after **P[7:0]** to reference the same display pixel.
3	R/W		Reserved, write as "0"
6:4	R/W		Pixel Mixing Delay
		000	Pixel Mixing signal delay with respect to Pixel Port data = 0
		100	**PIxMIx** TWO PCIks before **P[7:0]** to reference the same display pixel.
		101	**PIxMIx** ONE PCIk before **P[7:0]** to reference the same display pixel.
		110	**PIxMIx** ONE PCIk after **P[7:0]** to reference the same display pixel.
		111	**PIxMIx** TWO PCIks after **P[7:0]** to reference the same display pixel.
7	R/W		Reserved, write as "0"

Table 6.7 Hardware Delay Register (#XF)

XGA Index Register (#XA)

The contents of the XGA Index Register (#XA) are used as a pointer to select the additional indexed access registers (see Section 6.3.2).

Bit	R/W	Function
7:0	R/W	Pointer to an Indexed Register

XGA Data Register (#XB)

The XGA Index Register (#XA) is used as a pointer to select the additional XGA register to be accessed, which is then written to or read from by a write to or read from the XGA Data Register(#XB).

Bit	R/W	Function
7:0	R/W	Data contents for each Indexed register

6.3.2 Indexed Access I/O Registers (XGA mode)

The Indexed Access I/O registers are a number of indirectly accessed registers which map according to the published XGA specification. Of the large number of indexed registers included in the XGA specification only some are relevant to the operation of the IMS G174. Only those registers listed below are implemented; reads from unassigned index locations should not be performed on the IMS G174. The reason for this is that the Program Data Bus would be driven by the IMS G174 with indeterminate data, causing a possible contention with the real data residing elsewhere in the XGA subsystem.

Index Value	Indexed Register	See page
#X38	Cursor Color [0] Red	73
#X39	Cursor Color [0] Green	73
#X3A	Cursor Color [0] Blue	73
#X3B	Cursor Color [1] Red	73
#X3C	Cursor Color [1] Green	73
#X3D	Cursor Color [1] Blue	73
#X52	Display ID and comparator	74
#X60	Palette Index (same as Address Write Register)	74
#X62	Palette Index with Prefetch (same as Address Read Register)	74
#X64	Palette Mask (same as Pixel Mask Register)	74
#X65	Palette Data (same as Color Value Register)	75
#X66	Palette Sequence	76
#X67	Palette Red Value	76
#X68	Palette Green Value	76
#X69	Palette Blue Value	76

Table 6.8 Indexed Access I/O Registers

Each register is described in detail in the following pages.

Cursor Color Registers (Indexes #X38 – #X3D)

These registers contain the color component values for the cursor display. These colors are displayed directly and are not interpreted as addresses to be passed through the color palette. Although these registers may only be accessed when the IMS G174 is in XGA mode, the contents may be displayed according to the Cursor Data inputs **CD[1:0]** when the IMS G174 is in XGA or VGA mode.

If 6-bit operation is selected by the **8/$\overline{6}$** pin being taken low, bits [7:2] are presented to the upper bits of the DAC, with the two lowest bits being held to zero. Bits [1:0] of this register in 6-bit mode can still be accessed but not displayed.

Note: This is different to the effect of 6-bit operation elsewhere in the register set when VGA mode is active. VGA 6-bit mode uses the lowest 6 bits of the data field. XGA 6-bit mode involves the upper 6 bits of the data field.

Mode	Bit	R/W	Function
8-bit XGA	7:0	R/W	Cursor Color
6-bit XGA	7:2	R/W	Cursor Color

Table 6.9 Cursor Color Registers (Indexes #X38 – #X3D)

Display ID and Comparator Register (Index #X52)

This is a read only register, containing the results of the DAC comparators. Because the number of pins is restricted, the display ID cannot be fed into the IMS G174 from the monitor used. The value held in the display ID field of this register is set to read a fixed value unassigned by the XGA specification. When read, this value should be taken as indicating that the display ID is not representative of the monitor connected. In such circumstances other means should be used to determine the required resolution for the monitor type used.

Bit	R/W	Value	Function
4:0	R	00000	Display ID not representative of monitor connected
5	R	0	Red DAC output greater than comparator reference voltage
		1	Red DAC output less than comparator reference voltage
6	R	0	Green DAC output greater than comparator reference voltage
		1	Green DAC output less than comparator reference voltage
7	R	0	Blue DAC output greater than comparator reference voltage
		1	Blue DAC output less than comparator reference voltage

Table 6.10 Display ID and Comparator Register (Index #X52)

Palette Index Register (Index #X60)

Loading a value into the Palette Index Register points to a palette location which is updated when additional writes to the Palette Data register are performed. Block accesses are allowed to the color palette by the Address Register incrementing to point to the next location after three consecutive accesses to the Color Value register (or four consecutive accesses, depending on the Palette Sequence register).

Bit	R/W	Function
7:0	R/W	Palette Address

Palette Index with Prefetch Register (Index #X62)

Similar in operation to the Palette Index Register, when a value is written to the Palette Index with Prefetch Register, a read from the palette is performed which makes the palette data for that specified address available to be read through the Palette Data Register.

The Address Register is incremented before three color value read cycles during block reads.

Palette Mask Register (Index #X64)

The Palette Mask Register accessed through Index #X64 is identical to the Pixel Mask Register accessed when VGA mode is enabled.

Bit	R/W	Function
7:0	R/W	Palette Address Mask

Palette Data Register (Index #X65)

Data may be transferred to and from the color palette via successive accesses to the 8-bit Palette Data Register. This is identical in operation to the Color Value Register available in VGA mode.

There is an extra level of indirection necessary when in XGA mode. For example a typical palette access procedure could proceed as follows:

Access	Operation
Write #X60 to XGA Index Register	Points Data Register to Palette Index
Write #XNN to XGA Data Register	Sets Palette Index to location NN
Write #X65 to XGA Index Register	Points Data Register to Palette Data
Write #XRR to XGA Data Register	Writes RR as Red for location NN
Write #XGG to XGA Data Register	Writes GG as Green for location NN
Write #XBB to XGA Data Register	Writes BB as Blue for location NN
Write #XRR to XGA Data Register	Writes RR as Red for location NN+1

Table 6.11 Palette Data Register – typical access procedure

If 6-bit operation is selected by the **8/$\overline{6}$** pin being taken low, bits [7:2] are presented to the upper bits of the DAC, with the two lowest bits being held to zero. Bits [1:0] of this register in 6-bit mode can still be accessed but not displayed.

Note: This is different to the effect of 6-bit operation when VGA mode is active. VGA 6-bit mode uses the lowest 6 bits of the data field. XGA 6-bit mode involves the upper 6 bits of the data field.

Mode	Bit	R/W	Function
8-bit XGA	7:0	R/W	Palette Data
6-bit XGA	7:2	R/W	Palette Data
	1:0	R	Ignored on write, 00 on read.

Table 6.12 Palette Data Register (Index #X65)

Palette Sequence Register (Index #X66)

The Palette Sequence Register facilitates different palette data sequences while performing block reads from or block writes to the color palette. It contains two fields, one defining which RGB element is selected for the next palette data access, the other defining which of the following XGA palette data update sequences will be followed:

1. Red, Green, Blue
2. Red, Blue, Green, X (where X indicates no access, data is ignored)

In the second case there are four accesses to each update cycle in which the fourth data byte, labelled X, is ignored. If data is being read from the palette, the access labelled X will return the value zero.

The access sequence can be set at any point by setting bits [1:0] to the relevant state (see Table 6.13). The next access to the Palette Data Register will then be directed to the required color. In addition the state of the palette sequence register can be read, in which case the value returned indicates the color that is to be read or written by the next access to Index #X65 (Palette Data).

A write to any of the Palette Index Registers (with or without Prefetch) will reset the state of bits[1:0] to "00".

When the IMS G174 is in VGA mode, bit[2] is ignored if set to "1".

Bit	R/W	Value	Function
1:0	R/W	00	Next palette data access set to R
	R/W	01	Next palette data access set to G
	R/W	10	Next palette data access set to B
	R/W	11	Next palette data access set to X
2	R/W	0	Color order: R,G,B (update),R,G,B (update)...
		1	Color order: R,B,G (update),X,R,B,G (update),X...
7:3			Reserved, write as "0"

Table 6.13 Palette Sequence Register (Index #X66)

Palette Color Registers (Indexes #X67 – #X69)

When color values are written to the IMS G174 they are held in a temporary register while the byte values are compiled to give a complete RGB entry for a palette location. This compiled color value can be read and written independently by the Palette Color Registers.

These registers are particularly useful for providing interrupt support, enabling the exact state of the micro port logic to be reconstructed before the interrupted process is allowed to continue reading from or writing to the device. It is not possible to make use of the automatic palette address incrementing facilities by accessing these registers. Loading a whole palette is performed much more efficiently by using the block write facilities of the Palette Data Register.

If 6-bit operation is selected by the **8/$\overline{6}$** pin being taken low, bits [7:2] are presented to the upper bits of the DAC, with the two lowest bits being held to zero. Bits [1:0] of this register in 6-bit mode can still be accessed but not displayed.

Mode	Bit	R/W	Function
8-bit XGA	7:0	R/W	Palette Data
6-bit XGA	7:2	R/W	Palette Data

Table 6.14 Palette Color Registers (Indexes #X67 – #X69)

6.4 Pixel interface operation

Most pixel interface inputs are latched on the rising edge of the **PClk** input. Inputs are also latched on the falling edge of the **PClk** input if requested by enabling High Color Mode 1 in the Pixel Command Register. Under the control of the Pixel Command Register, the **PixMix** pin and the Cursor Data inputs, very complex images can be displayed by mixing areas of different pixel formats onto the same screen.

Three 16-bit true color formats, a 24-bit true color format and a mixed file format are supported. All these features can be enabled on a pixel boundary by the use of the **PixMix** pin.

6.4.1 The Blank function

As with any industry standard IMS G176 device, a **Blank** input pin is provided which can be used to blank the analogue outputs when this pin is low. A value of zero is applied to the inputs of the DACs regardless of the color value of the current pixel.

An example of such operation can be found in the timing diagram for video operation, Figure 6.5, page 83. The value of **Blank** latched at the input pin is always delayed by the same number of PClks as the pixel input data **P[7:0]**. The timing required on the **Blank** pin are also changed when in High Color Mode 1 to match the different timing constraints on pins **P[7:0]**.

6.4.2 "PixMix™" pixel mixing function

The PixMix pixel mixing function can be achieved either by software or hardware. In software the high color modes are enabled and the mixed file format is used. This format can be enabled by the Pixel Format bits [2:0] being set to 100 in the Pixel Command Register. 16-bit pixel words are assembled at the pixel port from a mixed format datastream applied to the device. Pseudo or true color pixels are displayed according to the value of the MSB of the pixel data. Using this method of software switching, picture-in-picture displays can be generated from existing hardware designs.

In hardware the **PixMix** pin is inverted and logical ORed with the Pixel Select bit (bit [7] in the Pixel Command Register #XE) to enable the high color modes on a pixel by pixel basis. The choice of high color mode 1 or 2 is determined by bit [5] of the Pixel Command Register.

Both methods allow areas of different pixel formats to be displayed on the same screen simultaneously for "picture-in-picture" capability.

6.4.3 High color modes

There are two high color modes which allow multiple byte pixels to be constructed from successive bytes latched on the VGA pixel port pins **P[7:0]**. The resulting pixel data then bypasses the palette and is applied directly to the DACs. These modes enable the user to achieve a greater color resolution (up to 16.7 million colors on a single display screen) while still only using an 8-bit pixel interface.

In any high color mode, the facilities can be switched on or off at a pixel boundary for 2 or 3 pixels or more. This synchronous switching can be done in hardware by using the the **PixMix** pin, as explained above, or in software by using the mixed file format. Asynchronous switching can be achieved using the Pixel Select bit in the Pixel Command Register #XE.

The integrity of the palette contents is always maintained in high color modes, so no rewriting of the palette is required when switching back to pseudo-color VGA operation.

High Color Mode 1

High Color Mode 1 latches data from **P[7:0]** on both the rising and falling edges of **PClk**. The rising edge latches byte[0] and the falling edge latches byte[1].

Only 16-bit pixels can be accumulated in this way as the DAC outputs can only change following a rising edge of **PClk**.

The Pixel Command Register bits 3, 4 and 6 specify the format of the resulting 16-bit true color pixel.

In both high color modes, if the **PixMix** pin is latched High on the rising edge of **PClk**, the high color mode is disabled for that pixel, and the single byte data **P[7:0]** is used as a normal VGA

address to the Color Palette. This is shown in Figure 6.1. This mode allows a pixel by pixel selection of 16-bit and 8-bit images on a single screen while still only using an 8-bit pixel interface.

The pixel set-up and hold times on all pixel inputs are modified when in High Color Mode 1 (see Figure 6.6, page 83). This also includes the control inputs **Blank**, **PixMix**, and cursor data **CD[1:0]**. It is not possible to change the pixel interface timing on a pixel-by-pixel basis. If it is required to use **PixMix** to switch in and out of High Color Mode 1 synchronously, bit [0] of the Pixel Command Register must be set to 1. This forces the pixel interface to adhere to the modified mode 1 timings under all conditions, allowing synchronous switching between High Color Mode 1 and standard VGA mode.

If the modified timing is not used throughout, and it is required to preserve the palette contents when switching to High Color Mode 1, the pixel port **P[7:0]** must be held to a valid state for 5 PClk periods before and after the switch. This allows the pixel interface to reconfigure to the modified timing. If High Color Mode 1 is used exclusively, this reconfiguration period is not required. Note that High Color Mode 1 is only available at a reduced **PClk** rate.

High Color Mode 2

High Color Mode 2 latches data from **P[7:0]** on just the rising edges of **PClk** until the full pixel depth has accumulated. Normal pixel timings are adhered to, with the advantage that a high speed **PClk** input is allowed. This in turn means that an existing system does not have to undergo redesigned pixel timing to benefit from the greater color resolution.

A further advantage is that 24-bit pixels can be accumulated giving a 24-bit true color capability to high color. Either two or three successive edges of **PClk** are used to accumulate the **P[7:0]** data to make a 16 or 24-bit pixel, depending on bits 3, 4 and 6 in the Pixel Command Register.

Because Mode 2 inherently uses subsampling, a 16-bit display is produced at one half the full rate **PClk** input frequency, and a 24-bit display at one third the full rate **PClk** frequency (this is shown in Figure 6.2). Therefore the resulting true color pixel will be displayed for two or three full rate **PClk** periods.

Because the input **PClk** is still operating at the full rate, the high color mode can be disabled revealing a VGA image that is still operating at the full pixel rate. This provides a VGA image and a reduced resolution 24-bit true color image on the same screen.

The above descriptions are summarized in Table 6.15.

Pixel Format bits[1] [2:0]	Pixel Command Register bit 5	High color modes enabled?	Function
XXX	X	N	**P[7:0]** used as VGA palette address
000	X	Y	True color data is [xRRRRRGG.GGGBBBBB]
001	0	Y	Reserved[2]
001	1	Y	True color data is [RRRRRRRR.GGGGGGGG.BBBBBBBB]
010	X	Y	True color data is [RRRRRGGG.GGGBBBBB]
011	X	Y	True color data is [RRRRRRGG.GGGGBBBB]
100	X	Y	True color data, software PixMix if bit15=0 is [0xxxxxxx.–VGA–] if bit15= 1 is [1RRRRRGG.GGGBBBBB]
101	X	Y	Reserved
110	X	Y	Reserved
111	X	Y	Reserved
1. Pixel Format bits are bits 3, 6 and 4 of the Pixel Command Register			
2. 24-bit high color is not available in High Color Mode 1			

Table 6.15 Pixel interface modes

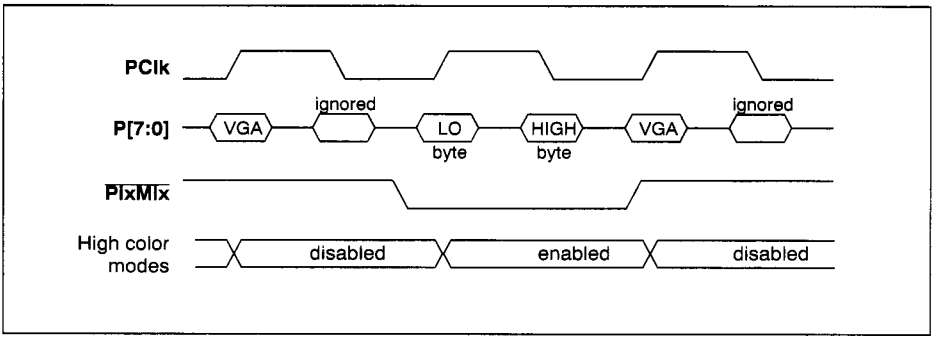


Figure 6.1 High Color Mode 1 operation

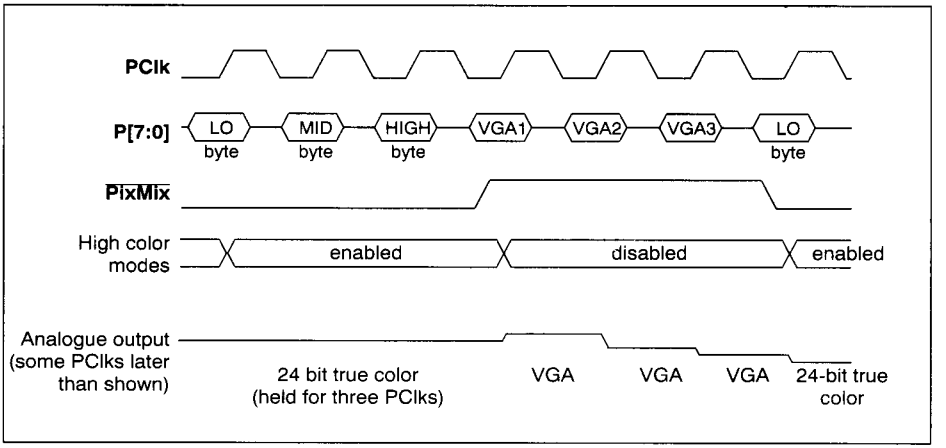


Figure 6.2 High Color Mode 2 operation (with 24 bit per pixel format)

6.5 Cursor Data inputs

The Cursor Data inputs to the IMS G174, **CD[1:0]**, are latched by **PClk** in the same way as the rest of the Pixel Interface. These values are displayed in preference to a palette color or a true color pixel according to the convention shown in Table 6.16.

CD[1:0]	Cursor Function
00	Cursor color[0]
01	Cursor color[1]
10	Transparent (palette or true color)
11	Complement (of palette or true color)

Table 6.16 Cursor Data Inputs

Transparent is used when it is required to display the overlaid palette or true color pixel within the block defining the cursor. Complement is used to generate the complement (all bits inverted) of the overlaid pixel. This ensures that cursor pixels programmed with this value will always be visible, whatever the overlaid color.

6.6 Timing reference guide

6.6.1 Micro port timing

Symbol	Parameter	Min.	Max.	Units	Notes
tWLWH	**WR** pulse width low	50		ns	
tRLRH	**RD** pulse width low	50		ns	
tWHWL	**WR** pulse width high	6×tCHCH +40ns		ns	
tRHWL	**RD** pulse width high	6×tCHCH +40ns		ns	
tSVWL	**RS** setup time	10		ns	
tSVRL	**RS** setup time	10		ns	
tWLSX	**RS** hold time	10		ns	
tRLSX	**RS** hold time	10		ns	
tDVWH	Write data setup time	10		ns	
tWHDX	Write data hold time	10		ns	
tRLQX	Output turn–on delay	5		ns	
tRLQV	Read enable access time		40	ns	
tRHQX	Output hold time	5		ns	
tRHQZ	Output turn–off delay		20	ns	1
tWHWL1	Successive write interval				
tWHRL1	Write followed by read interval				
tRHRL1	Successive read interval				
tRHWL1	Read followed by write interval	4×tCHCH +30ns		ns	2
tWHWL2	Write after color write				
tWHRL2	Read after color write				
tRHWL2	Write after color read				
tRHRL2	Read after color read	6×tCHCH +40ns		ns	2
tWHRL3	Read after read address write				
tCYC	Write/Read cycle time	6×tCHCH +40ns		ns	2,3
	Write/Read enable transition time		50	ns	

Table 6.17 Micro port timing parameters

Notes

1 Measured ±200mV from steady output voltage.

2 These parameters allow for synchronization between operations on the micro port and the pixel stream being processed by the color look–up table.

3 From the rising edge of Read or Write pulse to the rising edge of the next Read or Write pulse.

Operations on the micro port are internally synchronized to the pixel clock in the periods between cycles. This is the reason for the time between cycles on the micro port being specified in terms of pixel clock periods.

The minimum cycle time for all accesses (defined as the period between successive rising edges of the read or write strobe) is 6×tCHCH +40ns.

For example, in the case of a 25MHz system the pixel clock period (tCHCH) would be 40ns and the minimum cycle time for accesses on the microprocessor port is:

6×40ns + 40ns = 280ns

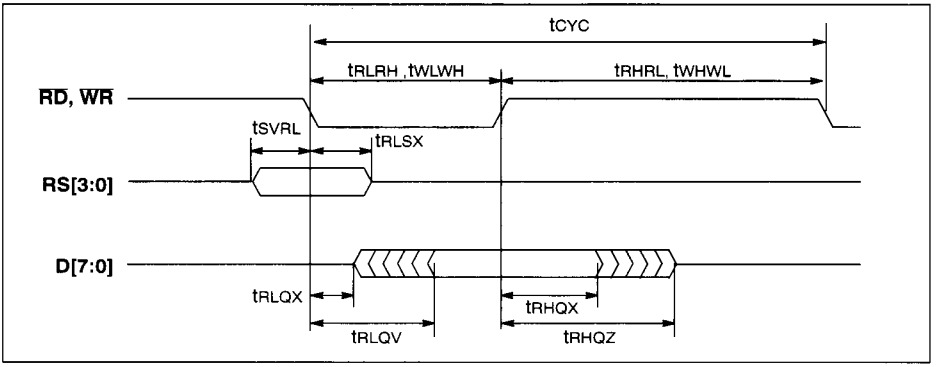


Figure 6.3 Basic read/write cycle

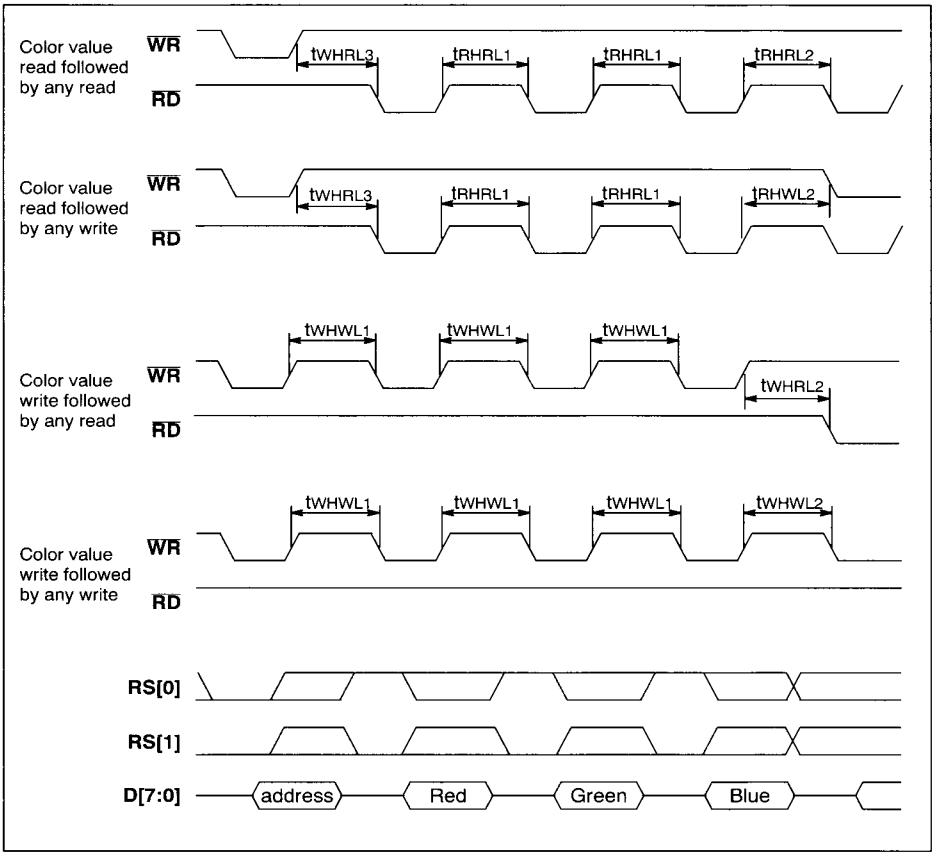


Figure 6.4 Color value read and write accesses

6.6.2 Video operation

Symbol	Parameter	66MHz Min.	85MHz Min.	All Max.	Units	Notes
tCHCH	**PClk** period	15.1	11.8	10000	ns	
ΔtCHCH	**PClk** jitter			±2.5	%	1
tCLCH	**PClk** width low	5	5	10000	ns	
tCHCL	**PClk** width high	5	5	10000	ns	
tPVCH	Pixel interface set–up time	3	3		ns	2, 3
tCHPX	Pixel interface hold time	3	3		ns	2, 3
tCHAV	**PClk** to valid DAC output	5	5	30	ns	4
ΔtCHAV	Differential output delay			2	ns	5
	Pixel clock transition time			50	ns	
tCHCH(D)	**PClk** period	20	20	10000	ns	6
tCLCH(D)	**PClk** width low	8	8		ns	6
tCHCL(D)	**PClk** width high	8	8		ns	6
tPVCH(D)	Pixel Interface set-up time	–1	–1		ns	2, 3, 6
tCHPX(D)	Pixel Interface hold time	7	7		ns	2, 3, 6

Table 6.18 Video operation timing parameters

Notes

1 This parameter allows for variation in the Pixel Clock frequency, but does not permit the Pixel Clock period to vary outside the minimum and maximum values for Pixel Clock (tCHCH) period specified above.

2 These parameters apply to the **$\overline{\text{Blank}}$**, **CD[1:0]**, **$\overline{\text{PixMix}}$** and **P[7:0]** pins.

3 The Pixel Address input to the color look–up table must be set up as a valid logic level with the appropriate setup and hold times to each rising edge of **PClk** (this requirement must be met during the blanking period).

4 A valid analogue output is defined as when the changing analogue signal is half way between its successive values. This parameter is stable with time but can vary between different devices and may vary with different DC operating conditions.

5 Between different analogue outputs on the same device.

6 (D) indicates the modified value of a parameter when the IMS G174 is in High Color Mode 1 and is using both edges of **PClk** to latch data. If the palette contents are to be preserved during the switch to High Color Mode 1, the pixel inputs P[7:0] must be held to a valid state for five **PClk** periods before and after the transition. This is not required if Mode 1 is used exclusively.

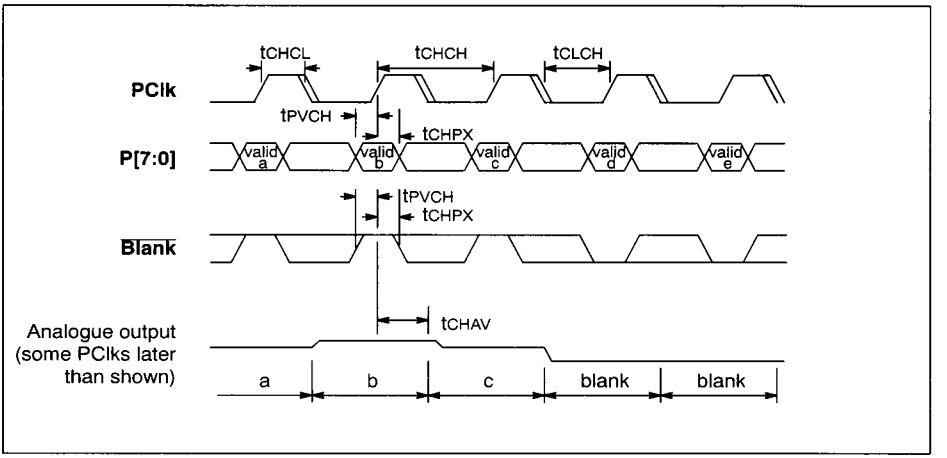


Figure 6.5 Video operation

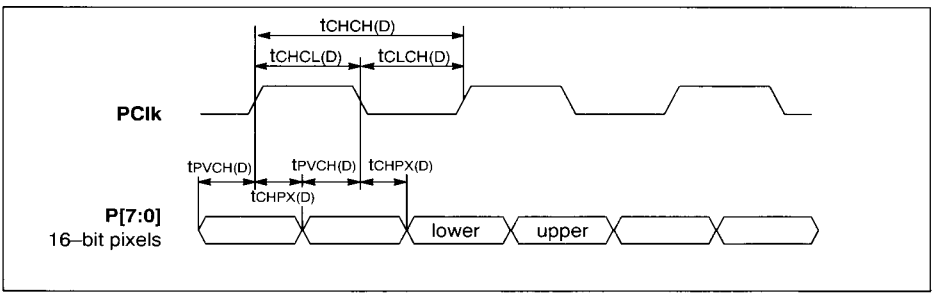


Figure 6.6 Pixel Interface (High Color Mode 1)

6.7 Electrical specifications

6.7.1 Absolute maximum ratings*

Symbol	Parameter	Min.	Max.	Units	Notes
Vdd/AVdd	DC supply voltage		7.0	V	
	Voltage on input and output pins	Gnd–1.0	Vdd+0.5	V	
TS	Storage temperature (ambient)	–55	125	°C	
TA	Temperature under bias	–40	85	°C	
PDmax	Power dissipation		1.5	W	
	Reference current	–15		mA	
	Analogue output current (per output)		45	mA	
	DC digital output current		25	mA	

Notes

*Stresses greater than those listed under 'Absolute maximum ratings' may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

6.7.2 DC operating conditions

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
Vdd	Positive supply voltage	4.75	5.0	5.25	V	1, 2, 3
Gnd	Ground		0		V	1
VIH	Input logic '1' voltage	2.0		Vdd+0.5	V	1, 3
VIL	Input logic '0' voltage	–0.5		0.8	V	1, 4
TC	Case temperature	0		70	°C	1
Iref	Reference current	–6.0		–10	mA	1, 5

Notes

1 All voltages are with respect to Gnd unless specified otherwise.

2 This parameter allows for a range of fixed power supply voltages to be used; it does not imply that the supply voltage should be allowed to vary dynamically within these limits.

3 These voltage ranges apply equally for AVdd and Vdd.

4 VIL(min) = –1.0V for a pulse width not exceeding 25% of the duty cycle (t_{CHCH}) or 10ns, whichever is the smaller value.

5 Reference currents below the minimum specified may cause the analogue outputs to become invalid.

6.7.3 DC electrical characteristics

Symbol	Parameter	Min.	Max.	Units	Notes
Idd	Average power supply current		250	mA	4
Vref	Voltage at **Iref** pin	Vdd–3	Vdd	volts	5
IIN	Digital input current		±10	µA	6,7
IINR	Digital input current		±100	µA	6,8
IOZ	Off state digital output current		±50	µA	6,9
VOH	Output logic '1'	2.4		V	IO = 5mA
VOL	Output logic '0'		0.4	V	IO = –5mA

Notes (Notes 1–3 apply to all parameters)

1 All voltages are with respect to Gnd unless specified otherwise.

2 The Pixel Clock frequency must be stable for a period of at least 20µs after power-up (or after change in a Pixel Clock frequency) before proper device operation is guaranteed.

3 Over the range of the DC operating conditions unless specified otherwise.

4 IO = IO(max). Idd is dependent on digital loading and cycle rate, the specified values are obtained with the outputs unloaded and at the maximum rated Pixel Clock frequency.

5 These voltages apply equally for AVdd and Vdd.

6 Vdd = max, Gnd ≤ VIN ≤ Vdd.

7 On digital inputs (**P[7:0]**, **PClk**, **$\overline{\text{RD}}$**, **$\overline{\text{Blank}}$**, **$\overline{\text{WR}}$**, **$\overline{\text{PixMix}}$** and **RS[1:0]**).

8 On digital inputs (**$\overline{\text{VSync}}$**, **RS[3:2]**, **CD[1:0]**)

9 On digital input/output (**D[7:0]**).

6.7.4 DAC Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
	Resolution	6		8	bits	
VO(max)	Output voltage			1.5	V	IO≤10mA
IO(max)	Maximum output current			–21	mA	VO≤1V
IO	Full scale output current	–16.74	–17.62	–18.50	mA	4
IO	Full scale output current	–17.72	–18.65	–19.58	mA	5
K	DAC gain constant		2.10			6
	Full scale error		±2.5	±5	%	7
	DAC to DAC correlation error		±1	±2.5	%	8
	Rise time (10% to 90%)		2	5	ns	9
	Full scale settling time		12.5		ns	9 ,11,12
	Integral linearity (8-bit)		±0.5	±1	LSB	10
	Integral linearity (6-bit)		±0.25	±0.5	LSB	10
	Differential linearity (8-bit)		±0.25	±1	LSB	10
	Differential linearity (6-bit)		±0.25	±0.5	LSB	10
	Monotonicity	guaranteed				
	Glitch energy		120		pVsec	9, 12

Table 6.19 DAC Characteristics

Notes (Notes 1–3 apply to all parameters)

1 All voltages are with respect to Gnd unless specified otherwise.

2 The Pixel Clock frequency must be stable for a period of at least 20µs after power-up (or after change in a Pixel Clock frequency) before proper device operation is guaranteed.

3 Tested over the operating temperature range and at nominal supply voltage with Iref = –8.88mA.

4 Using Iref = –8.39mA

5 Using Iref = –8.88mA

6 IO = K × Iref

7 Full scale error from the value predicted by the DAC gain constant, K.

8 About the mid point of the distribution of the three DACs measured at full scale deflection.

9 Load = 37.5Ω + 30pF with **Iref** = –8.88mA.

10 Linearity measured from the best fit line through the DAC characteristic. Monotonicity guaranteed.

11 From a 2% change in the output voltage until settling to within 2% of the final value.

12 This parameter is sampled, not 100% tested.

6.7.5 AC test conditions

Parameter	
Input pulse levels	Gnd to 3V
Typical input rise and fall times (10% to 90%)	3ns
Digital input timing reference level	1.5V
Digital output timing reference level	0.8V and 2.4V
Digital output load	see Figure 6.7

Table 6.20 AC test conditions

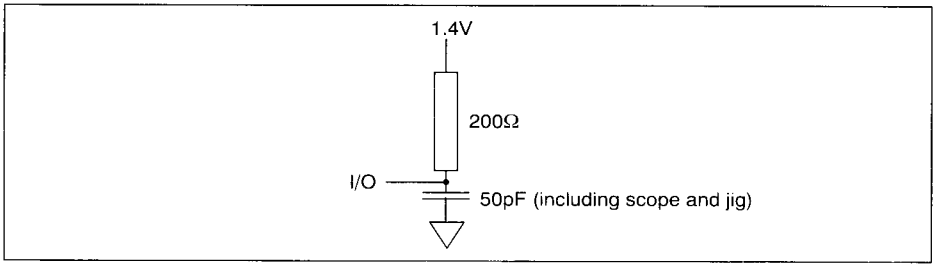


Figure 6.7 Digital output load

6.7.6 Capacitance

Symbol	Parameter	Min.	Max.	Units	Notes
CI	Digital input		7	pF	1, 2
CO	Digital output		7	pF	1, 2, 3
COA	Analogue output		10	pF	1, 2 ,4

Table 6.21 Capacitance values

Notes

1 These parameters are sampled, not 100% tested.

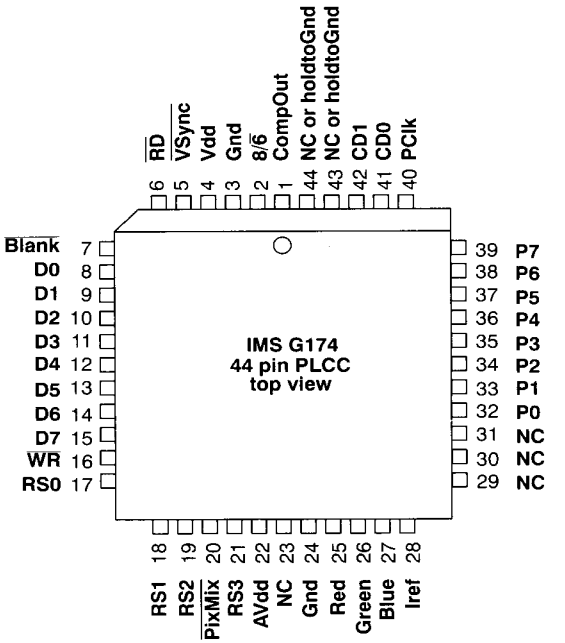
2 Measured on a Boonton meter.

3 $\overline{\textbf{RD}}$ ≥ VIH(min) to disable **D[7:0]**

4 $\overline{\textbf{Blank}}$ ≤ VIL(max) to disable **Red**, **Green** and **Blue**.

6.8 Package specifications

44 pin plastic leaded-chip-carrier package

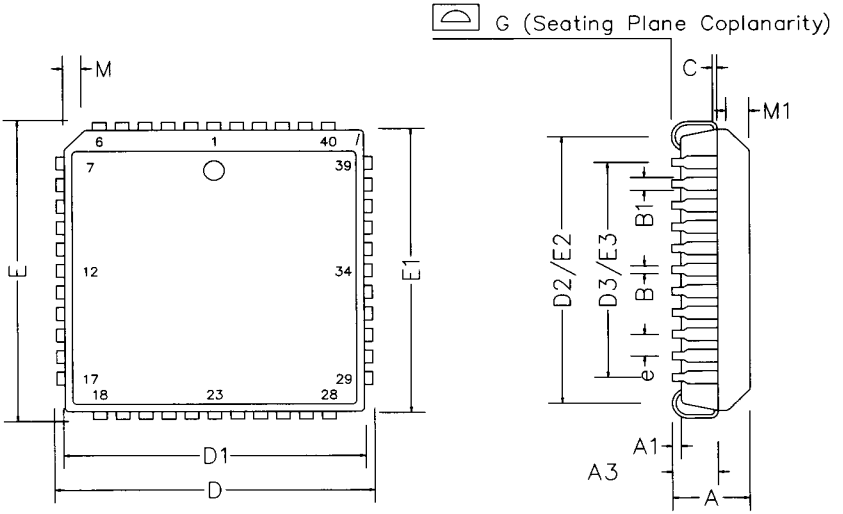


Note

All **Vdd** pins **must** be connected to the 5 Volt power supply.
All **Gnd** pins **must** be connected to ground.

Figure 6.8 IMS G174 44 pin PLCC J-bend package pinout

DIM	CONTROL DIMENSIONS INCH			ALTERNATIVE DIMENSIONS mm		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.165	0.170	0.180	4.191	4.318	4.572
A1	0.020	–	–	0.508	–	–
A3	0.095	–	0.110	2.413	–	2.794
B	0.013	–	0.023	0.330	–	0.584
B1	0.025	–	0.035	0.635	–	0.889
C	0.0095	0.010	0.0105	0.241	0.254	0.267
D	0.685	0.690	0.695	17.399	17.526	17.653
D1	0.650	0.655	0.660	16.510	16.637	16.764
D2	0.590	0.610	0.630	14.986	15.494	16.002
D3	–	0.500REF	–	–	12.700REF	–
E	0.685	0.690	0.695	17.399	17.526	17.653
E1	0.650	0.655	0.660	16.510	16.637	16.764
E2	0.590	0.610	0.630	14.986	15.494	16.002
E3	–	0.500REF	–	–	12.700REF	–
e	–	0.050BSC	–	–	1.270BSC	–
G	–	–	0.004	–	–	0.102
L	–	N/A	–	–	N/A	–
L1	–	N/A	–	–	N/A	–
M	0.042	–	0.048	1.067	–	1.219
M1	0.042	–	0.056	1.067	–	1.422



Notes;

1. Maximum lead displacement from notional centre line = ±0.007".

Figure 6.9 IMS G174 44 pin PLCC J-bend package dimensions

6.9 Ordering information

Device	Clock rate	Package	Part number
IMS G174	66MHz	44 pin plastic LCC	IMS G174JI66Z
IMS G174	85MHz	44 pin plastic LCC	IMS G174JI85Z