8BIT 40MSPS ADC BW1223X

GENERAL DESCRIPTION

The BW1223X is a CMOS 8-bit A/D converter for video applications. It is a two-step ping-pong A/D converter which consists of reference resistor-matrix, 4-bit coarse and fine A/D converters.
The maximum conversion rate of BW1223X is 30MSPS and supply voltage is 3.3V single.

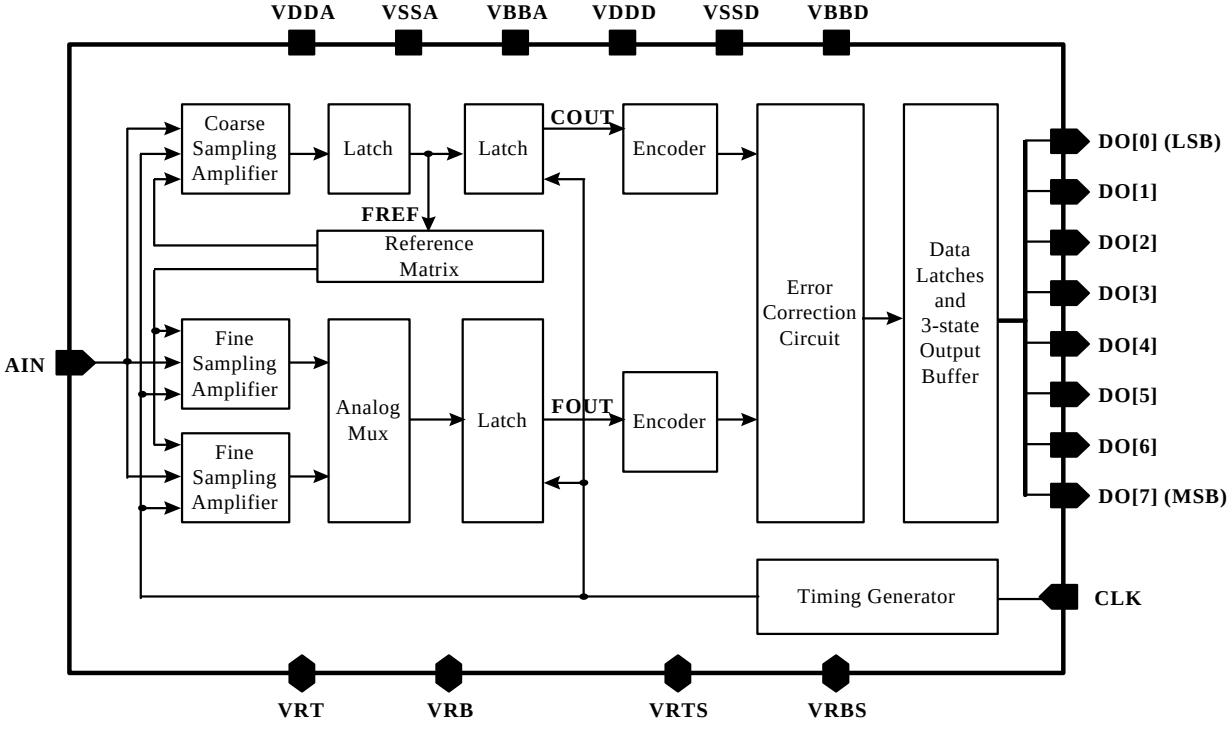
FEATURES

- **Process : CMOS**
- **Resolution : 8Bit**
- **Maximum Conversion Rate : 40MSPS**
- **Power Supply : 3.3V Single**
- **Power Consumption : 60mW**
- **Differential Linearity Error : ±0.3 LSB (Typ)**
- **Integral Linearity Error : ±0.5 LSB (Typ)**
- **On-Chip Reference Bias Resistors**
- **Reference Bias Adjustable Externally**

TYPICAL APPLICATIONS

- Multi-media Applications
- Frame-grabber Scanner
- Camcorder
- Digital Video (TV/VCR)
- Broadcasting and Studio Equipments.
- Medical Electronics (ultra-sound and imaging)
- High Speed Instruments (digital scope, radar)

FUNCTIONAL BLOCK DIAGRAM



CORE PIN DESCRIPTION

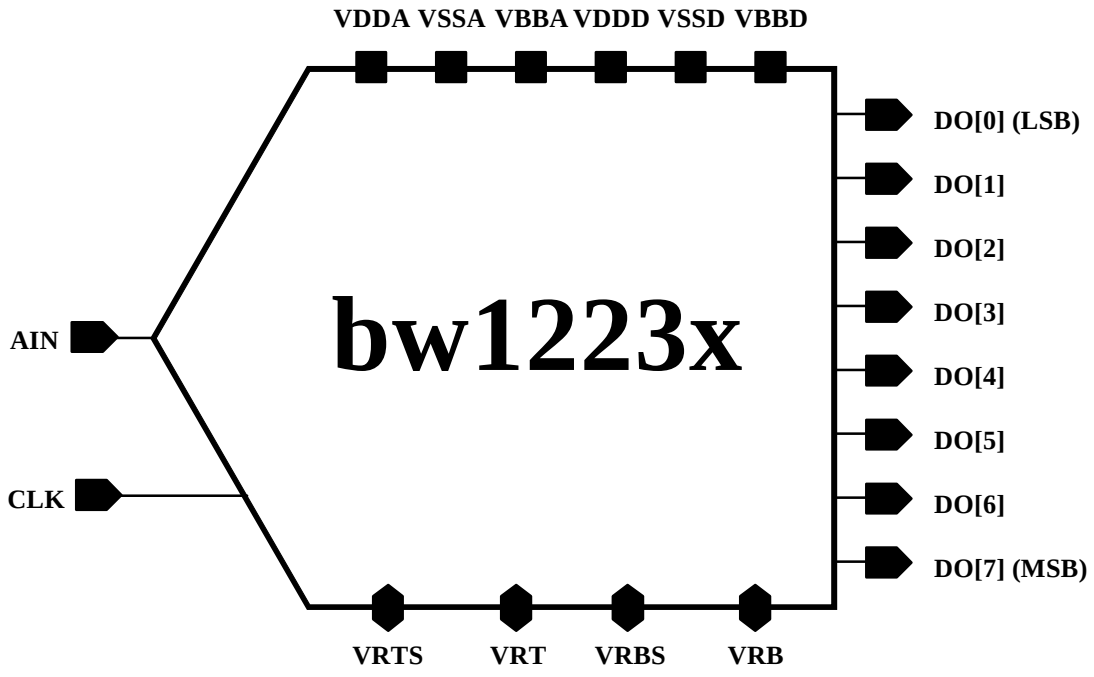
NAME	I/O TYPE	I/O PAD	PIN DESCRIPTION
VRTS	AB	poa_bb	Internal Reference Top Bias (Short to VRTS for Self-Bias)
VRT	AB	poa_bb	2.6V External Reference Top Bias
VRBS	AB	poa_bb	Internal Reference Bottom Bias (Short to VRBS for Self-Bias)
VRB	AB	poa_bb	0.6V External Reference Bottom Bias
VDDA	AP	vdda	+3.3V Analog Power.
VBBA	AG	vbba	Analog Sub Bias.
VSSA	AG	vssa	Analog Ground.
AIN	AI	piar10_bb	Analog Input Input Span : VRB ~ VRT
CLK	DI	picc_bb	Clock Input
DO[7:0]	DO	pot2_bb	Digital Output
VBBD	DG	vbba	Digital Sub Bias.
VSSD	DG	vsstd	Digital Ground.
VDDD	DP	vddd	Digital Power.

I/O TYPE ABBR.

- AI : Analog Input
- DI : Digital Input
- AO : Analog Output
- DO : Digital Output
- AB : Analog Bidirectional
- DB : Digital Bidirectional

- AP : Analog Power
- DP : Digital Power
- AG : Analog Ground
- DG : Digital Ground

CORE CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Characteristics	Symbol	Value	Unit
Supply Voltage	VDD	-0.3 to 4.5	V
Analog Input Voltage	AIN	-0.3 to VDD+0.3	V
Digital Input Voltage	CLK	-0.3 to VDD+0.3	V
Digital Output Voltage	V_{OH}, V_{OL}	-0.3 to VDD+0.3	V
Reference Voltage	VRT/VRB	-0.3 to VDD+0.3	V
Storage Temperature Range	T_{stg}	-45 to 125	°C

NOTES

1. ABSOLUTE MAXIMUM RATING specifies the values beyond which the device may be damaged permanently. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect reliability. Each condition value is applied with the other values kept within the following operating conditions and function operation under any of these conditions is not implied.
2. All voltages are measured with respect to VSS unless otherwise specified.
3. 100pF capacitor is discharged through a 1.5kΩ resistor (Human body model)

RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Min	Typ	Max	Unit
Supply Voltage	VDDA - VSSA VDDD - VSSD	3.15	3.3	3.45	V
Supply Voltage Difference	VDDA - VDDD	-0.1	0.0	0.1	V
Reference Input Voltage	VRT VRB	- -	2.6 0.6	- -	V
Analog Input Voltage	AIN	VRB	-	VRT	V
Clock High Time Clock Low Time	T_{pwh} T_{pwl}	- -	16.6 16.6	- -	ns
Digital Input 'L' Voltage Digital Input 'H' Voltage	V_{IL} V_{IH}	- 3.0	- -	0.3 -	V
Operating Temperature	T_{opr}	0	-	70	°C

NOTES

1. It is strongly recommended that all the supply pins (VDDA, VDDD, VDDP) be powered from the same source to avoid power latch-up.

DC ELECTRICAL CHARACTERISTICS

Characteristics	Symbol	Min	Typ	Max	Unit	Conditions
Resolution	-	-	8	-	Bits	-
Reference Current	IREF	-	6.25	-	mA	VRT : 2.6V VRB : 0.6V
Differential Linearity Error	DLE	-	±0.3	±0.5	LSB	AIN : 0.6 ~ 2.6V (Ramp Input) F_s : 1MHz 20MHz
Integral Linearity Error	ILE	-	±0.5	±0.8	LSB	
Bottom Offset Voltage Error	EOB	-	±6.3	±6.5	LSB	EOB = AIN(0,1) - VRB
Top Offset Voltage Error	EOT	-	±5.4	±5.6	LSB	EOT = VRT - AIN(254,255)

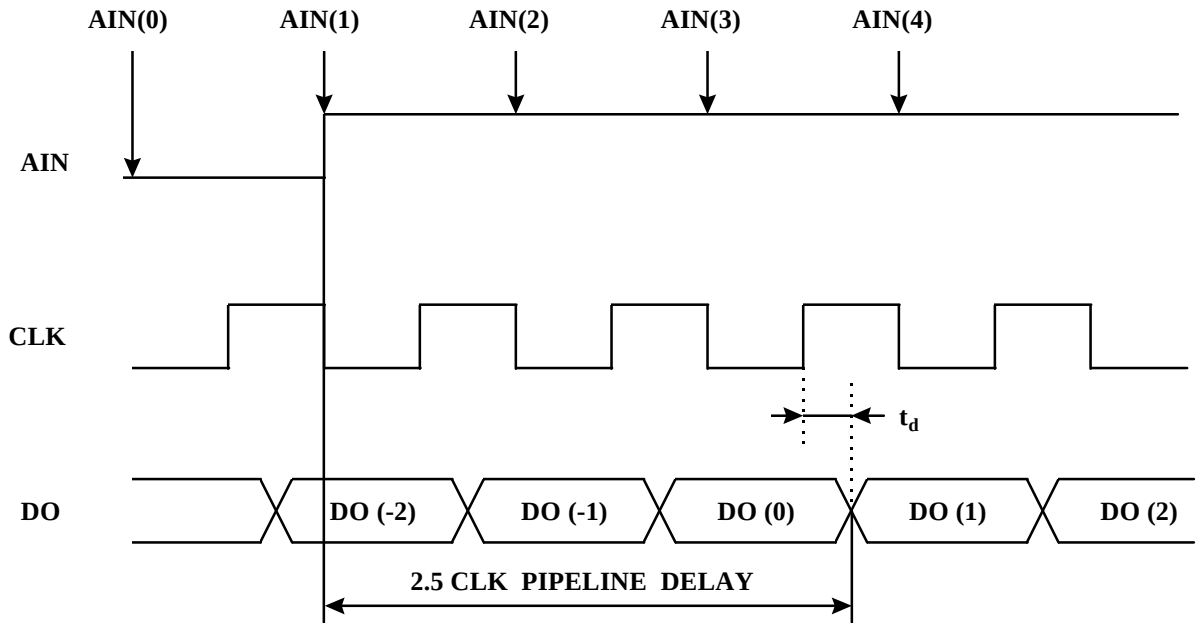
NOTES

1. Converter Specifications (unless otherwise specified)
   VDDA=3.3V VDDD=3.3V
   VSSA=GND VSSD=GND
   VRT=2.6V VRB=0.6V
   Ta=25°C
2. TBD : To Be Determined

AC ELECTRICAL CHARACTERISTICS

Characteristics	Symbol	Min	Typ	Max	Unit	Conditions
Clock High Time	T_{pwh}	-	16.6	-	ns	-
Clock Low Time	T_{pwl}	-	16.6	-	ns	
Conversion Rate	F_s	40	-	-	MSPS	
Dynamic Supply Current	I_s (IREF)	-	20 (6.25)	-	mA	I_s = I(VDDA) + I(VDDD) + IREF F_s : 40MHz
Digital Output Data Delay	t_d	-	10	20	ns	See "DELAY TIMING DIAGRAM"
Signal to Noise Distortion Ratio (SNDR)	SNR1 SNR2 SNR3	38	42 42 42	-	dB	AIN : 1, 2, 4MHz respectively (Sine Input) F_s : 40MHz

DELAY TIMING DIAGRAM



FUNCTIONAL DESCRIPTION

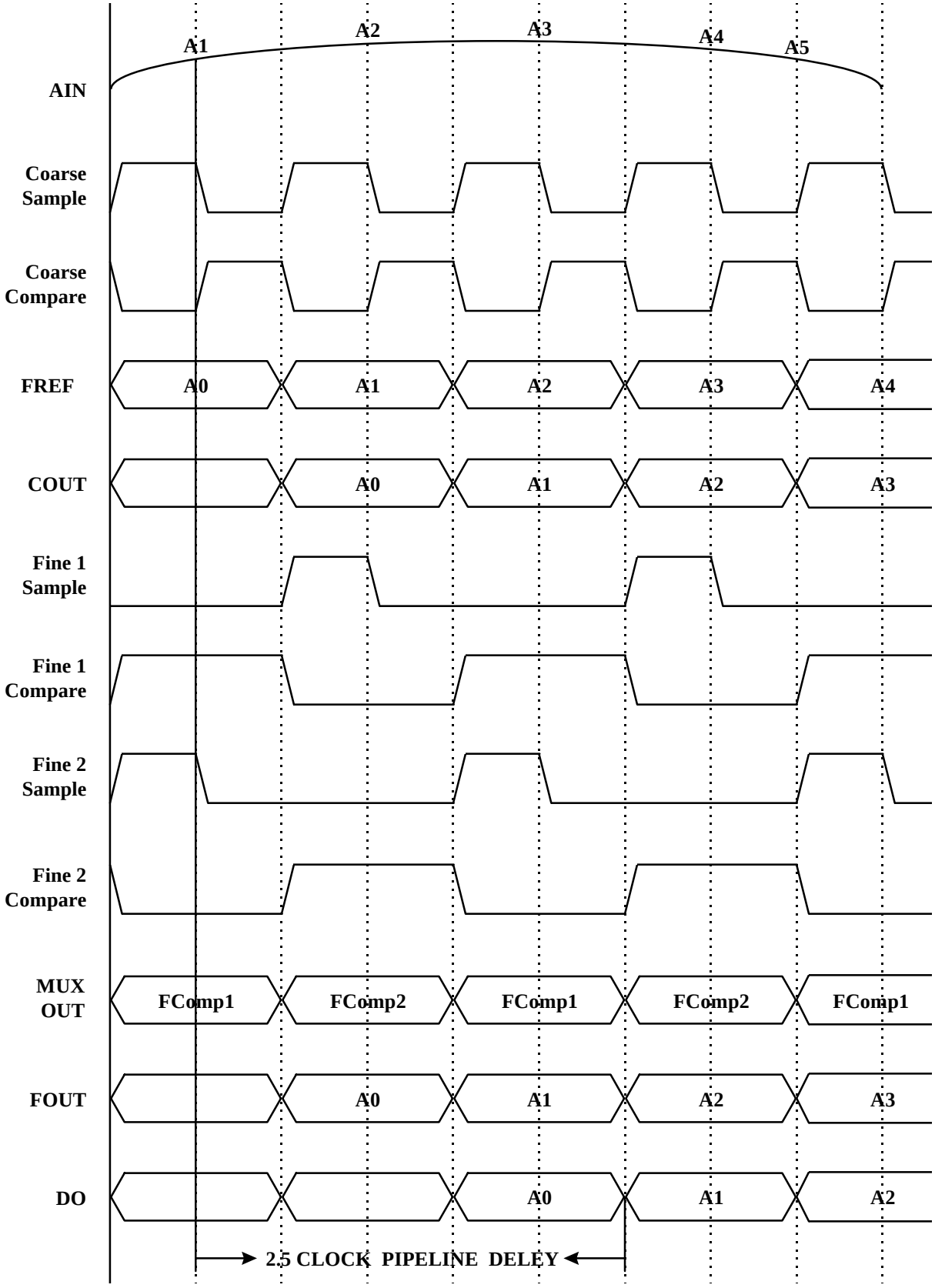
1. BW1223X is a two-step ping-pong A/D converter with subranging reference resistor matrix.
   It consists of 4-bit coarse A/D converter and fine A/D converter of which the accuracy is 4.459 bits. The latching comparators in coarse and fine A/D converters have offset cancellation features built in such as auto-zero and averaging, and the number of comparators are 15 in the coarse converter and 42 in the fine one.
   The sampling operation of fine A/D converter is performed, through 21 analog MUXs, in a ping-pong manner between the two sampling amplifier banks each of which consists of 21 latching comparators.

2. The reference resistor matrix switch one of the 16 different sets of reference voltages, according to the states of the coarse comparator digital outputs, to the fine sampling amplifier banks. This fact and the use of a CMOS auto-zero comparator surely eliminate the extra pain for implementing high accuracy D/A converter of 8 bits or more, and thus a low-power, high-performance and high speed A/D converter results.

3. The operation of BW1223X can be stated as follows. (refer to the 'TIMING DIAGRAM' that follows)
   During the first cycle of external clock, the analog input 'AIN' is traced by each converter, and at the falling edge of CLK the 'AIN' is sampled and held to be compared with the 16-level coarse reference voltages. The result of comparison in coarse comparator, 'COUT', is latched and used to select a set of fine reference voltage 'FREF' which, to be compared with the sampled analog input, is fed to the fine sampling amplifier banks. The result of the comparison is reproduced by successive comparators with sufficiently large gain and then multiplexed to the latching digital logic in a ping-pong manner. Latching logic in coarse and fine converters refine the results of comparison to generate A/D converter output 'FOUT' and 'COUT', and from which the final digital output 'DO' is generated.
   The overall pipeline delay, measured from the sampling instance to the time that the 'DO' comes to be available, is 2.5 clock cycles.

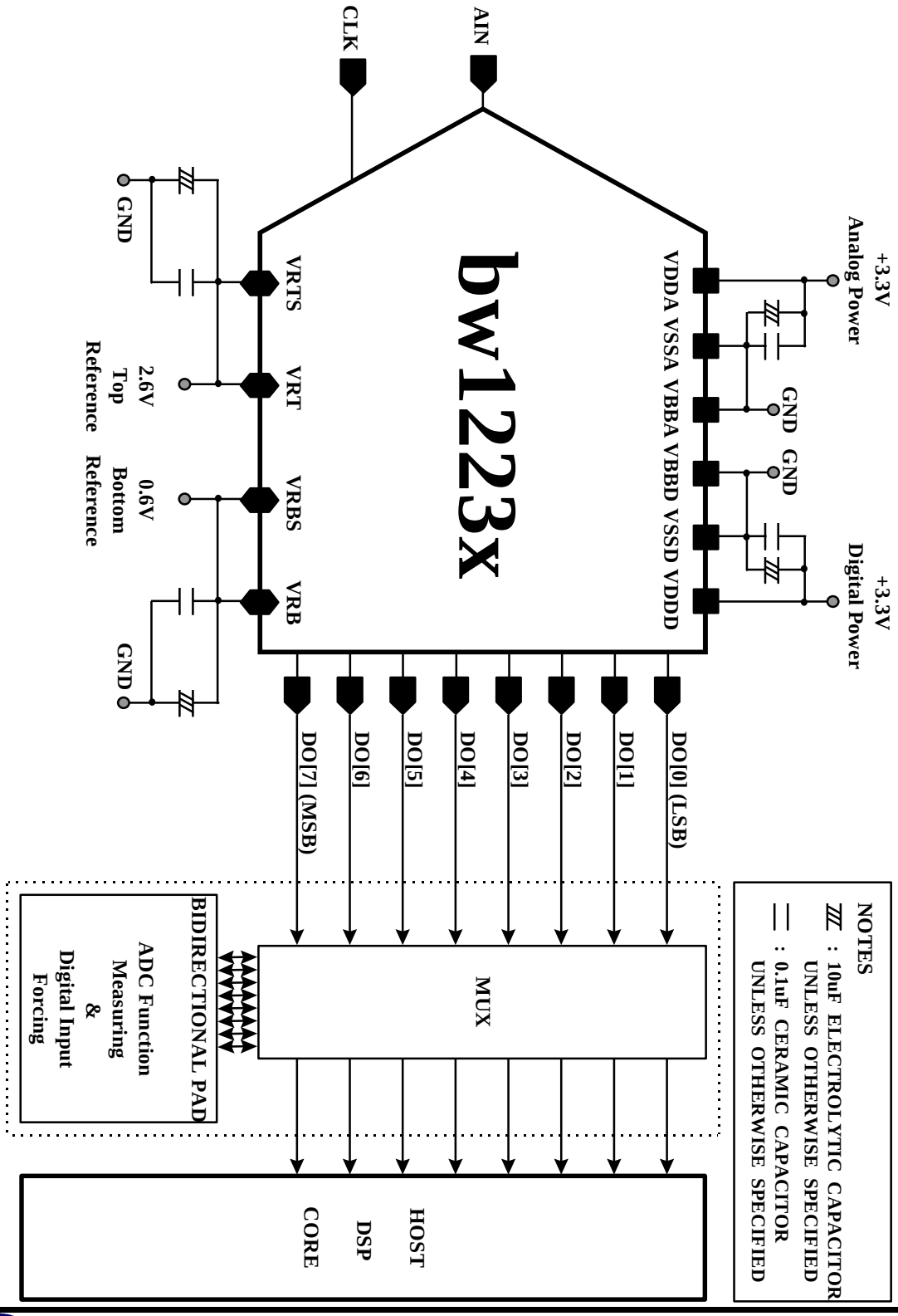
4. BW1223X implements the error correction scheme to correct the error which stems from the mismatch between the offset of coarse A/D converter and that of the fine A/D converter. This scheme can handle coarse comparator offset error up to 3 LSBs and helps reducing the differential linearity error consequently.

TIMING DIAGRAM

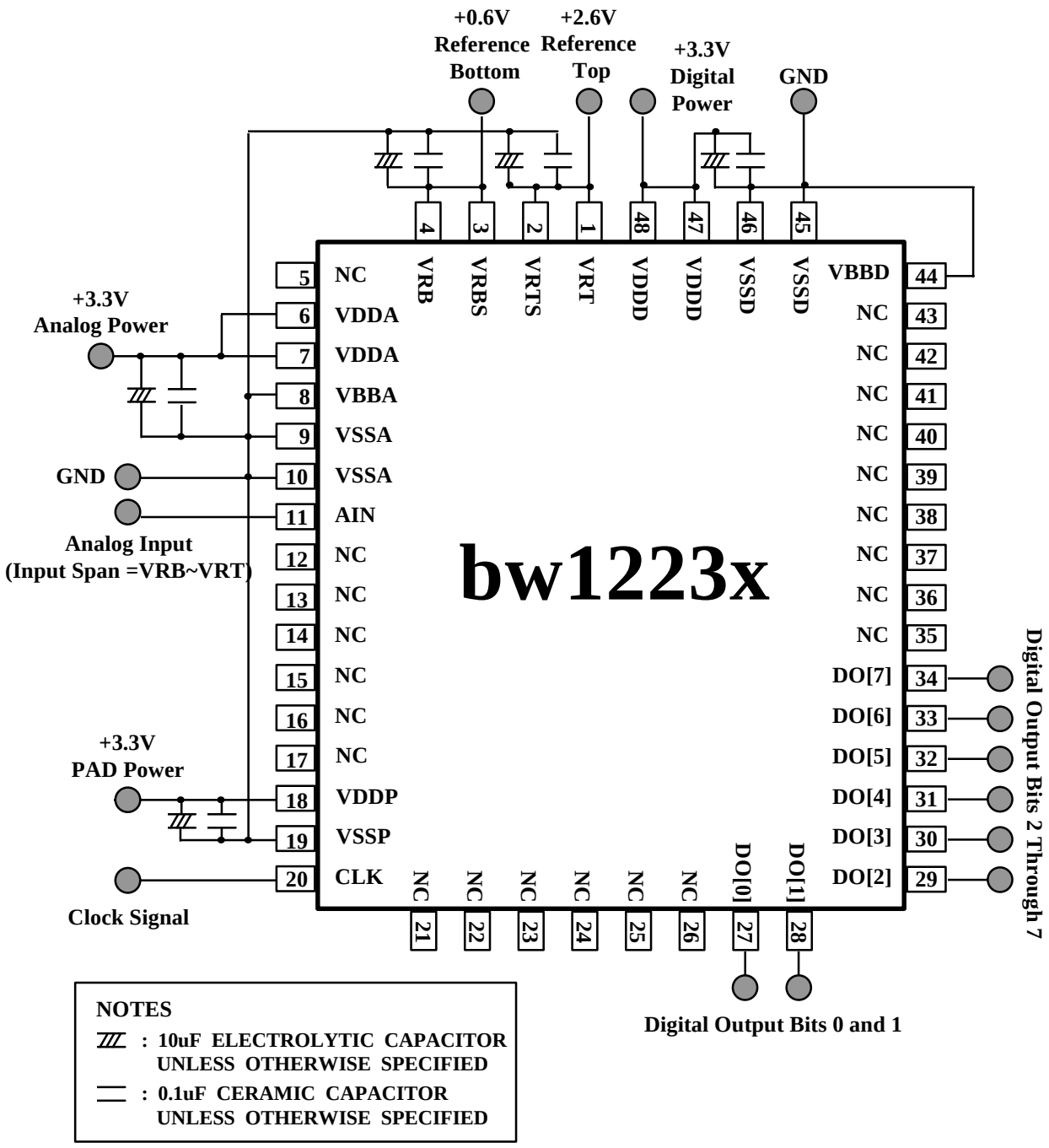


CORE EVALUATION GUIDE

1. ADC function is evaluated by external check on the bidirectional pads connected to input nodes of HOST DSP back-end circuit.
2. The reference voltages may be biased externally through VRT and VRB pins, otherwise these voltages are internally generated with VRT and VRB shorted to VRTS and VRBS respectively.



PACKAGE CONFIGURATION



NOTES

1. You can test ADC function by checking external bidirectional pad connected to internal signal path.
2. ESD (ElectroStatic Discharge) sensitive device. Although the digital control inputs are diode protected, permanent damage may occur on devices subjected to high electrostatic discharges. It is recommended that unused devices be stored in conductive foam or shunts to avoid performance degradation or loss of functionality. The protective foam should be discharged to the destination socket before devices are inserted.
3. NC denotes "No Connection".

PACKAGE PIN DESCRIPTION

NAME	PIN NO.	I/O TYPE	PIN DESCRIPTION
VRT	1	AB	+2.6V External Reference Top Bias.
VRTS	2	AB	Internal Reference Top Bias. (Short to VRTS for Self-Bias.)
VRBS	3	AB	Internal Reference Bottom Bias. (Short to VRBS for Self-Bias.)
VRB	4	AB	+0.6V External Reference Bottom Bias.
NC	5	-	No Connection
VDDA	6, 7	AP	+3.3V Analog Power.
VBBA	8	AG	Analog Sub Bias.
VSSA	9, 10	AG	Analog Ground.
AIN	11	AI	Analog Input. Input Span = VRT ~ VRB.
NC	12~17	-	No Connection
VDDP	18	DP	PAD Power
VSSP	19	DG	PAD Ground
CLK	20	DI	Clock Input.
NC	21~26	-	No Connection
DO[7:0]	34~27	DO	Digital Output.
NC	35~43	-	No Connection
VBBD	44	DG	Digital Sub Bias.
VSSD	45, 46	DG	Digital Ground.
VDDD	47, 48	DP	Digital Power.

I/O TYPE ABBR.

- AI : Analog Input
- DI : Digital Input
- AO : Analog Output
- DO : Digital Output
- AB : Analog Bidirectional
- DB : Digital Bidirectional

- AP : Analog Power
- DP : Digital Power
- AG : Analog Ground
- DG : Digital Ground

FEEDBACK REQUEST

It should be quite helpful to our ADC core development if you specify your system requirements on ADC in the following characteristic checking table and fill out the additional questions.
We appreciate your interest in our products. Thank you very much.

Characteristics	Min	Typ	Max	Unit	Remarks
Analog Power Supply Voltage				V	
Digital Power Supply Voltage				V	
Bit Resolution				Bit	
Reference Input Voltage				V	
Analog Input Voltage				V_{pp}	
Operating Temperature				°C	
Integral Non-linearity Error				LSB	
Differential Non-linearity Error				LSB	
Bottom Offset Voltage Error				LSB	
Top Offset Voltage Error				LSB	
Maximum Conversion Rate				MSPS	
Dynamic Supply Current				mA	
Power Dissipation				mW	
Signal-to-noise+distortion Ratio				dB	
Pipeline Delay				CLK	
Digital Output Format (Provide detailed description & timing diagram)					

1. Between single input-output and differential input-output configurations, which one is suitable for your system and why?

2. Please comment on the internal/external pin configurations you want our ADC to have, if you have any reason to prefer some type of configuration.

3. Freely list those functions you want to be implemented in our ADC, if you have any.