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PRELIMINARY

Notice: This is not a final specification.
Some parametric limits are subject to change.

7544 Group
SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

REJ03B0012-0102Z
Rev.1.02
2003.06.25

DESCRIPTION

The 7544 Group is the 8-bit microcomputer based on the 740 family core technology.

The 7544 Group has a serial I/O, 8-bit timers, a 16-bit timer, and an A-D converter, and is useful for control of home electric appliances and office automation equipment.
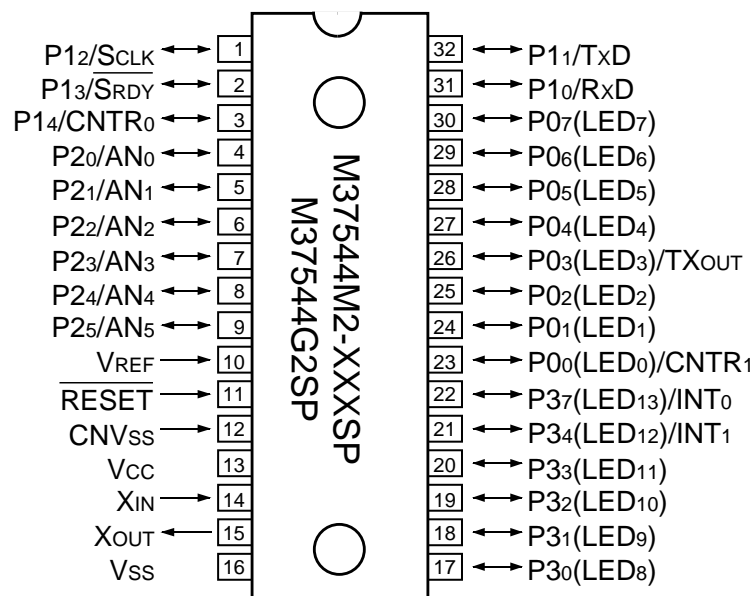
FEATURES

- Basic machine-language instructions 71
- The minimum instruction execution time .... 0.25 µs
  (at 8 MHz oscillation frequency, double-speed mode for the shortest instruction)
- Memory size ROM .... 8 K bytes
  RAM .... 256 bytes
- Programmable I/O ports 25
- Interrupts .... 12 sources, 12 vectors
- Timers .... 8-bit $\times$ 2
  .... 16-bit $\times$ 1
- Serial I/O .... 8-bit $\times$ 1 (UART or Clock-synchronized)
- A-D converter .... 8-bit $\times$ 6 channels

- Clock generating circuit .... Built-in type
  (low-power dissipation by a ring oscillator enabled)
  (connect to external ceramic resonator or quartz-crystal oscillator permitting RC oscillation)
- Watchdog timer .... 16-bit $\times$ 1
- Power source voltage
  X_{IN} oscillation frequency at ceramic/quartz-crystal oscillation, in double-speed mode
  At 8 MHz .... 4.5 to 5.5 V
  X_{IN} oscillation frequency at ceramic/quartz-crystal oscillation, in high-speed mode
  At 8 MHz .... 4.0 to 5.5 V
  X_{IN} oscillation frequency at RC oscillation
  At 4 MHz .... 4.0 to 5.5 V
- Power dissipation .... 22.5mW(standard)
- Operating temperature range .... −20 to 85 °C

APPLICATION

Office automation equipment, factory automation equipment, home electric appliances, consumer electronics, etc.

PIN CONFIGURATION (TOP VIEW)

Pin	Signal	Pin	Signal
1	P1$_2$/S$_{CLK}$	32	P1$_1$/T$_X$D
2	P1$_3$/$\overline{S_{RDY}}$	31	P1$_0$/R$_X$D
3	P1$_4$/CNTR$_0$	30	P0$_7$(LED$_7$)
4	P2$_0$/AN$_0$	29	P0$_6$(LED$_6$)
5	P2$_1$/AN$_1$	28	P0$_5$(LED$_5$)
6	P2$_2$/AN$_2$	27	P0$_4$(LED$_4$)
7	P2$_3$/AN$_3$	26	P0$_3$(LED$_3$)/TX$_{OUT}$
8	P2$_4$/AN$_4$	25	P0$_2$(LED$_2$)
9	P2$_5$/AN$_5$	24	P0$_1$(LED$_1$)
10	V$_{REF}$	23	P0$_0$(LED$_0$)/CNTR$_1$
11	$\overline{RESET}$	22	P3$_7$(LED$_{13}$)/INT$_0$
12	CNV$_{SS}$	21	P3$_4$(LED$_{12}$)/INT$_1$
13	V$_{CC}$	20	P3$_3$(LED$_{11}$)
14	X$_{IN}$	19	P3$_2$(LED$_{10}$)
15	X$_{OUT}$	18	P3$_1$(LED$_9$)
16	V$_{SS}$	17	P3$_0$(LED$_8$)

M37544M2-XXXSP
M37544G2SP

Package type : 32P4B

Fig. 1 Pin configuration (32P4B type)

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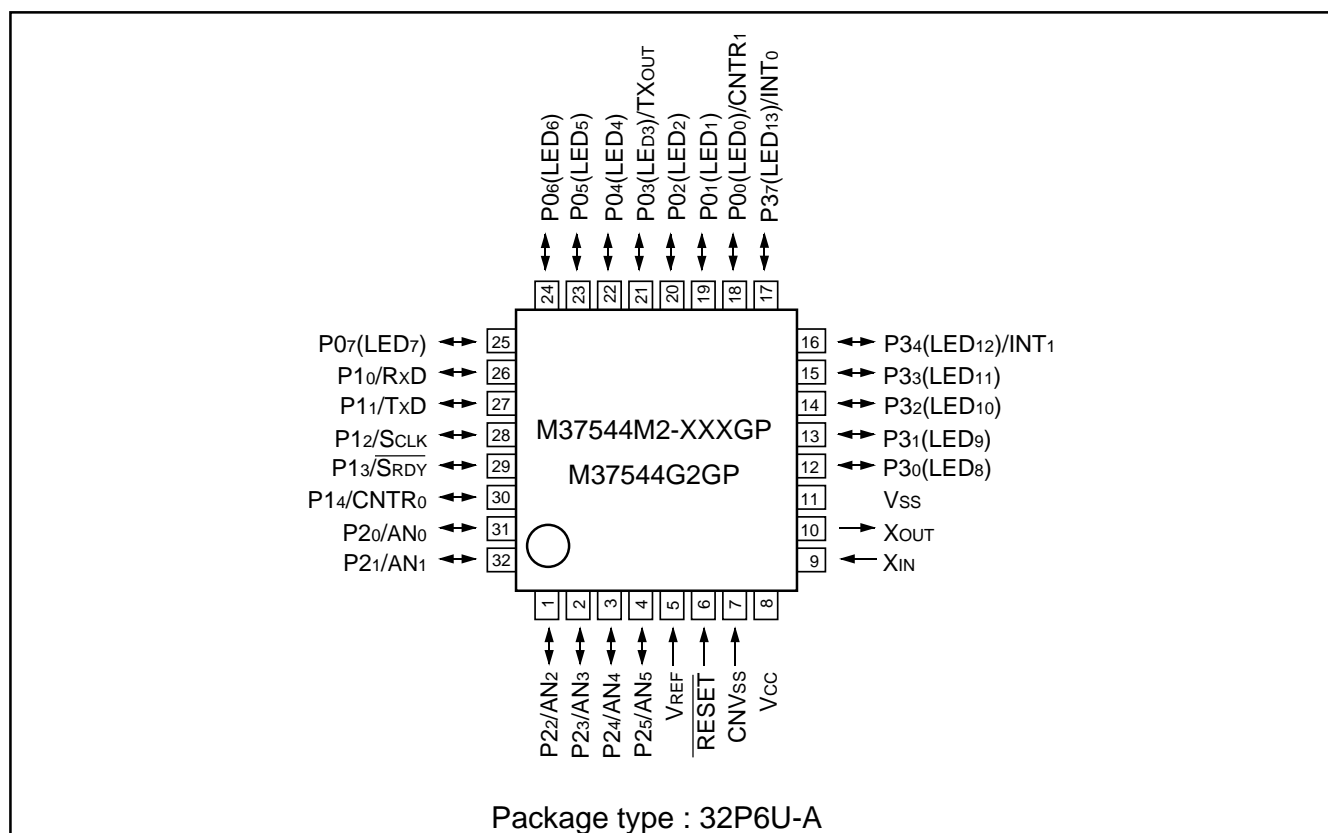
Fig. 2 Pin configuration (32P6U-A type)
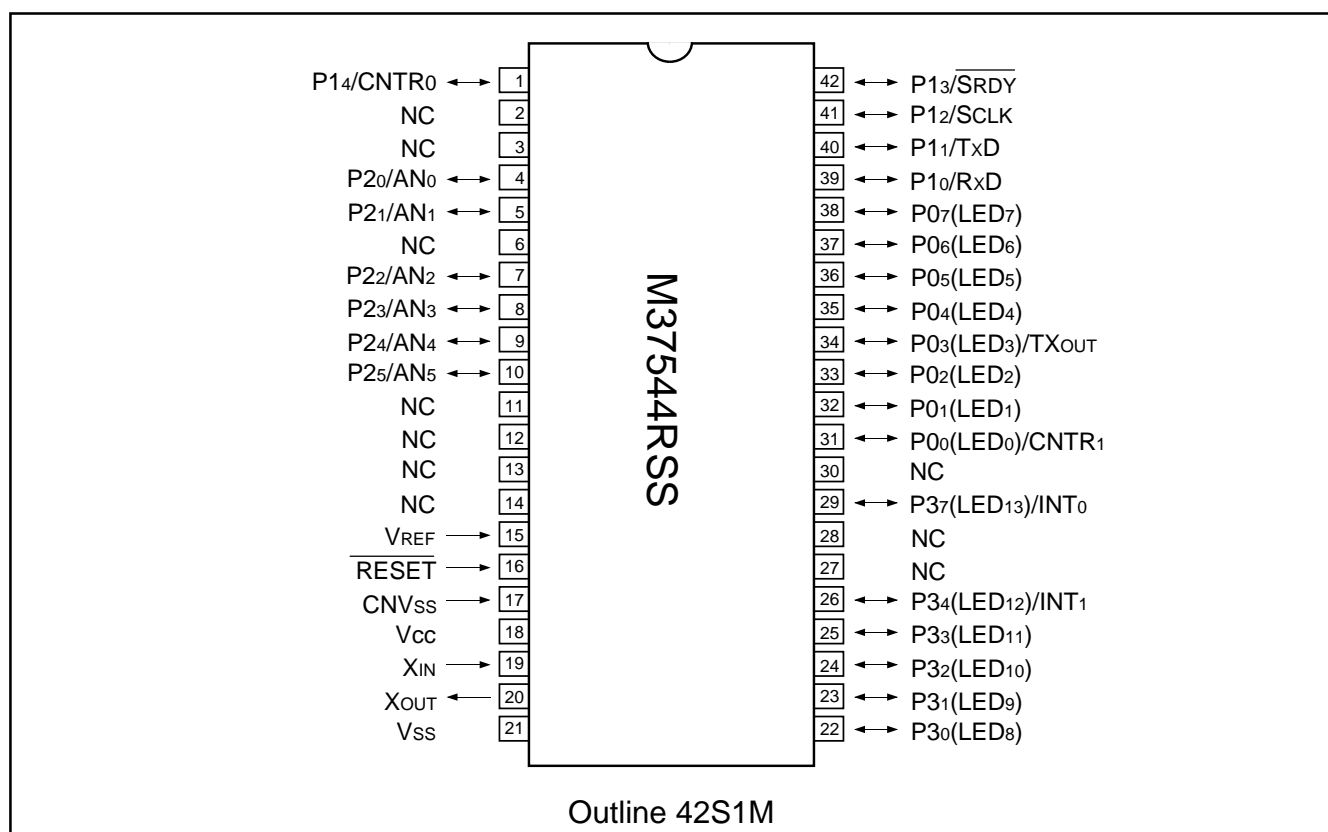
Fig. 3 Pin configuration (42S1M type)

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FUNCTIONAL BLOCK

FUNCTIONAL BLOCK DIAGRAM (Package: 32P4B)
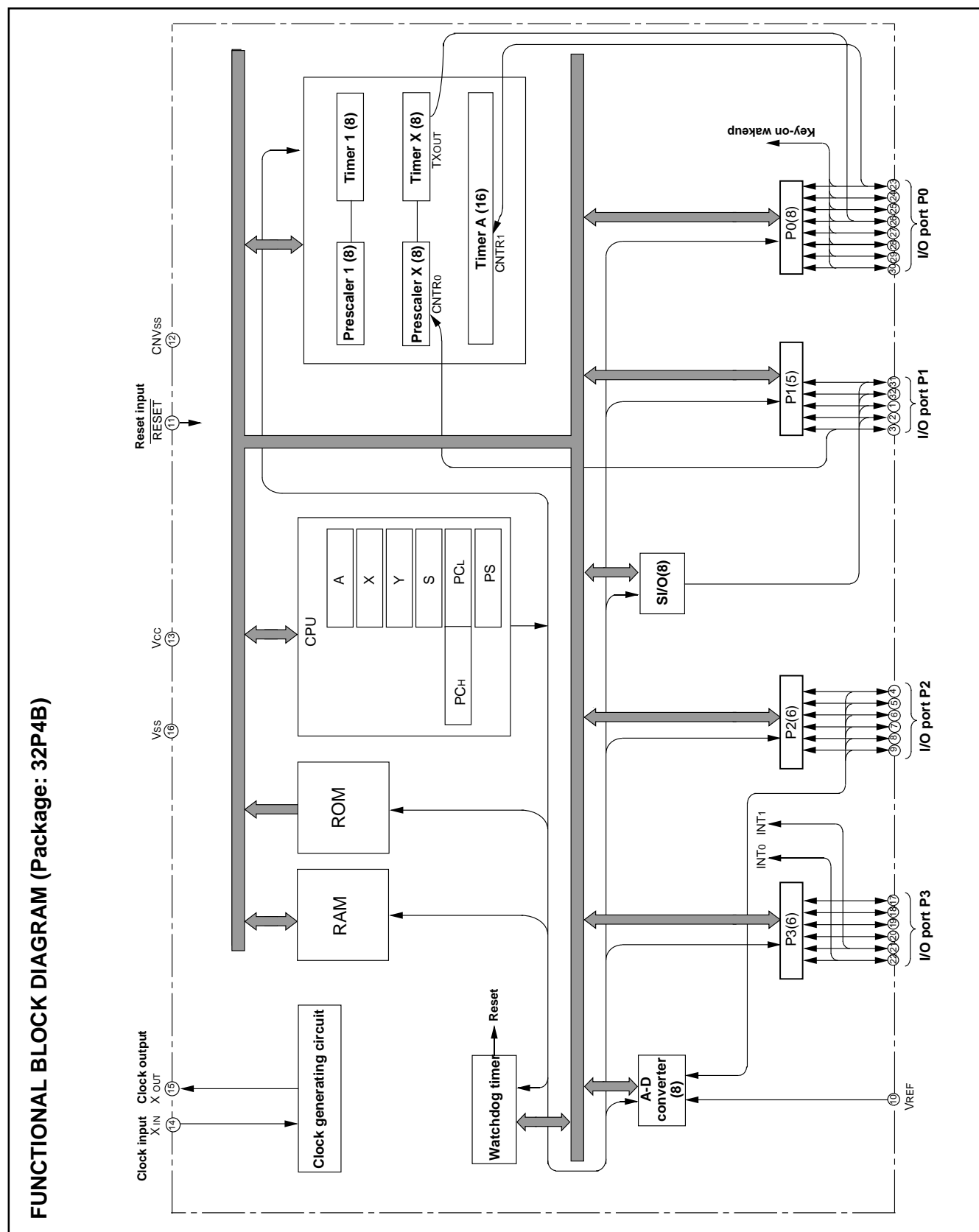
Fig. 4 Functional block diagram (32P4B package)

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FUNCTIONAL BLOCK DIAGRAM (Package: 32P6U)
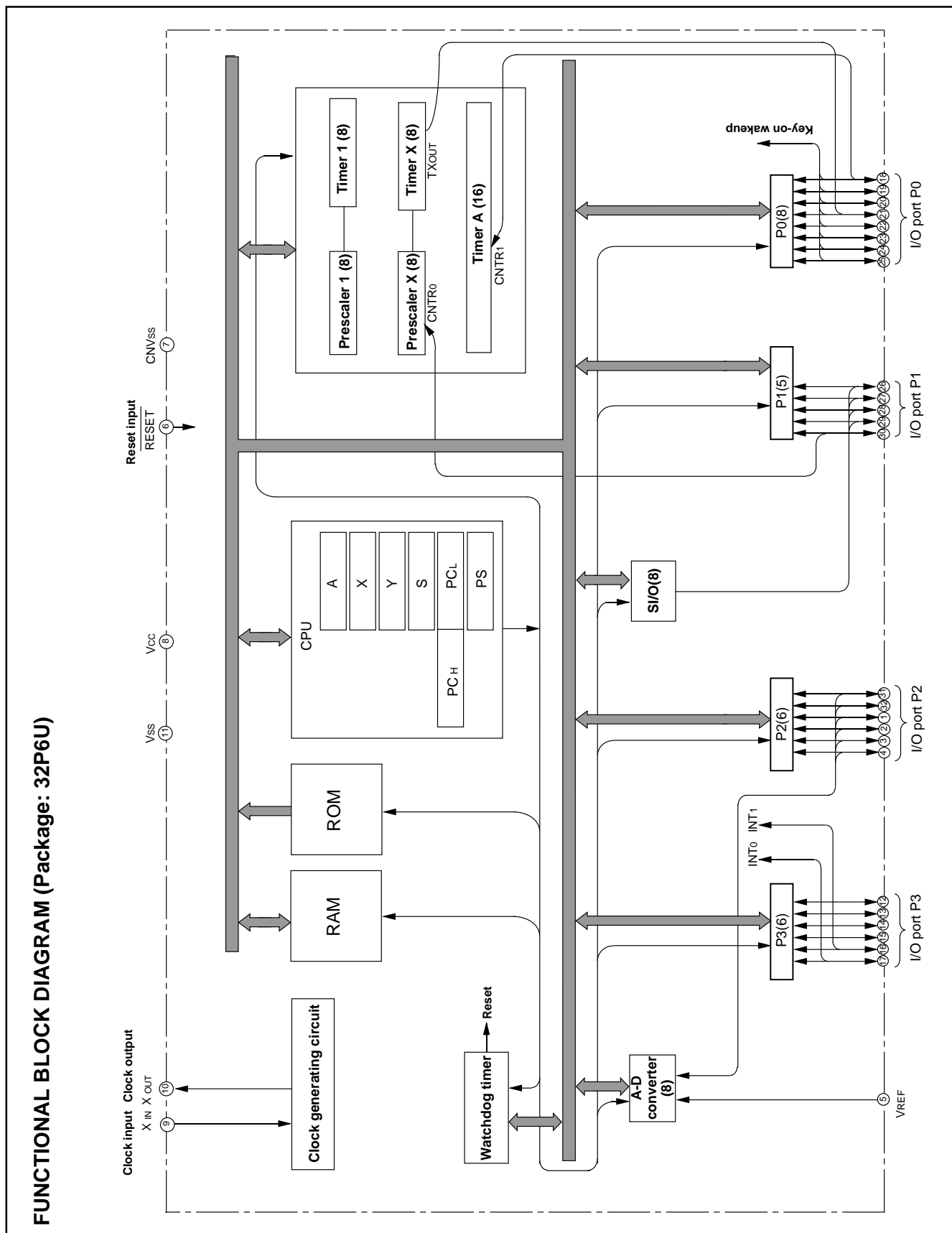
Fig. 5 Functional block diagram (32P6U package)

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PIN DESCRIPTION

Table 1 Pin description

Pin	Name	Function	Function expect a port function
Vcc, Vss	Power source	•Apply voltage of 4.0 to 5.5 V to Vcc, and 0 V to Vss.	
V_{REF}	Analog reference voltage	•Reference voltage input pin for A-D converter	
CNVss	CNVss	•Chip operating mode control pin, which is always connected to Vss.	
$\overline{RESET}$	Reset input	•Reset input pin for active "L"	
X_{IN}	Clock input	•Input and output pins for main clock generating circuit	
		•Connect a ceramic resonator or quartz-crystal oscillator between the X_{IN} and X_{OUT} pins.	
X_{OUT}	Clock output	•For using RC oscillator, short between the X_{IN} and X_{OUT} pins, and connect the capacitor and resistor.	
		•If an external clock is used, connect the clock source to the X_{IN} pin and leave the X_{OUT} pin open.	
		• When the ring oscillator is selected as the main clock, connect X_{IN} pin to V_{CC} and leave X_{OUT} open.	
$P0_0/CNTR_1$ $P0_1$ $P0_2$ $P0_3/TX_{OUT}$ $P0_4$–$P0_7$	I/O port P0	•8-bit I/O port. •I/O direction register allows each pin to be individually programmed as either input or output. •CMOS compatible input level •CMOS 3-state output structure •P0 can output a large current for driving LED. •Whether a built-in pull-up resistor is to be used or not can be determined by program.	• Key-input (key-on wake up interrupt input) pins • Timer X and timer A function pin
$P1_0/RxD$ $P1_1/TxD$ $P1_2/S_{CLK}$ $P1_3/\overline{S_{RDY}}$	I/O port P1	•5-bit I/O port •I/O direction register allows each pin to be individually programmed as either input or output. •CMOS compatible input level •CMOS 3-state output structure •CMOS/TTL level can be switched for $P1_0$ and $P1_2$	• Serial I/O function pin
$P1_4/CNTR_0$			• Timer X function pin
$P2_0/AN_0$–$P2_5/AN_5$	I/O port P2	•6-bit I/O port having almost the same function as P0 •CMOS compatible input level •CMOS 3-state output structure	• Input pins for A-D converter
$P3_0$–$P3_3$	I/O port P3	•6-bit I/O port •I/O direction register allows each pin to be individually programmed as either input or output. •CMOS compatible input level (CMOS/TTL level can be switched for $P3_4$ and $P3_7$). •CMOS 3-state output structure •P3 can output a large current for driving LED.	
$P3_4/INT_1$ $P3_7/INT_0$		•Whether a built-in pull-up resistor is to be used or not can be determined by program.	• Interrupt input pins

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GROUP EXPANSION

We are planning to expand the 7544 group as follow:

Memory type

Support for Mask ROM version, One Time PROM version, and Emulator MCU .

Memory size

ROM/PROM size .... 8 K bytes

RAM size .... 256 bytes

Package

32P4B .... 32-pin plastic molded SDIP

32P6U-A .... 0.8 mm-pitch 32-pin plastic molded LQFP

42S1M .... 42-pin shrink ceramic PIGGY BACK
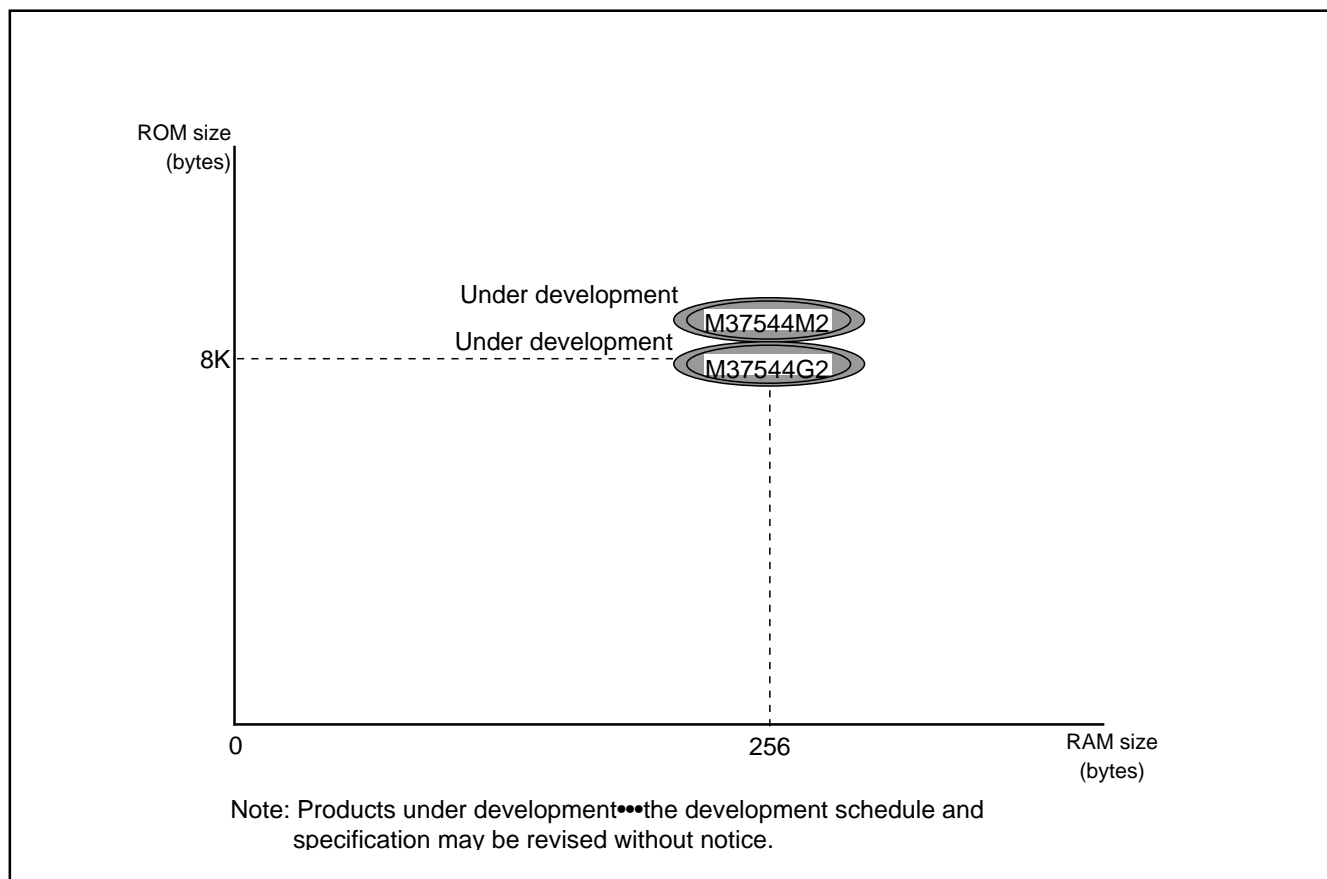
Fig. 6 Memory expansion plan

Currently supported products are listed below.

Table 2 List of supported products

Product	(P) ROM size (bytes) ROM size for User ()	RAM size (bytes)	Package	Remarks
M37544M2-XXXSP*	8192 (8062)	256	32P4B	Mask ROM version
M37544M2-XXXGP*			32P6U-A	Mask ROM version
M37544G2SP*			32P4B	One Time PROM version (blank)
M37544G2GP*			32P6U-A	One Time PROM version (blank)
M37544RSS	————	256	42S1M	Emulator MCU

*: Under development

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FUNCTIONAL DESCRIPTION

Central Processing Unit (CPU)
The MCU uses the standard 740 family instruction set. Refer to the table of 740 family addressing modes and machine-language instructions or the SERIES 740 <SOFTWARE> USER'S MANUAL for details on each instruction set.
Machine-resident 740 family instructions are as follows:
1. The FST and SLW instructions cannot be used.
2. The MUL and DIV instructions can be used.
3. The WIT instruction can be used.
4. The STP instruction can be used.
This instruction cannot be used while CPU operates by a ring oscillator.

Accumulator (A)
The accumulator is an 8-bit register. Data operations such as data transfer, etc., are executed mainly through the accumulator.

Index register X (X), Index register Y (Y)
Both index register X and index register Y are 8-bit registers. In the index addressing modes, the value of the OPERAND is added to the contents of register X or register Y and specifies the real address.
When the T flag in the processor status register is set to "1", the value contained in index register X becomes the address for the second OPERAND.

Stack pointer (S)
The stack pointer is an 8-bit register used during subroutine calls and interrupts. The stack is used to store the current address data and processor status when branching to subroutines or interrupt routines.
The lower eight bits of the stack address are determined by the contents of the stack pointer. The upper eight bits of the stack address are determined by the Stack Page Selection Bit. If the Stack Page Selection Bit is "0", then the RAM in the zero page is used as the stack area. If the Stack Page Selection Bit is "1", then RAM in page 1 is used as the stack area.
The Stack Page Selection Bit is located in the SFR area in the zero page. Note that the initial value of the Stack Page Selection Bit varies with each microcomputer type. Also some microcomputer types have no Stack Page Selection Bit and the upper eight bits of the stack address are fixed. The operations of pushing register contents onto the stack and popping them from the stack are shown in Fig. 9.

Program counter (PC)
The program counter is a 16-bit counter consisting of two 8-bit registers PC_H and PC_L. It is used to indicate the address of the next instruction to be executed.
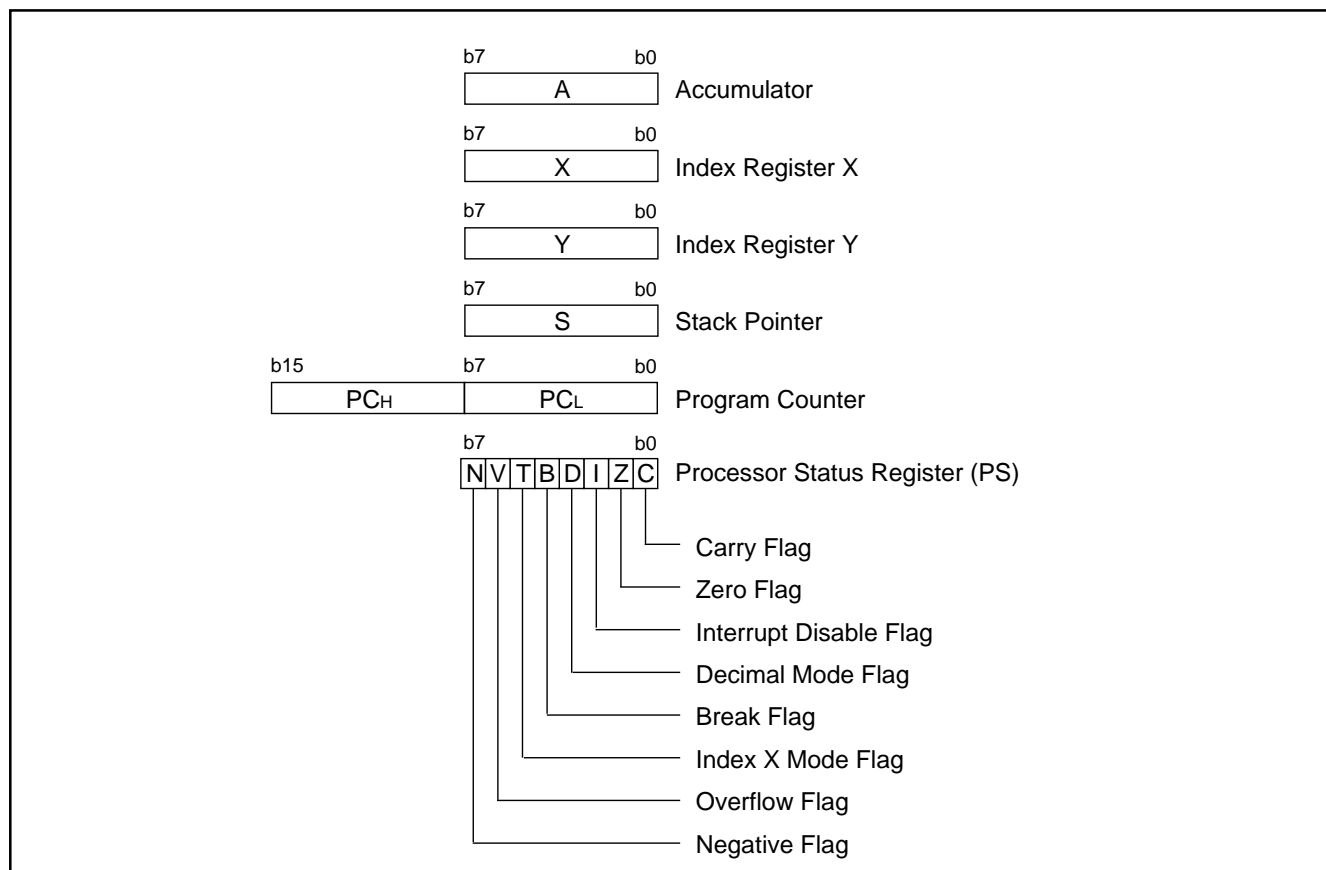

Fig. 7 740 Family CPU register structure

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Notice: This is not a final specification.
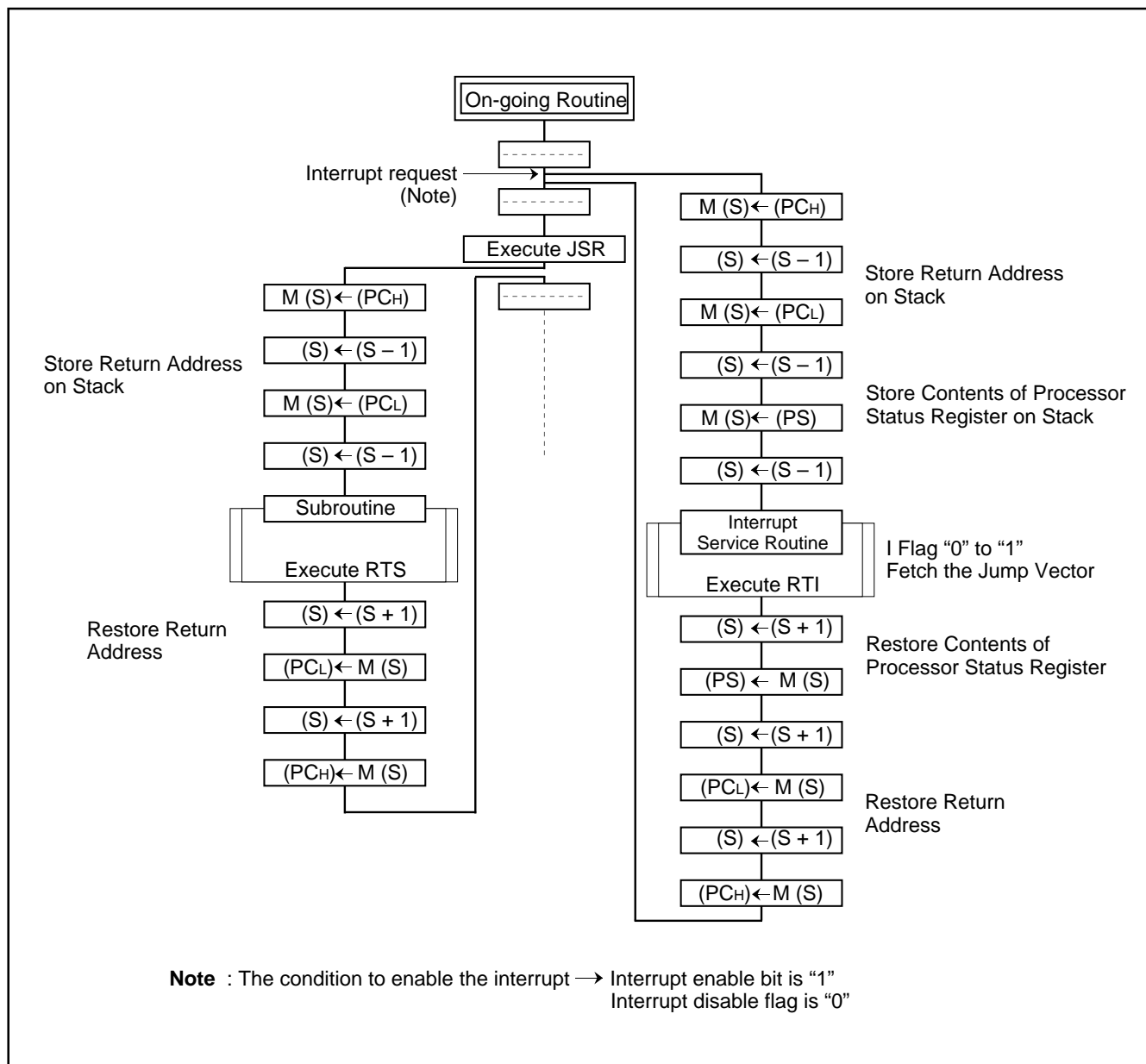Some parametric limits are subject to change.

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Fig. 8 Register push and pop at interrupt generation and subroutine call

Table 3 Push and pop instructions of accumulator or processor status register

	Push instruction to stack	Pop instruction from stack
Accumulator	PHA	PLA
Processor status register	PHP	PLP

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Processor status register (PS)

The processor status register is an 8-bit register consisting of flags which indicate the status of the processor after an arithmetic operation. Branch operations can be performed by testing the Carry (C) flag, Zero (Z) flag, Overflow (V) flag, or the Negative (N) flag. In decimal mode, the Z, V, N flags are not valid.

After reset, the Interrupt disable (I) flag is set to "1", but all other flags are undefined. Since the Index X mode (T) and Decimal mode (D) flags directly affect arithmetic operations, they should be initialized in the beginning of a program.

(1) Carry flag (C)

The C flag contains a carry or borrow generated by the arithmetic logic unit (ALU) immediately after an arithmetic operation. It can also be changed by a shift or rotate instruction.

(2) Zero flag (Z)

The Z flag is set if the result of an immediate arithmetic operation or a data transfer is "0", and cleared if the result is anything other than "0".

(3) Interrupt disable flag (I)

The I flag disables all interrupts except for the interrupt generated by the BRK instruction. Interrupts are disabled when the I flag is "1".

When an interrupt occurs, this flag is automatically set to "1" to prevent other interrupts from interfering until the current interrupt is serviced.

(4) Decimal mode flag (D)

The D flag determines whether additions and subtractions are executed in binary or decimal. Binary arithmetic is executed when this flag is "0"; decimal arithmetic is executed when it is "1". Decimal correction is automatic in decimal mode. Only the ADC and SBC instructions can be used for decimal arithmetic.

(5) Break flag (B)

The B flag is used to indicate that the current interrupt was generated by the BRK instruction. The BRK flag in the processor status register is always "0". When the BRK instruction is used to generate an interrupt, the processor status register is pushed onto the stack with the break flag set to "1". The saved processor status is the only place where the break flag is ever set.

(6) Index X mode flag (T)

When the T flag is "0", arithmetic operations are performed between accumulator and memory, e.g. the results of an operation between two memory locations is stored in the accumulator. When the T flag is "1", direct arithmetic operations and direct data transfers are enabled between memory locations, i.e. between memory and memory, memory and I/O, and I/O and I/O. In this case, the result of an arithmetic operation performed on data in memory location 1 and memory location 2 is stored in memory location 1. The address of memory location 1 is specified by index register X, and the address of memory location 2 is specified by normal addressing modes.

(7) Overflow flag (V)

The V flag is used during the addition or subtraction of one byte of signed data. It is set if the result exceeds +127 to -128. When the BIT instruction is executed, bit 6 of the memory location operated on by the BIT instruction is stored in the overflow flag.

(8) Negative flag (N)

The N flag is set if the result of an arithmetic operation or data transfer is negative. When the BIT instruction is executed, bit 7 of the memory location operated on by the BIT instruction is stored in the negative flag.

Table 4 Set and clear instructions of each bit of processor status register

	C flag	Z flag	I flag	D flag	B flag	T flag	V flag	N flag
Set instruction	SEC	–	SEI	SED	–	SET	–	–
Clear instruction	CLC	–	CLI	CLD	–	CLT	CLV	–

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[CPU mode register] CPUM
The CPU mode register contains the stack page selection bit.
This register is allocated at address 003B16.

Switching method of CPU mode register
Switch the CPU mode register (CPUM) at the head of program after releasing Reset in the following method.
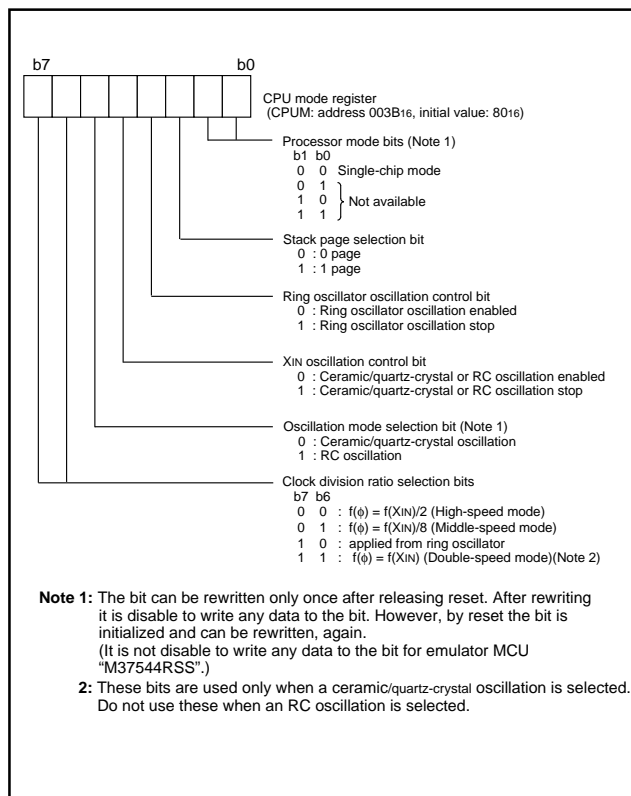


```
b7                    b0
┌─┬─┬─┬─┬─┬─┬─┬─┐
└─┴─┴─┴─┴─┴─┴─┴─┘   CPU mode register
                    (CPUM: address 003B16, initial value: 8016)

                    Processor mode bits (Note 1)
                    b1 b0
                    0  0   Single-chip mode
                    0  1
                    1  0  } Not available
                    1  1

                    Stack page selection bit
                    0 : 0 page
                    1 : 1 page

                    Ring oscillator oscillation control bit
                    0 : Ring oscillator oscillation enabled
                    1 : Ring oscillator oscillation stop

                    XIN oscillation control bit
                    0 : Ceramic/quartz-crystal or RC oscillation enabled
                    1 : Ceramic/quartz-crystal or RC oscillation stop

                    Oscillation mode selection bit (Note 1)
                    0 : Ceramic/quartz-crystal oscillation
                    1 : RC oscillation

                    Clock division ratio selection bits
                    b7 b6
                    0  0 : f(φ) = f(XIN)/2 (High-speed mode)
                    0  1 : f(φ) = f(XIN)/8 (Middle-speed mode)
                    1  0 : applied from ring oscillator
                    1  1 : f(φ) = f(XIN) (Double-speed mode)(Note 2)
```

Note 1: The bit can be rewritten only once after releasing reset. After rewriting it is disable to write any data to the bit. However, by reset the bit is initialized and can be rewritten, again.
(It is not disable to write any data to the bit for emulator MCU "M37544RSS".)

2: These bits are used only when a ceramic/quartz-crystal oscillation is selected. Do not use these when an RC oscillation is selected.

Fig. 9 Structure of CPU mode register


```
┌─────────────────────────────┐
│    After releasing reset     │   Start with a built-in ring oscillator
└─────────────────────────────┘
              │
              ▼
┌─────────────────────────────┐   An initial value is set as a ceramic/quartz-crystal
│  Switch the oscillation mode │   oscillation mode. When it is switched to an RC
│   selection bit (bit 5 of CPUM) │ oscillation, its oscillation starts.
└─────────────────────────────┘
              │
              ▼
┌─────────────────────────────┐   When using a ceramic/quartz-crystal oscillation, wait
│  Wait by ring oscillator operation until │  until establlishment of oscillation from oscillation starts.
│  establishment of oscillator clock │  When using an RC oscillation, wait time is not required
└─────────────────────────────┘   basically (time to execute the instruction to switch from
                                   a ring oscillator meets the requirement).
              │
              ▼
┌─────────────────────────────┐   Select 1/1, 1/2, 1/8 or ring oscillator.
│  Switch the clock division ratio │
│  selection bits (bits 6 and 7 of CPUM) │
└─────────────────────────────┘
              │
              ▼
┌─────────────────────────────┐
│         Main routine         │
└─────────────────────────────┘
```

Fig. 10 Switching method of CPU mode register

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Memory

Special function register (SFR) area
The SFR area in the zero page contains control registers such as I/O ports and timers.

RAM
RAM is used for data storage and for a stack area of subroutine calls and interrupts.

ROM
The first 128 bytes and the last 2 bytes of ROM are reserved for device testing and the rest is a user area for storing programs.

Interrupt vector area
The interrupt vector area contains reset and interrupt vectors.

Zero page
The 256 bytes from addresses 0000_{16} to $00FF_{16}$ are called the zero page area. The internal RAM and the special function registers (SFR) are allocated to this area.
The zero page addressing mode can be used to specify memory and register addresses in the zero page area. Access to this area with only 2 bytes is possible in the zero page addressing mode.

Special page
The 256 bytes from addresses $FF00_{16}$ to $FFFF_{16}$ are called the special page area. The special page addressing mode can be used to specify memory addresses in the special page area. Access to this area with only 2 bytes is possible in the special page addressing mode.

■ Note on use
The content of RAM is undefined when the microcomputer is reset. The initial values must be surely set before you use it.

RAM area

RAM capacity (bytes)	address XXXX$_{16}$
256	013F$_{16}$

ROM area

ROM capacity (bytes)	address YYYY$_{16}$	address ZZZZ$_{16}$
8192	E000$_{16}$	E080$_{16}$
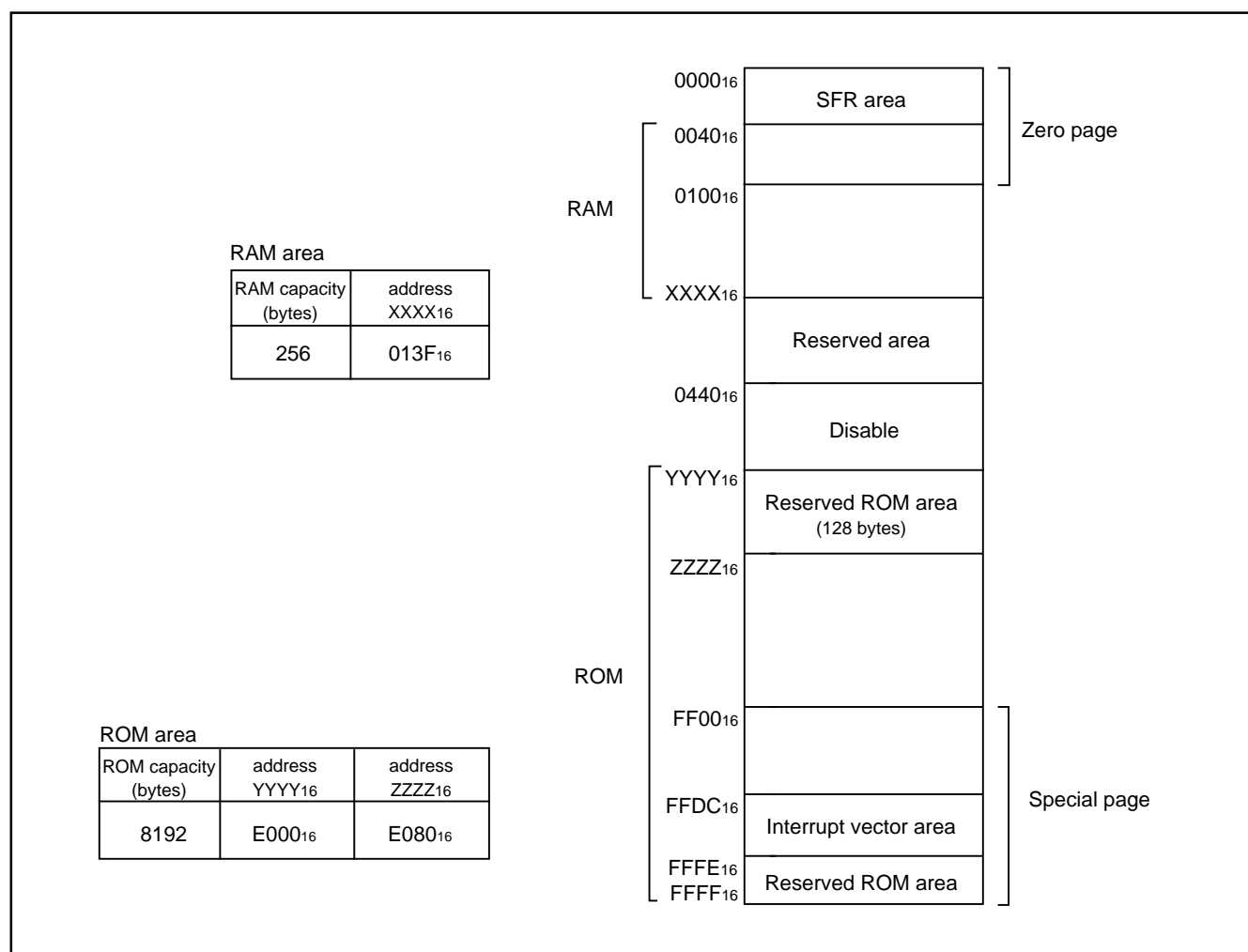
Fig. 11 Memory map diagram

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Address	Register	Address	Register
0000_{16}	Port P0 (P0)	0020_{16}	Reserved
0001_{16}	Port P0 direction register (P0D)	0021_{16}	Reserved
0002_{16}	Port P1 (P1)	0022_{16}	Reserved
0003_{16}	Port P1 direction register (P1D)	0023_{16}	Reserved
0004_{16}	Port P2 (P2)	0024_{16}	Reserved
0005_{16}	Port P2 direction register (P2D)	0025_{16}	Reserved
0006_{16}	Port P3 (P3)	0026_{16}	Reserved
0007_{16}	Port P3 direction register (P3D)	0027_{16}	Reserved
0008_{16}	Reserved	0028_{16}	Prescaler 1 (PRE1)
0009_{16}	Reserved	0029_{16}	Timer 1 (T1)
$000A_{16}$	Reserved	$002A_{16}$	Reserved
$000B_{16}$	Reserved	$002B_{16}$	Timer X mode register (TXM)
$000C_{16}$	Reserved	$002C_{16}$	Prescaler X (PREX)
$000D_{16}$	Reserved	$002D_{16}$	Timer X (TX)
$000E_{16}$	Reserved	$002E_{16}$	Timer count source set register1 (TCSS1)
$000F_{16}$	Reserved	$002F_{16}$	Timer count source set register2 (TCSS2)
0010_{16}	Reserved	0030_{16}	Reserved
0011_{16}	Reserved	0031_{16}	Reserved
0012_{16}	Reserved	0032_{16}	Reserved
0013_{16}	Reserved	0033_{16}	Reserved
0014_{16}	Reserved	0034_{16}	A-D control register (ADCON)
0015_{16}	Reserved	0035_{16}	A-D register (AD)
0016_{16}	Pull-up control register (PULL)	0036_{16}	Reserved
0017_{16}	Port P1P3 control register (P1P3C)	0037_{16}	Reserved
0018_{16}	Transmit/Receive buffer register (TB/RB)	0038_{16}	MISRG
0019_{16}	Serial I/O status register (SIO1STS)	0039_{16}	Watchdog timer control register (WDTCON)
$001A_{16}$	Serial I/O control register (SIO1CON)	$003A_{16}$	Interrupt edge selection register (INTEDGE)
$001B_{16}$	UART control register (UARTCON)	$003B_{16}$	CPU mode register (CPUM)
$001C_{16}$	Baud rate generator (BRG)	$003C_{16}$	Interrupt request register 1 (IREQ1)
$001D_{16}$	Timer A mode register (TAM)	$003D_{16}$	Interrupt request register 2 (IREQ2)
$001E_{16}$	Timer A (low-order) (TAL)	$003E_{16}$	Interrupt control register 1 (ICON1)
$001F_{16}$	Timer A (high-order) (TAH)	$003F_{16}$	Interrupt control register 2 (ICON2)

Note : Do not access to the SFR area including nothing.

Fig. 12 Memory map of special function register (SFR)

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I/O Ports

[Direction registers] PiD

The I/O ports have direction registers which determine the input/output direction of each pin. Each bit in a direction register corresponds to one pin, and each pin can be set to be input or output.
When "1" is set to the bit corresponding to a pin, this pin becomes an output port. When "0" is set to the bit, the pin becomes an input port.
When data is read from a pin set to output, not the value of the pin itself but the value of port latch is read. Pins set to input are floating, and permit reading pin values.
If a pin set to input is written to, only the port latch is written to and the pin remains floating.

[Pull-up control register] PULL

By setting the pull-up control register (address 0016_{16}), ports P0 and P3 can exert pull-up control by program. However, pins set to output are disconnected from this control and cannot exert pull-up control.

[Port P1P3 control register] P1P3C

By setting the port P1P3 control register (address 0017_{16}), a CMOS input level or a TTL input level can be selected for ports $P1_0$, $P1_2$, $P3_4$, and $P3_7$ by program.

b7   b0

Pull-up control register
(PULL: address 0016_{16}, initial value: 00_{16})

$P0_0$ pull-up control bit

$P0_1$ pull-up control bit

$P0_2$, $P0_3$ pull-up control bit

$P0_4$ – $P0_7$ pull-up control bit

$P3_0$ – $P3_3$ pull-up control bit

$P3_4$ pull-up control bit

Disable

0 : Pull-up Off
1 : Pull-up On

$P3_7$ pull-up control bit

Note : Pins set to output ports are disconnected from pull-up control.
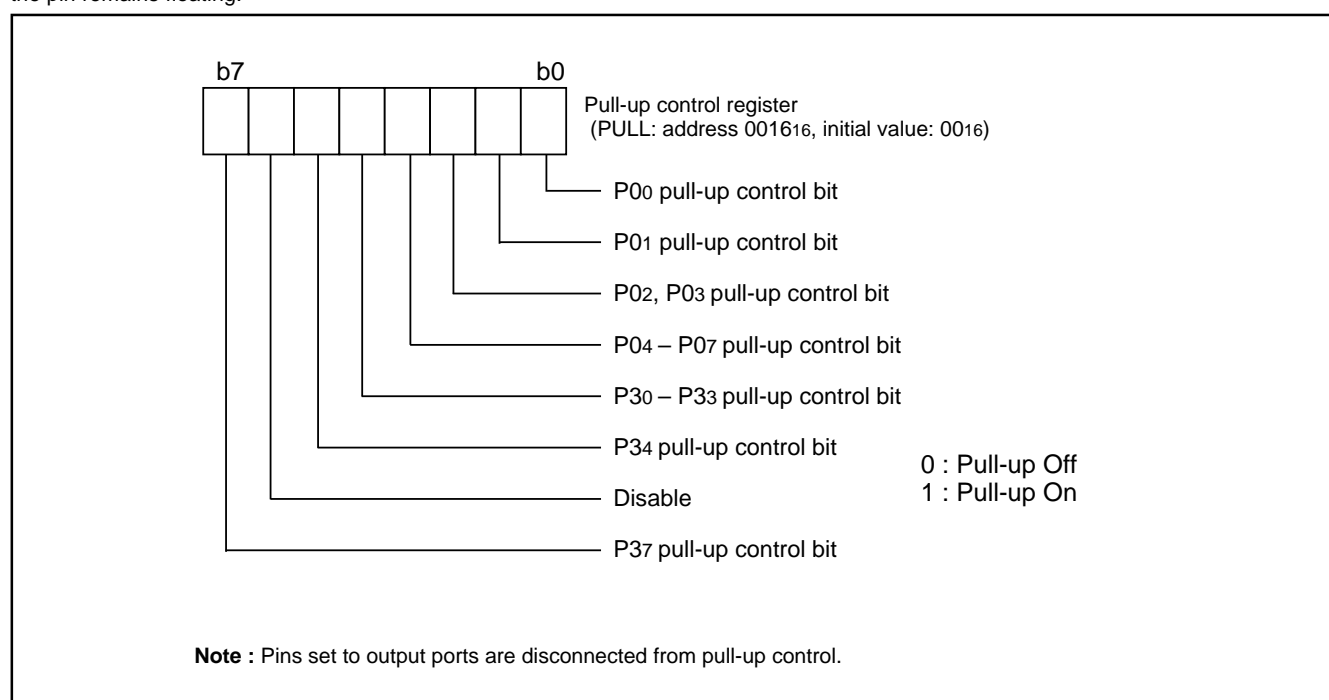
Fig. 13 Structure of pull-up control register

b7   b0

Port P1P3 control register
(P1P3C: address 0017_{16}, initial value: 00_{16})

$P3_7/INT_0$ input level selection bit
0 : CMOS level
1 : TTL level

$P3_4/INT_1$ input level selection bit
0 : CMOS level
1 : TTL level

$P1_0$,$P1_2$ input level selection bit
0 : CMOS level
1 : TTL level

Disable
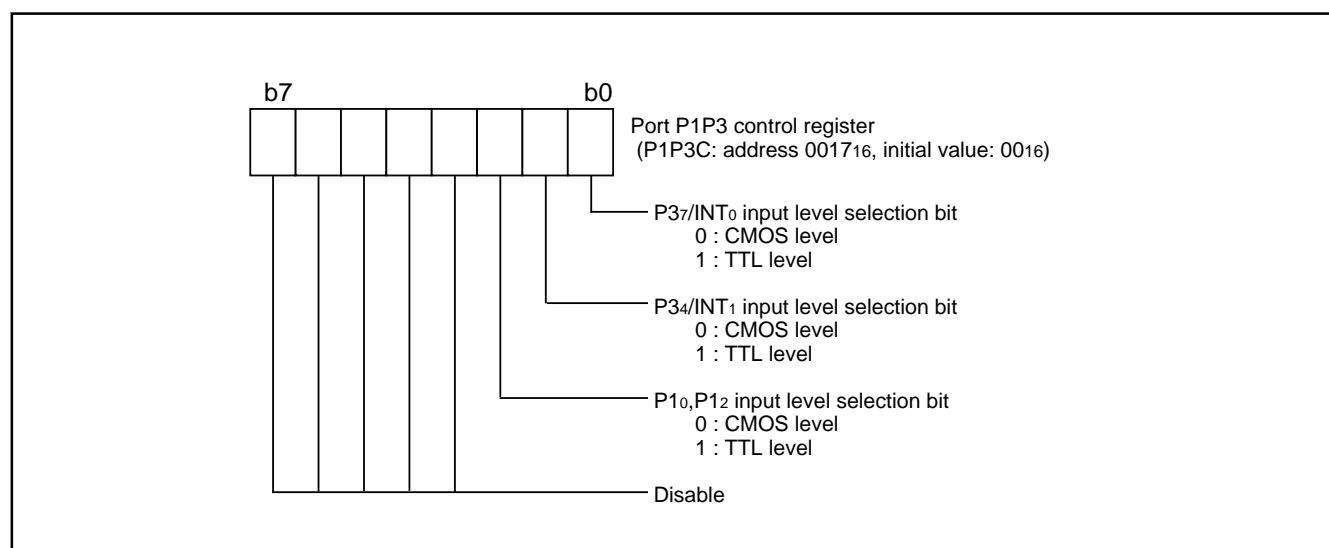
Fig. 14 Structure of port P1P3 control register

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Table 5 I/O port function table

Pin	Name	Input/output	I/O format	Non-port function	Related SFRs	Diagram No.
$P0_0$/$CNTR_1$ $P0_1$ $P0_2$ $P0_3$/TX_{OUT} $P0_4$–$P0_7$	I/O port P0	I/O individual bits	•CMOS compatible input level •CMOS 3-state output (**Note**)	Key input interrupt Timer X function output Timer A function input	Pull-up control register Timer X mode register Timer A mode register Interrupt edge selection register	(1) (2) (3)
$P1_0$/RxD $P1_1$/TxD $P1_2$/S_{CLK} $P1_3$/S_{RDY}	I/O port P1			Serial I/O function input/output	Serial I/O control register Port P1,P3 control register	(4) (5) (6) (7)
$P1_4$/$CNTR_0$				Timer X function input/output	Timer X mode register	(8)
$P2_0$/AN_0– $P2_5$/AN_5	I/O port P2			A-D conversion input	A-D control register	(9)
$P3_0$–$P3_3$	I/O port P3				Pull-up control register	(10)
$P3_4$/INT_1 $P3_7$/INT_0				External interrupt input	Interrupt edge selection register Pull-up control register Port P1,P3 control register	(11)

Note : Ports $P1_0$, $P1_2$, $P3_4$, and $P3_7$ are CMOS/TTL level.

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Notice: This is not a final specification.
Some parametric limits are subject to change.
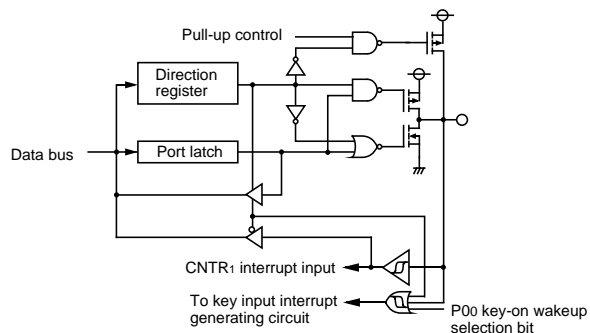
(1)Port P0₀

(2)Ports P0₁,P0₂,P0₄–P0₇
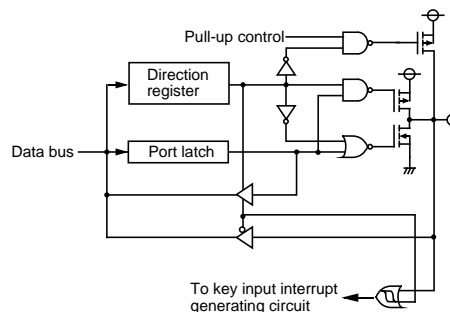
(3)Port P0₃
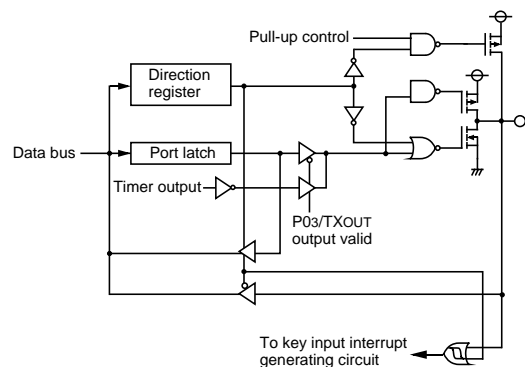
(4)Port P1₀
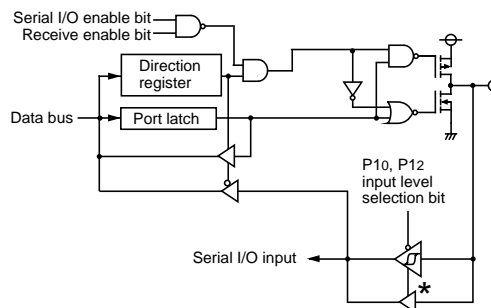
(5)Port P1₁
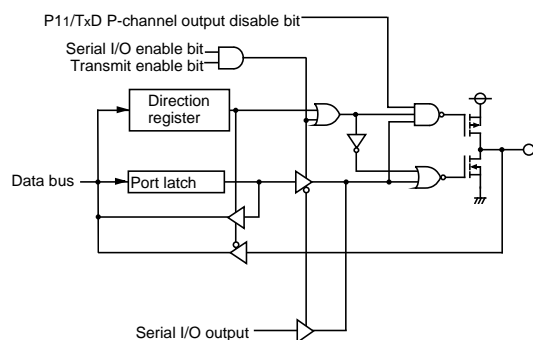
(6)Port P1₂
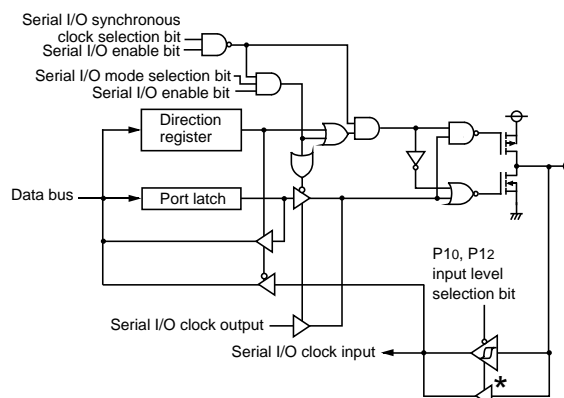
✱ P10, P12, P34, and P37 input level are switched to the CMOS/TTL level by the port P1P3 control register.
When the TTL level is selected, there is no hysteresis characteristics.

Fig. 15 Block diagram of ports (1)

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Some parametric limits are subject to change.

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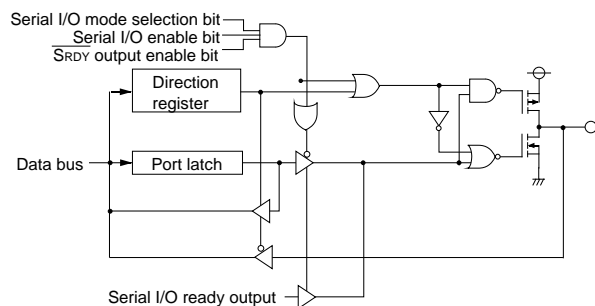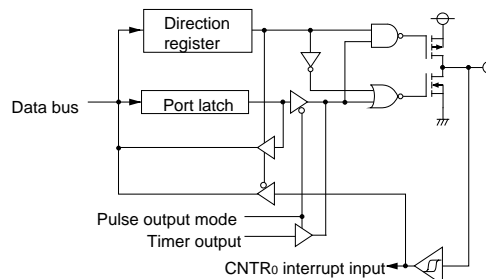
(7) Port P1$_3$

(8) Port P1$_4$

(9) Ports P2$_0$–P2$_5$
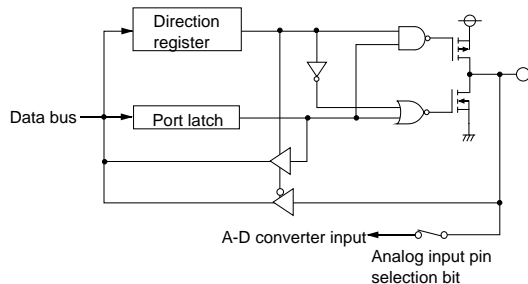
(10) Ports P3$_0$–P3$_3$
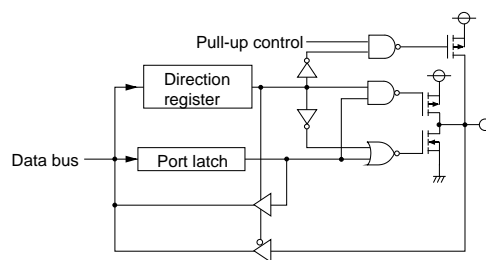
(11) Ports P3$_4$, P3$_7$
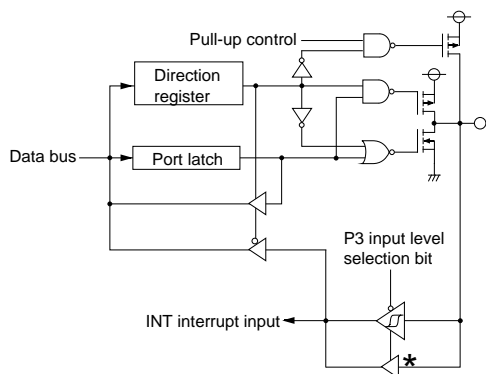
* P1$_0$, P1$_2$, P3$_4$, and P3$_7$ input level are switched to the CMOS/TTL level by the port P1P3 control register.
When the TTL level is selected, there is no hysteresis characteristics.

Fig. 16 Block diagram of ports (2)

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Notice: This is not a final specification.
Some parametric limits are subject to change.

Interrupts

Interrupts occur by 12 different sources : 5 external sources, 6 internal sources and 1 software source.

Interrupt control

All interrupts except the BRK instruction interrupt have an interrupt request bit and an interrupt enable bit, and they are controlled by the interrupt disable flag. When the interrupt enable bit and the interrupt request bit are set to "1" and the interrupt disable flag is set to "0", an interrupt is accepted.

The interrupt request bit can be cleared by program but not be set. The interrupt enable bit can be set and cleared by program.

The reset and BRK instruction interrupt can never be disabled with any flag or bit. All interrupts except these are disabled when the interrupt disable flag is set.

When several interrupts occur at the same time, the interrupts are received according to priority.

Interrupt operation

Upon acceptance of an interrupt the following operations are automatically performed:

1. The processing being executed is stopped.
2. The contents of the program counter and processor status register are automatically pushed onto the stack.
3. The interrupt disable flag is set and the corresponding interrupt request bit is cleared.
4. Concurrently with the push operation, the interrupt destination address is read from the vector table into the program counter.

■ Notes on use

When setting the followings, the interrupt request bit may be set to "1".

•When setting external interrupt active edge
Related register: Interrupt edge selection register (address $003A_{16}$)
Timer X mode register (address $2B_{16}$)
Timer A mode register (address $1D_{16}$)

When not requiring the interrupt occurrence synchronized with these setting, take the following sequence.

① Set the corresponding interrupt enable bit to "0" (disabled).
② Set the interrupt edge select bit (active edge switch bit) to "1".
③ Set the corresponding interrupt request bit to "0" after 1 or more instructions have been executed.
④ Set the corresponding interrupt enable bit to "1" (enabled).

Table 6 Interrupt vector address and priority

Interrupt source	Priority	Vector addresses (**Note 1**)		Interrupt request generating conditions	Remarks
		High-order	Low-order		
Reset (**Note 2**)	1	$FFFD_{16}$	$FFFC_{16}$	At reset input	Non-maskable
Serial I/O receive	2	$FFFB_{16}$	$FFFA_{16}$	At completion of serial I/O data receive	
Serial I/O transmit	3	$FFF9_{16}$	$FFF8_{16}$	At completion of serial I/O transmit shift or when transmit buffer is empty	
INT0	4	$FFF7_{16}$	$FFF6_{16}$	At detection of either rising or falling edge of INT0 input	External interrupt (active edge selectable)
INT1	5	$FFF5_{16}$	$FFF4_{16}$	At detection of either rising or falling edge of INT1 input	External interrupt (active edge selectable)
Key-on wake-up	6	$FFF3_{16}$	$FFF2_{16}$	At falling of conjunction of input logical level for port P0 (at input)	External interrupt (valid at falling)
CNTR0	7	$FFF1_{16}$	$FFF0_{16}$	At detection of either rising or falling edge of CNTR0 input	External interrupt (active edge selectable)
CNTR1	8	$FFEF_{16}$	$FFEE_{16}$	At detection of either rising or falling edge of CNTR1 input	External interrupt (active edge selectable)
Timer X	9	$FFED_{16}$	$FFEC_{16}$	At timer X underflow	
Reserved area	—	$FFEB_{16}$	$FFEA_{16}$	Not available	
Reserved area	—	$FFE9_{16}$	$FFE8_{16}$	Not available	
Timer A	10	$FFE7_{16}$	$FFE6_{16}$	At timer A underflow	
Reserved area	—	$FFE5_{16}$	$FFE4_{16}$	Not available	
A-D conversion	11	$FFE3_{16}$	$FFE2_{16}$	At completion of A-D conversion	
Timer 1	12	$FFE1_{16}$	$FFE0_{16}$	At timer 1 underflow	STP release timer underflow
Reserved area	—	$FFDF_{16}$	$FFDE_{16}$	Not available	
BRK instruction	13	$FFDD_{16}$	$FFDC_{16}$	At BRK instruction execution	Non-maskable software interrupt

Note 1: Vector addressed contain internal jump destination addresses.
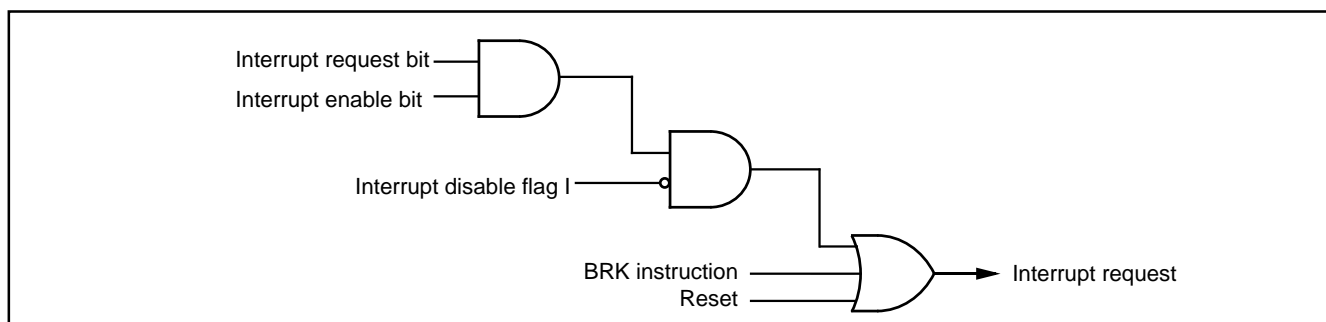   **2:** Reset function in the same way as an interrupt with the highest priority.

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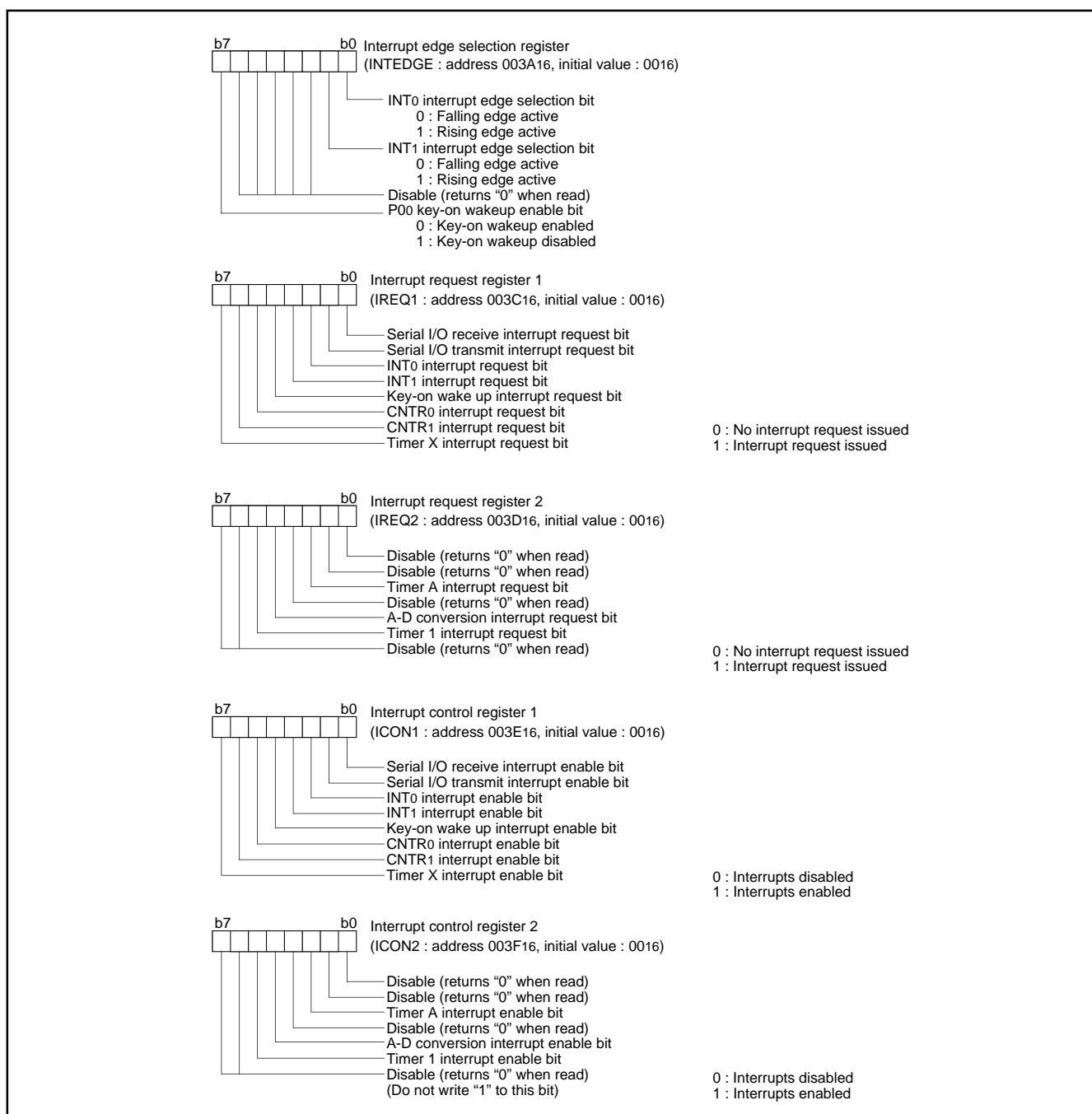
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Fig. 17 Interrupt control

Fig. 18 Structure of Interrupt-related registers

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Key Input Interrupt (Key-On Wake-Up)

A key-on wake-up interrupt request is generated by applying "L" level to any pin of port P0 that has been set to input mode. In other words, it is generated when the AND of input level goes from "1" to "0". An example of using a key input interrupt is shown in Figure 19, where an interrupt request is generated by pressing one of the keys provided as an active-low key matrix which uses ports P0$_0$ to P0$_3$ as input ports.
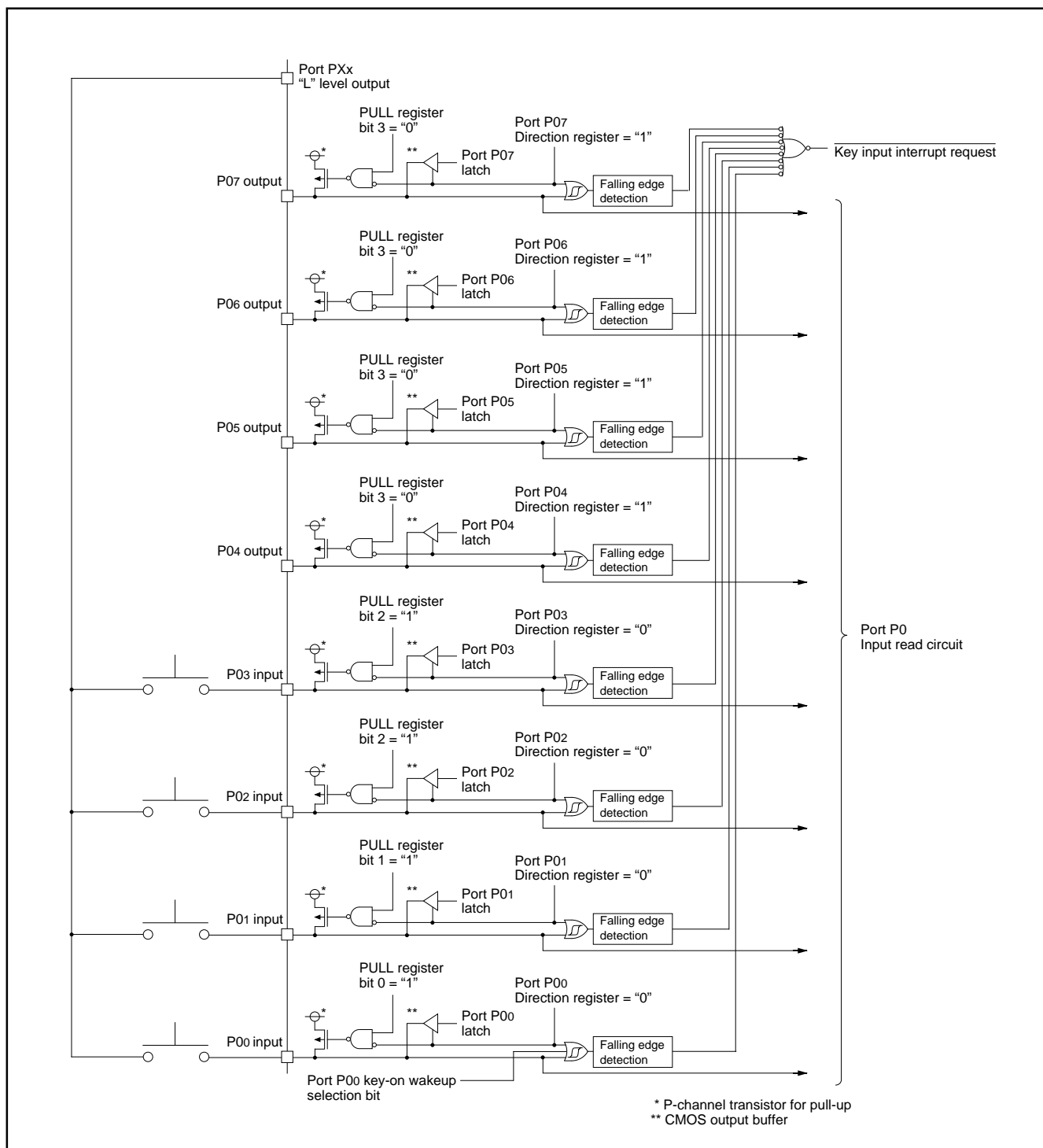
Fig. 19 Connection example when using key input interrupt and port P0 block diagram

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Timers

The 7544 Group has 3 timers: timer 1, timer A and timer X.

The division ratio of every timer and prescaler is $1/(n+1)$ provided that the value of the timer latch or prescaler is n.

All the timers are down count timers. When a timer reaches "0", an underflow occurs at the next count pulse, and the corresponding timer latch is reloaded into the timer. When a timer underflows, the interrupt request bit corresponding to each timer is set to "1".

● Timer 1

Timer 1 is an 8-bit timer and counts the prescaler output.

When Timer 1 underflows, the timer 1 interrupt request bit is set to "1".

Prescaler 1 is an 8-bit prescaler and counts the signal selected by the timer 1 count source selection bit.

Prescaler 1 and Timer 1 have the prescaler 1 latch and the timer 1 latch to retain the reload value, respectively. The value of prescaler 1 latch is set to Prescaler 1 when Prescaler 1 underflows. The value of timer 1 latch is set to Timer 1 when Timer 1 underflows.

When writing to Prescaler 1 (PRE1) is executed, the value is written to both the prescaler 1 latch and Prescaler 1.

When writing to Timer 1 (T1) is executed, the value is written to both the timer 1 latch and Timer 1.

When reading from Prescaler 1 (PRE1) and Timer 1 (T1) is executed, each count value is read out.

Timer 1 always operates in the timer mode.

Prescaler 1 counts the signal selected by the timer 1 count source selection bit. Each time the count clock is input, the contents of Prescaler 1 is decremented by 1. When the contents of Prescaler 1 reach "00_{16}", an underflow occurs at the next count clock, and the prescaler 1 latch is reloaded into Prescaler 1 and count continues. The division ratio of Prescaler 1 is $1/(n+1)$ provided that the value of Prescaler 1 is n.

The contents of Timer 1 is decremented by 1 each time the underflow signal of Prescaler 1 is input. When the contents of Timer 1 reach "00_{16}", an underflow occurs at the next count clock, and the timer 1 latch is reloaded into Timer 1 and count continues. The division ratio of Timer 1 is $1/(m+1)$ provided that the value of Timer 1 is m. Accordingly, the division ratio of Prescaler 1 and Timer 1 is $1/((n+1)\times(m+1))$ provided that the value of Prescaler 1 is n and the value of Timer 1 is m.

Timer 1 cannot stop counting by software.

● Timer A

Timer A is a 16-bit timer and counts the signal selected by the timer A count source selection bit. When Timer A underflows, the timer A interrupt request bit is set to "1".

Timer A consists of the low-order of Timer A (TAL) and the high-order of Timer A (TAH).

Timer A has the timer A latch to retain the reload value. The value of timer A latch is set to Timer A at the timing shown below.
• When Timer A undeflows.
• When an active edge is input from CNTR1 pin (valid only when period measurement mode and pulse width HL continuously measurement mode).

When writing to both the low-order of Timer A (TAL) and the high-order of Timer A (TAH) is executed, the value is written to both the timer A latch and Timer A.

When reading from the low-order of Timer A (TAL) and the high-order of Timer A (TAH) is executed, the following values are read out according to the operating mode.
• In timer mode, event counter mode:
The count value of Timer A is read out.
• In period measurement mode, pulse width HL continuously measurement mode:
The measured value is read out.

Be sure to write to/read out the low-order of Timer A (TAL) and the high-order of Timer A (TAH) in the following order;

Read
Read the high-order of Timer A (TAH) first, and the low-order of Timer A (TAL) next and be sure to read out both TAH and TAL.

Write
Write to the low-order of Timer A (TAL) first, and the high-order of Timer A (TAH) next and be sure to write to both TAL and TAH.

Timer A can be selected in one of 4 operating modes by setting the timer A mode register.

(1) Timer mode

Timer A counts the selected by the timer A count source selection bit. Each time the count clock is input, the contents of Timer A is decremented by 1. When the contents of Timer A reach "0000_{16}", an underflow occurs at the next count clock, and the timer A latch is reloaded into Timer A. The division ratio of Timer A is $1/(n+1)$ provided that the value of Timer A is n.

(2) Period measurement mode

In the period measurement mode, the pulse period input from the P00/CNTR1 pin is measured.

CNTR1 interrupt request is generated at rising/falling edge of CNTR1 pin input singal. Simultaneously, the value in the timer A latch is reloaded inTimer A and count continues. The active edge of CNTR1 pin input signal can be selected from rising or falling by the CNTR1 active edge switch bit .The count value when trigger input from CNTR1 pin is accepted is retained until Timer A is read once.

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(3) Event counter mode
Timer A counts signals input from the P0₀/CNTR₁ pin.
Except for this, the operation in event counter mode is the same as in timer mode.
The active edge of CNTR₁ pin input signal can be selected from rising or falling by the CNTR₁ active edge switch bit .

(4) Pulse width HL continuously measurement mode
In the pulse width HL continuously measurement mode, the pulse width ("H" and "L" levels) input to the P0₀/CNTR₁ pin is measured. CNTR₁ interrupt request is generated at both rising and falling edges of CNTR₁ pin input signal. Except for this, the operation in pulse width HL continuously measurement mode is the same as in period measurement mode.
The count value when trigger input from the CNTR₁ pin is accepted is retained until Timer A is read once.

Timer A can stop counting by setting "1" to the timer A count stop bit in any mode.
Also, when Timer A underflows, the timer A interrupt request bit is set to "1".

Note on Timer A is described below;

■ **Note on Timer A**
CNTR₁ interrupt active edge selection
CNTR₁ interrupt active edge depends on the CNTR₁ active edge switch bit.
When this bit is "0", the CNTR₁ interrupt request bit is set to "1" at the falling edge of the CNTR₁ pin input signal. When this bit is "1", the CNTR₁ interrupt request bit is set to "1" at the rising edge of the CNTR₁ pin input signal.
However, in the pulse width HL continuously measurement mode, CNTR₁ interrupt request is generated at both rising and falling edges of CNTR₁ pin input signal regardless of the setting of CNTR₁ active edge switch bit.
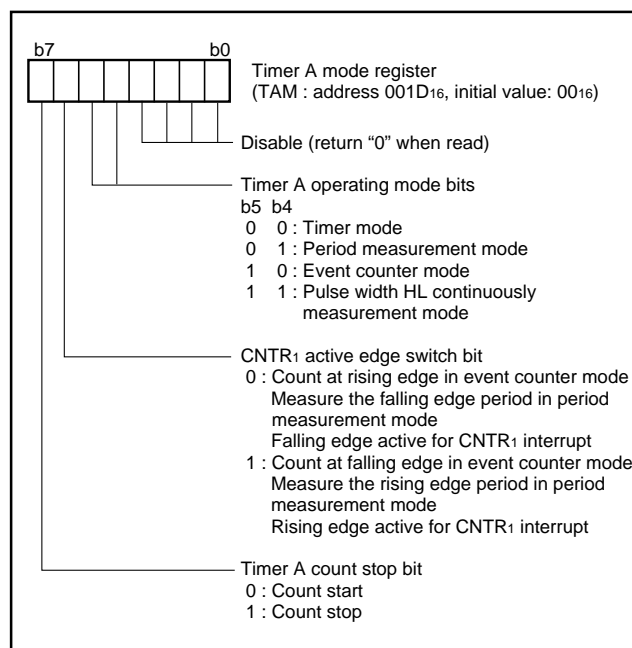
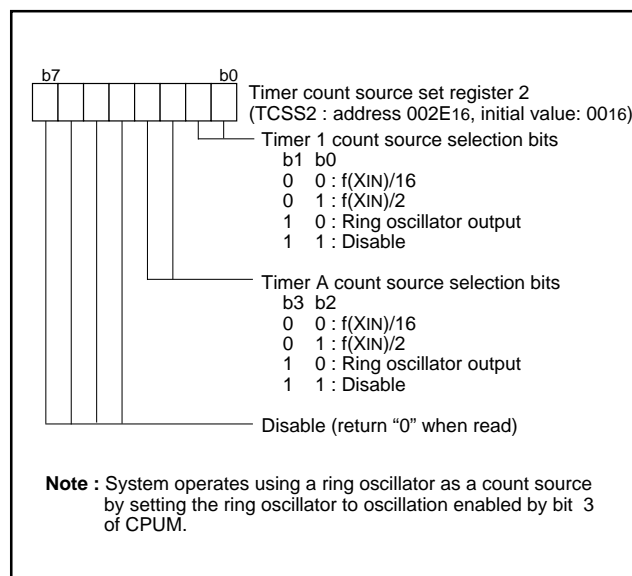**Fig. 20 Structure of timer A mode register**

Fig. 21 Timer count source set register 2

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Notice: This is not a final specification.
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●Timer X

Timer X is an 8-bit timer and counts the prescaler X output.

When Timer X underflows, the timer X interrupt request bit is set to "1".

Prescaler X is an 8-bit prescaler and counts the signal selected by the timer X count source selection bit.

Prescaler X and Timer X have the prescaler X latch and the timer X latch to retain the reload value, respectively. The value of prescaler X latch is set to Prescaler X when Prescaler X underflows. The value of timer X latch is set to Timer X when Timer X underflows.

When writing to Prescaler X (PREX) and Timer X (TX) is executed, writing to "latch only" or "latch and prescaler (timer)" can be selected by the setting value of the timer X write control bit.

When reading from Prescaler X (PREX) and Timer X (TX) is executed, each count value is read out.

Timer X can be selected in one of 4 operating modes by setting the timer X operating mode bits of the timer X mode register.

(1) Timer mode

Prescaler X counts the count source selected by the timer X count source selection bits. Each time the count clock is input, the contents of Prescaler X is decremented by 1. When the contents of Prescaler X reach "00_{16}", an underflow occurs at the next count clock, and the prescaler X latch is reloaded into Prescaler X and count continues. The division ratio of Prescaler X is 1/(n+1) provided that the value of Prescaler X is n.

The contents of Timer X is decremented by 1 each time the underflow signal of Prescaler X is input. When the contents of Timer X reach "00_{16}", an underflow occurs at the next count clock, and the timer X latch is reloaded into Timer X and count continues. The division ratio of Timer X is 1/(m+1) provided that the value of Timer X is m. Accordingly, the division ratio of Prescaler X and Timer X is 1/((n+1)✕(m+1)) provided that the value of Prescaler X is n and the value of Timer X is m.

(2) Pulse output mode

In the pulse output mode, the waveform whose polarity is inverted each time timer X underflows is output from the CNTR0 pin.

The output level of CNTR0 pin can be selected by the CNTR0 active edge switch bit. When the CNTR0 active edge switch bit is "0", the output of CNTR0 pin is started at "H" level. When this bit is "1", the output is started at "L" level.

Also, the inverted waveform of pulse output from CNTR0 pin can be output from TXOUT pin by setting "1" to the P03/TXOUT output valid bit.

When using a timer in this mode, set the port P14 and P03 direction registers to output mode.

(3) Event counter mode

The timer A counts signals input from the P14/CNTR0 pin.

Except for this, the operation in event counter mode is the same as in timer mode.

The active edge of CNTR0 pin input signal can be selected from rising or falling by the CNTR0 active edge switch bit .

(4) Pulse width measurement mode

In the pulse width measurement mode, the pulse width of the signal input to P14/CNTR0 pin is measured.

The operation of Timer X can be controlled by the level of the signal input from the CNTR0 pin.

When the CNTR0 active edge switch bit is "0", the signal selected by the timer X count source selection bit is counted while the input signal level of CNTR0 pin is "H". The count is stopped while the pin is "L". Also, when the CNTR0 active edge switch bit is "1", the signal selected by the timer X count source selection bit is counted while the input signal level of CNTR0 pin is "L". The count is stopped while the pin is "H".

Timer X can stop counting by setting "1" to the timer X count stop bit in any mode.

Also, when Timer X underflows, the timer X interrupt request bit is set to "1".

Note on Timer X is described below;

■ Note on Timer X

CNTR0 interrupt active edge selection

CNTR0 interrupt active edge depends on the CNTR0 active edge switch bit.

When this bit is "0", the CNTR0 interrupt request bit is set to "1" at the falling edge of CNTR0 pin input signal. When this bit is "1", the CNTR0 interrupt request bit is set to "1" at the rising edge of CNTR0 pin input signal.
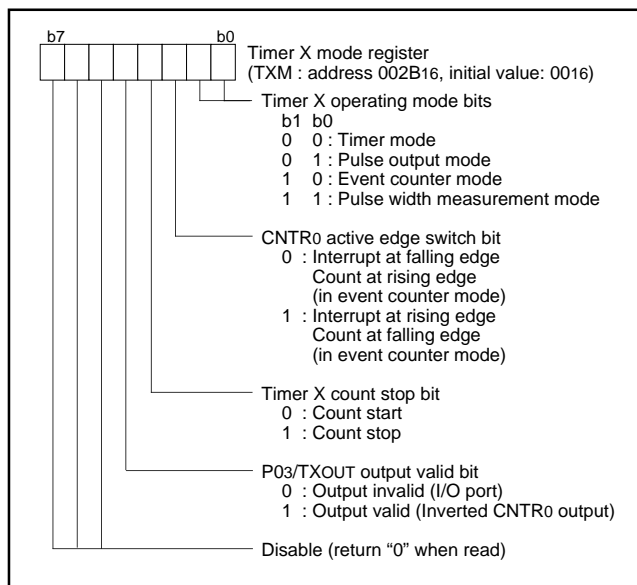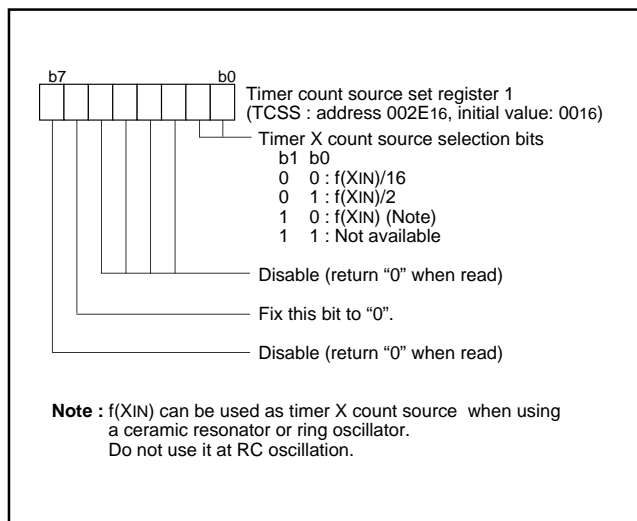
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Fig. 22 Structure of timer X mode register

b7 ... b0

Timer X mode register
(TXM : address 002B16, initial value: 0016)

Timer X operating mode bits
b1 b0
0 0 : Timer mode
0 1 : Pulse output mode
1 0 : Event counter mode
1 1 : Pulse width measurement mode

CNTR0 active edge switch bit
0 : Interrupt at falling edge
Count at rising edge
(in event counter mode)
1 : Interrupt at rising edge
Count at falling edge
(in event counter mode)

Timer X count stop bit
0 : Count start
1 : Count stop

P03/TXOUT output valid bit
0 : Output invalid (I/O port)
1 : Output valid (Inverted CNTR0 output)

Disable (return "0" when read)

Fig. 23 Timer count source set register

b7 ... b0

Timer count source set register 1
(TCSS : address 002E16, initial value: 0016)

Timer X count source selection bits
b1 b0
0 0 : f(XIN)/16
0 1 : f(XIN)/2
1 0 : f(XIN) (Note)
1 1 : Not available

Disable (return "0" when read)

Fix this bit to "0".

Disable (return "0" when read)

Note : f(XIN) can be used as timer X count source when using
a ceramic resonator or ring oscillator.
Do not use it at RC oscillation.

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Fig. 24 Block diagram of timer 1 and timer A

Fig. 25 Block diagram of timer X

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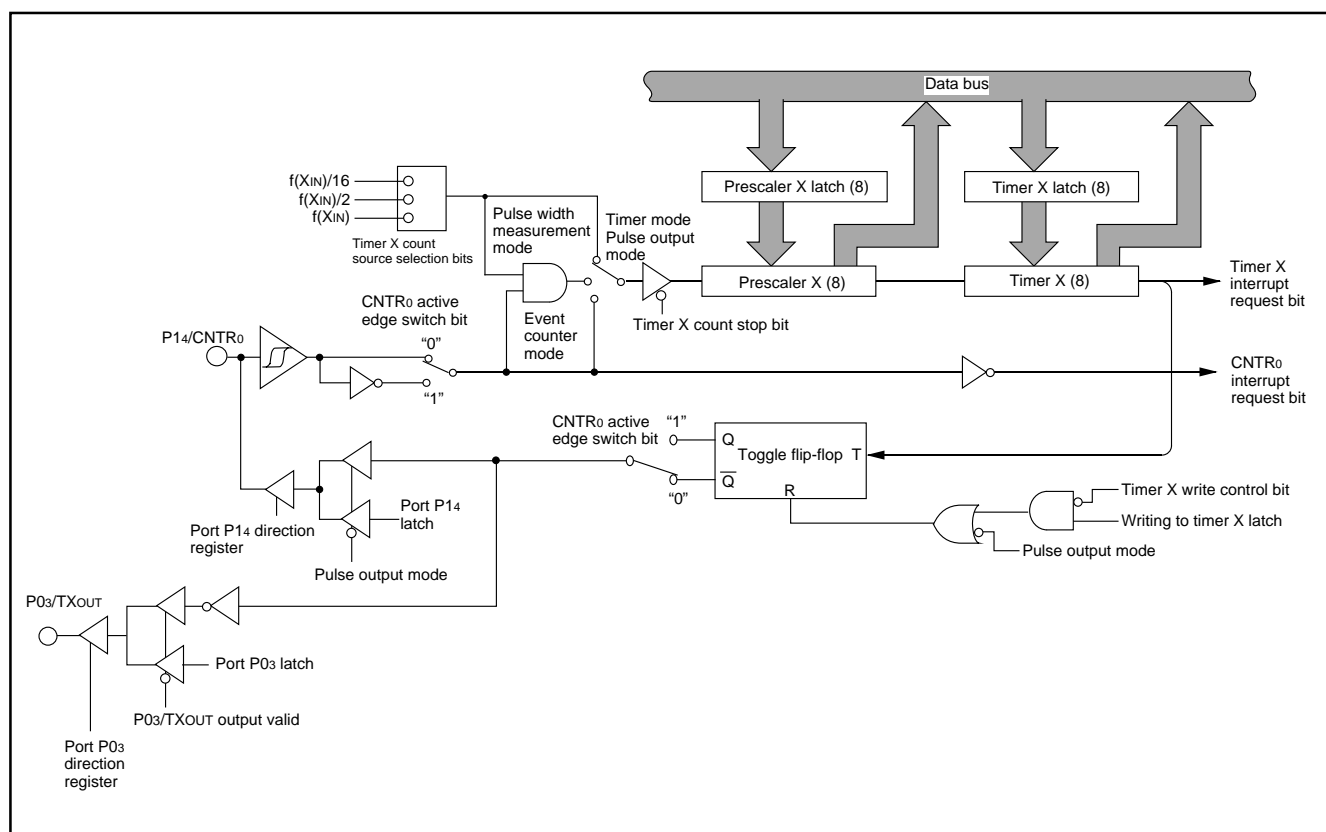Notice: This is not a final specification.
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Serial I/O
●Serial I/O

Serial I/O can be used as either clock synchronous or asynchronous (UART) serial I/O. A dedicated timer is also provided for baud rate generation.

(1) Clock Synchronous Serial I/O Mode

Clock synchronous serial I/O mode can be selected by setting the serial I/O mode selection bit of the serial I/O control register (bit 6) to "1".

For clock synchronous serial I/O, the transmitter and the receiver must use the same clock. If an internal clock is used, transfer is started by a write signal to the TB/RB.
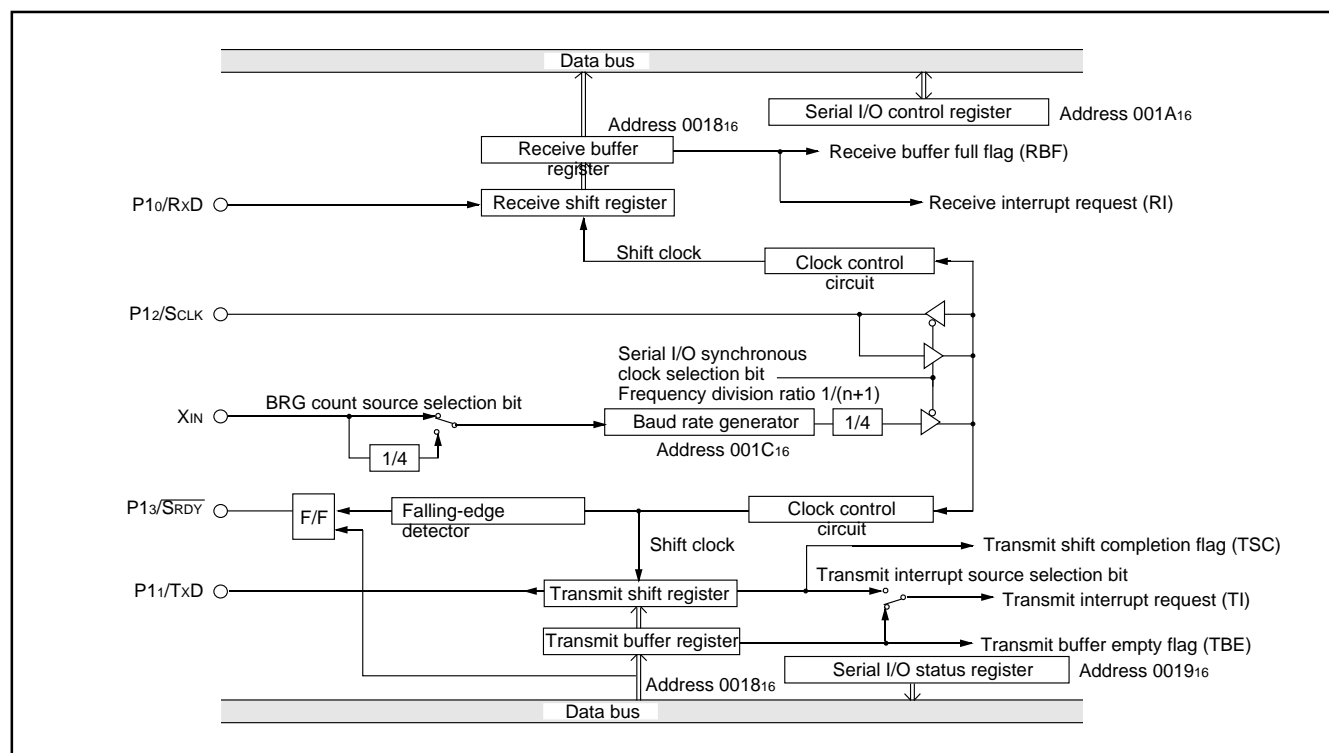
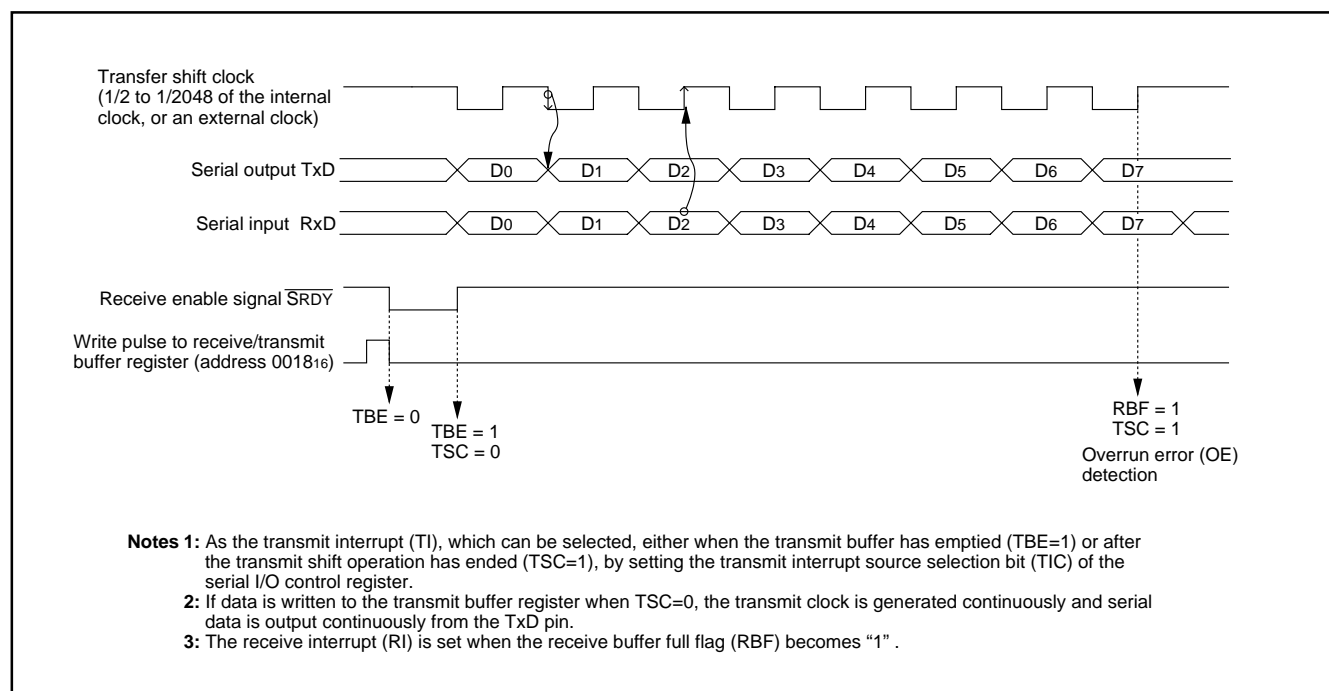**Fig. 26 Block diagram of clock synchronous serial I/O**

Fig. 27 Operation of clock synchronous serial I/O function

Notes 1: As the transmit interrupt (TI), which can be selected, either when the transmit buffer has emptied (TBE=1) or after the transmit shift operation has ended (TSC=1), by setting the transmit interrupt source selection bit (TIC) of the serial I/O control register.
2: If data is written to the transmit buffer register when TSC=0, the transmit clock is generated continuously and serial data is output continuously from the TxD pin.
3: The receive interrupt (RI) is set when the receive buffer full flag (RBF) becomes "1".

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Some parametric limits are subject to change.

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(2) Asynchronous Serial I/O (UART) Mode

Clock asynchronous serial I/O mode (UART) can be selected by clearing the serial I/O mode selection bit of the serial I/O control register to "0".

Eight serial data transfer formats can be selected, and the transfer formats used by a transmitter and receiver must be identical.

The transmit and receive shift registers each have a buffer, but the two buffers have the same address in memory. Since the shift register cannot be written to or read from directly, transmit data is written to the transmit buffer register, and receive data is read from the receive buffer register.

The transmit buffer register can also hold the next data to be transmitted, and the receive buffer register can hold a character while the next character is being received.
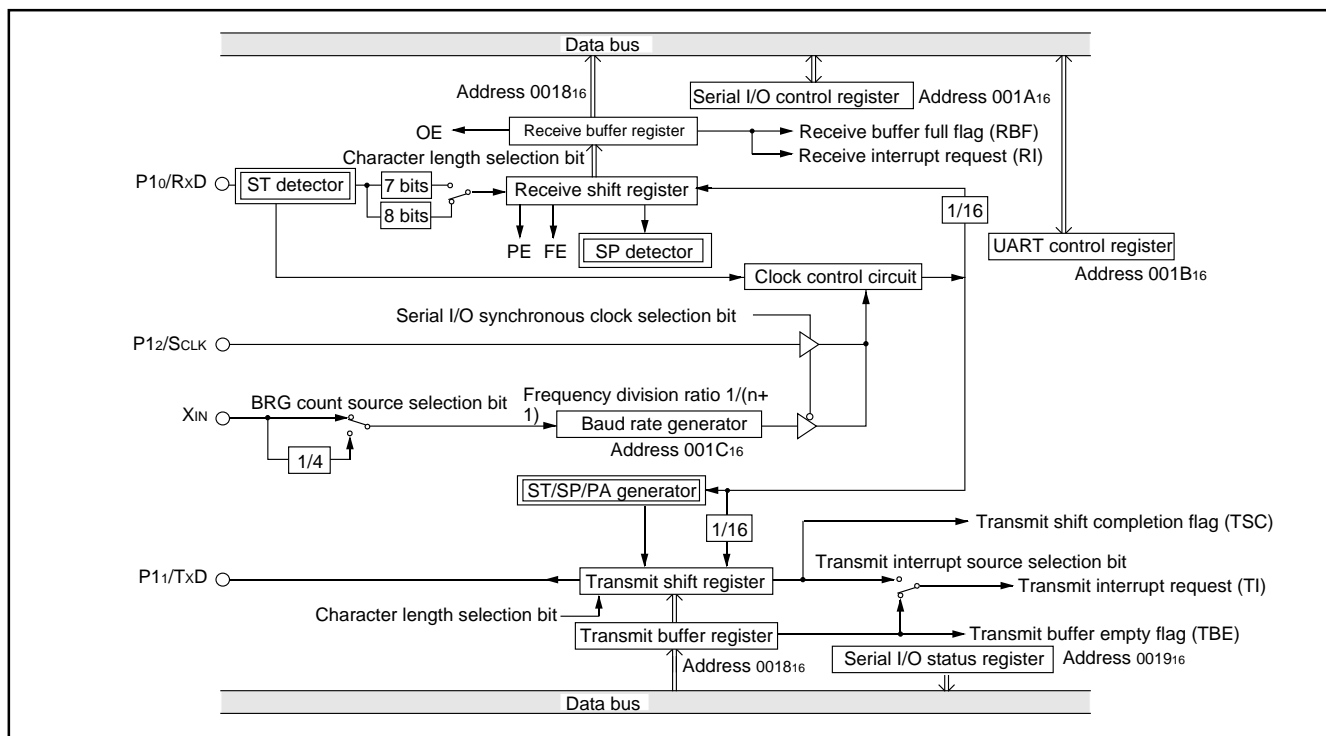

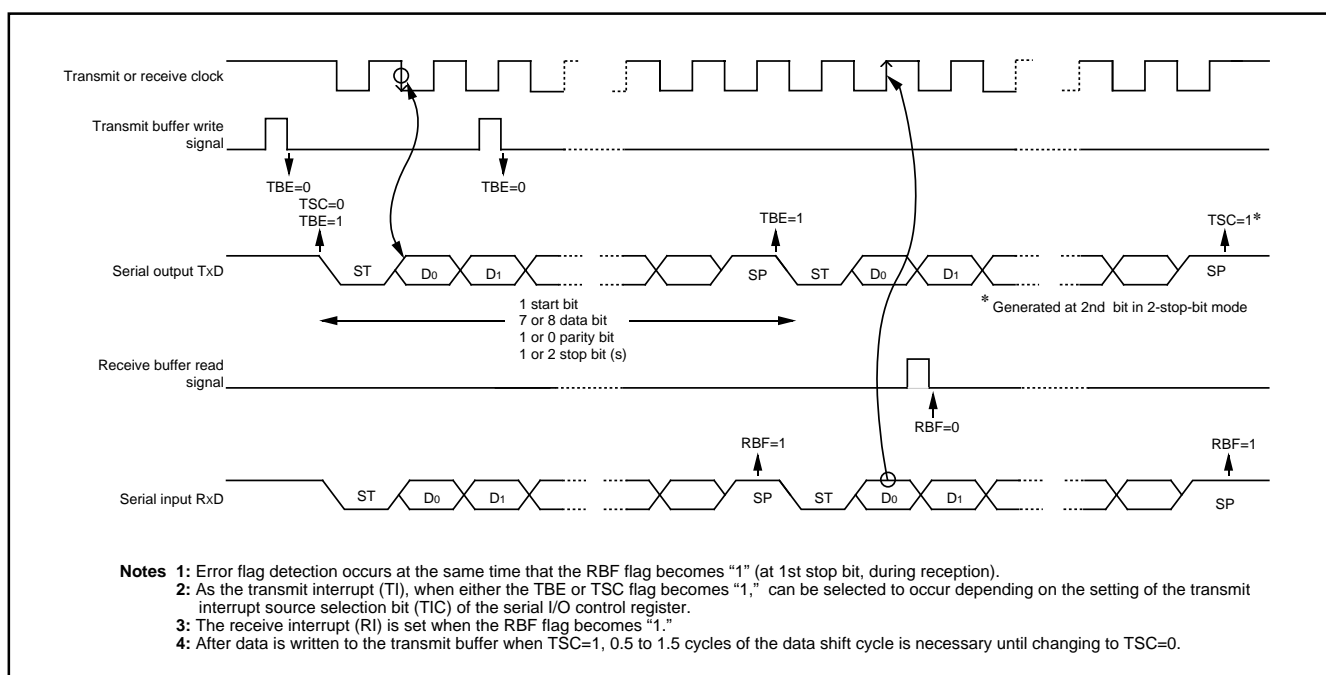**Fig. 28 Block diagram of UART serial I/O**

Notes 1: Error flag detection occurs at the same time that the RBF flag becomes "1" (at 1st stop bit, during reception).
2: As the transmit interrupt (TI), when either the TBE or TSC flag becomes "1," can be selected to occur depending on the setting of the transmit interrupt source selection bit (TIC) of the serial I/O control register.
3: The receive interrupt (RI) is set when the RBF flag becomes "1."
4: After data is written to the transmit buffer when TSC=1, 0.5 to 1.5 cycles of the data shift cycle is necessary until changing to TSC=0.

Fig. 29 Operation of UART serial I/O function

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[Transmit buffer register/receive buffer register (TB/RB)] 0018₁₆

The transmit buffer register and the receive buffer register are located at the same address. The transmit buffer is write-only and the receive buffer is read-only. If a character bit length is 7 bits, the MSB of data stored in the receive buffer is "0".

[Serial I/O status register (SIOSTS)] 0019₁₆

The read-only serial I/O status register consists of seven flags (bits 0 to 6) which indicate the operating status of the serial I/O function and various errors.

Three of the flags (bits 4 to 6) are valid only in UART mode.

The receive buffer full flag (bit 1) is cleared to "0" when the receive buffer register is read.

If there is an error, it is detected at the same time that data is transferred from the receive shift register to the receive buffer register, and the receive buffer full flag is set. A write to the serial I/O status register clears all the error flags OE, PE, FE, and SE (bit 3 to bit 6, respectively). Writing "0" to the serial I/O enable bit SIOE (bit 7 of the serial I/O control register) also clears all the status flags, including the error flags.

Bits 0 to 6 of the serial I/O status register are initialized to "0" at reset, but if the transmit enable bit of the serial I/O control register has been set to "1", the transmit shift completion flag (bit 2) and the transmit buffer empty flag (bit 0) become "1".

[Serial I/O control register (SIOCON)] 001A₁₆

The serial I/O control register consists of eight control bits for the serial I/O function.

[UART control register (UARTCON)] 001B₁₆

The UART control register consists of four control bits (bits 0 to 3) which are valid when asynchronous serial I/O is selected and set the data format of an data transfer and one bit (bit 4) which is always valid and sets the output structure of the P1₁/TXD pin.

[Baud rate generator (BRG)] 001C₁₆

The baud rate generator determines the baud rate for serial transfer. The baud rate generator divides the frequency of the count source by $1/(n + 1)$, where n is the value written to the baud rate generator.

■ **Notes on serial I/O**

• Serial I/O interrupt

When setting the transmit enable bit to "1", the serial I/O transmit interrupt request bit is automatically set to "1". When not requiring the interrupt occurrence synchronized with the transmission enabled, take the following sequence.

① Set the serial I/O transmit interrupt enable bit to "0" (disabled).

② Set the transmit enable bit to "1".

③ Set the serial I/O transmit interrupt request bit to "0" after 1 or more instructions have been executed.

④ Set the serial I/O transmit interrupt enable bit to "1" (enabled).

• I/O pin function when serial I/O is enabled.

The functions of P1₂ and P1₃ are switched with the setting values of a serial I/O mode selection bit and a serial I/O synchronous clock selection bit as follows.

(1) Serial I/O mode selection bit → "1" :

Clock synchronous type serial I/O is selected.

Setup of a serial I/O synchronous clock selection bit

"0" : P1₂ pin turns into an output pin of a synchronous clock.

"1" : P1₂ pin turns into an input pin of a synchronous clock.

Setup of a SRDY output enable bit (SRDY)

"0" : P1₃ pin can be used as a normal I/O pin.

"1" : P1₃ pin turns into a SRDY output pin.
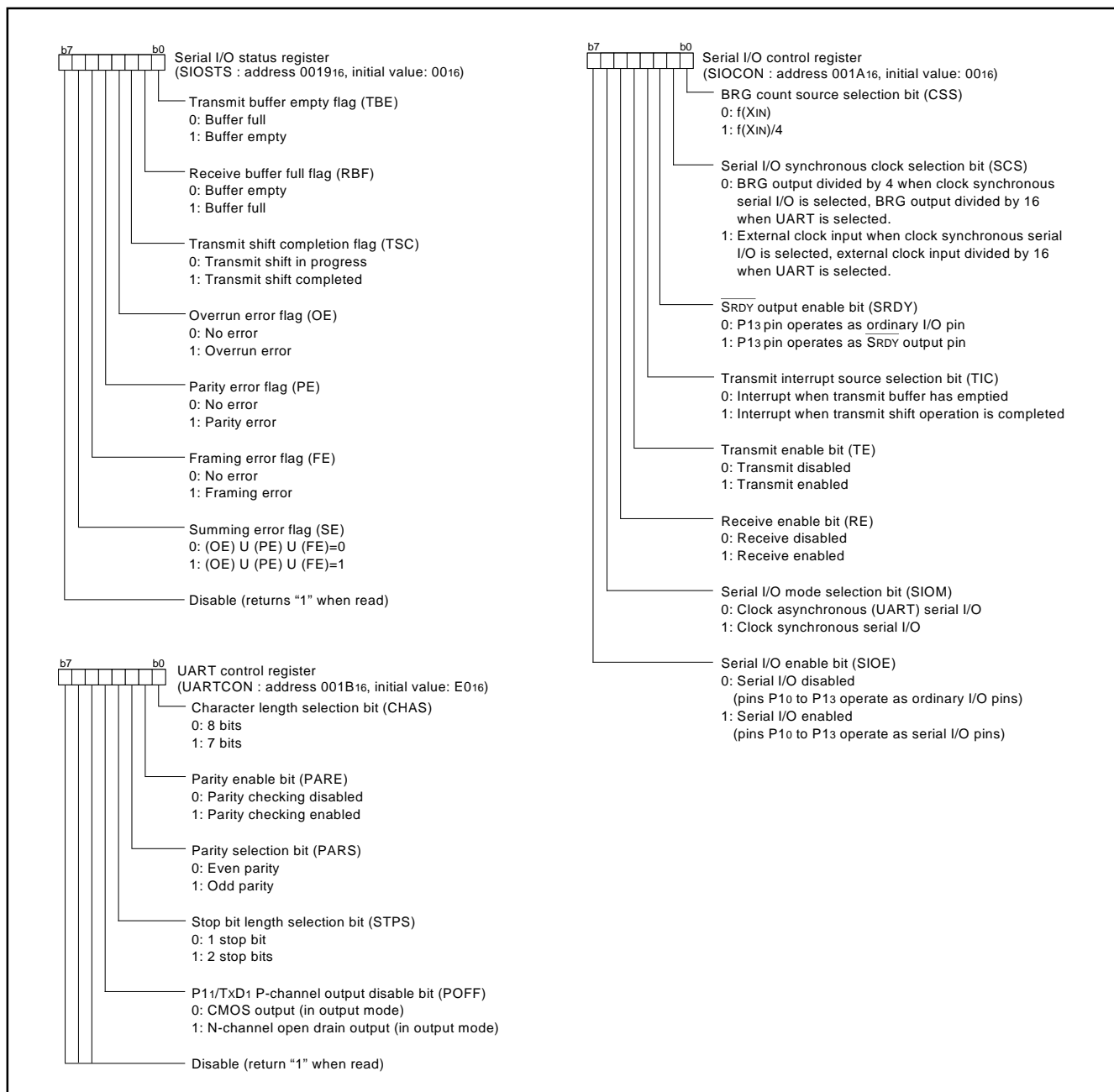
(2) Serial I/O mode selection bit → "0" :

Clock asynchronous (UART) type serial I/O is selected.

Setup of a serial I/O synchronous clock selection bit

"0": P1₂ pin can be used as a normal I/O pin.

"1": P1₂ pin turns into an input pin of an external clock.

When clock asynchronous (UART) type serial I/O is selected, it is P1₃ pin. It can be used as a normal I/O pin.

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Notice: This is not a final specification.
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Serial I/O status register
(SIOSTS : address 0019_{16}, initial value: 00_{16})

Transmit buffer empty flag (TBE)
0: Buffer full
1: Buffer empty

Receive buffer full flag (RBF)
0: Buffer empty
1: Buffer full

Transmit shift completion flag (TSC)
0: Transmit shift in progress
1: Transmit shift completed

Overrun error flag (OE)
0: No error
1: Overrun error

Parity error flag (PE)
0: No error
1: Parity error

Framing error flag (FE)
0: No error
1: Framing error

Summing error flag (SE)
0: (OE) U (PE) U (FE)=0
1: (OE) U (PE) U (FE)=1

Disable (returns "1" when read)

Serial I/O control register
(SIOCON : address $001A_{16}$, initial value: 00_{16})

BRG count source selection bit (CSS)
0: $f(X_{IN})$
1: $f(X_{IN})/4$

Serial I/O synchronous clock selection bit (SCS)
0: BRG output divided by 4 when clock synchronous
   serial I/O is selected, BRG output divided by 16
   when UART is selected.
1: External clock input when clock synchronous serial
   I/O is selected, external clock input divided by 16
   when UART is selected.

$\overline{SRDY}$ output enable bit (SRDY)
0: P1$_3$ pin operates as ordinary I/O pin
1: P1$_3$ pin operates as $\overline{SRDY}$ output pin

Transmit interrupt source selection bit (TIC)
0: Interrupt when transmit buffer has emptied
1: Interrupt when transmit shift operation is completed

Transmit enable bit (TE)
0: Transmit disabled
1: Transmit enabled

Receive enable bit (RE)
0: Receive disabled
1: Receive enabled

Serial I/O mode selection bit (SIOM)
0: Clock asynchronous (UART) serial I/O
1: Clock synchronous serial I/O

Serial I/O enable bit (SIOE)
0: Serial I/O disabled
   (pins P1$_0$ to P1$_3$ operate as ordinary I/O pins)
1: Serial I/O enabled
   (pins P1$_0$ to P1$_3$ operate as serial I/O pins)

UART control register
(UARTCON : address $001B_{16}$, initial value: $E0_{16}$)

Character length selection bit (CHAS)
0: 8 bits
1: 7 bits

Parity enable bit (PARE)
0: Parity checking disabled
1: Parity checking enabled

Parity selection bit (PARS)
0: Even parity
1: Odd parity

Stop bit length selection bit (STPS)
0: 1 stop bit
1: 2 stop bits

P1$_1$/TxD$_1$ P-channel output disable bit (POFF)
0: CMOS output (in output mode)
1: N-channel open drain output (in output mode)

Disable (return "1" when read)

Fig. 30 Structure of serial I/O-related registers

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A-D Converter

The functional blocks of the A-D converter are described below.

[A-D conversion register] AD

The A-D conversion register is a read-only register that stores the result of A-D conversion. Do not read out this register during an A-D conversion.

[A-D control register] ADCON

The A-D control register controls the A-D converter. Bit 2 to 0 are analog input pin selection bits. Bit 4 is the AD conversion completion bit. The value of this bit remains at "0" during A-D conversion, and changes to "1" at completion of A-D conversion.

A-D conversion is started by setting this bit to "0".

[Comparison voltage generator]

The comparison voltage generator divides the voltage between AV_{SS} and V_{REF} by 256, and outputs the divided voltages.

[Channel selector]

The channel selector selects one of ports $P2_5/AN_5$ to $P2_0/AN_0$, and inputs the voltage to the comparator.

[Comparator and control circuit]

The comparator and control circuit compares an analog input voltage with the comparison voltage and stores its result into the A-D conversion register. When A-D conversion is completed, the control circuit sets the AD conversion completion bit and the AD interrupt request bit to "1". Because the comparator is constructed linked to a capacitor, set $f(X_{IN})$ to 500 kHz or more during A-D conversion.
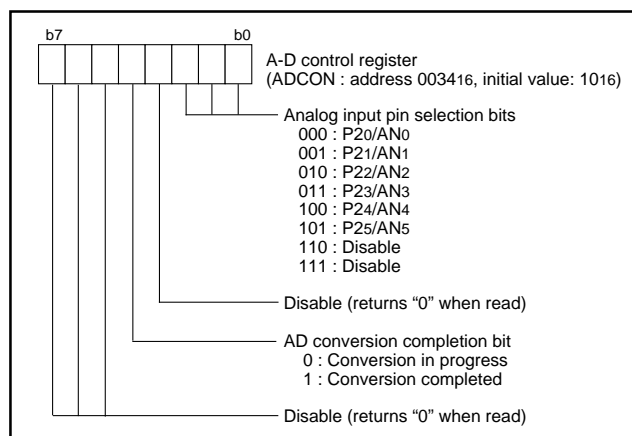
Fig. 31 Structure of A-D control register
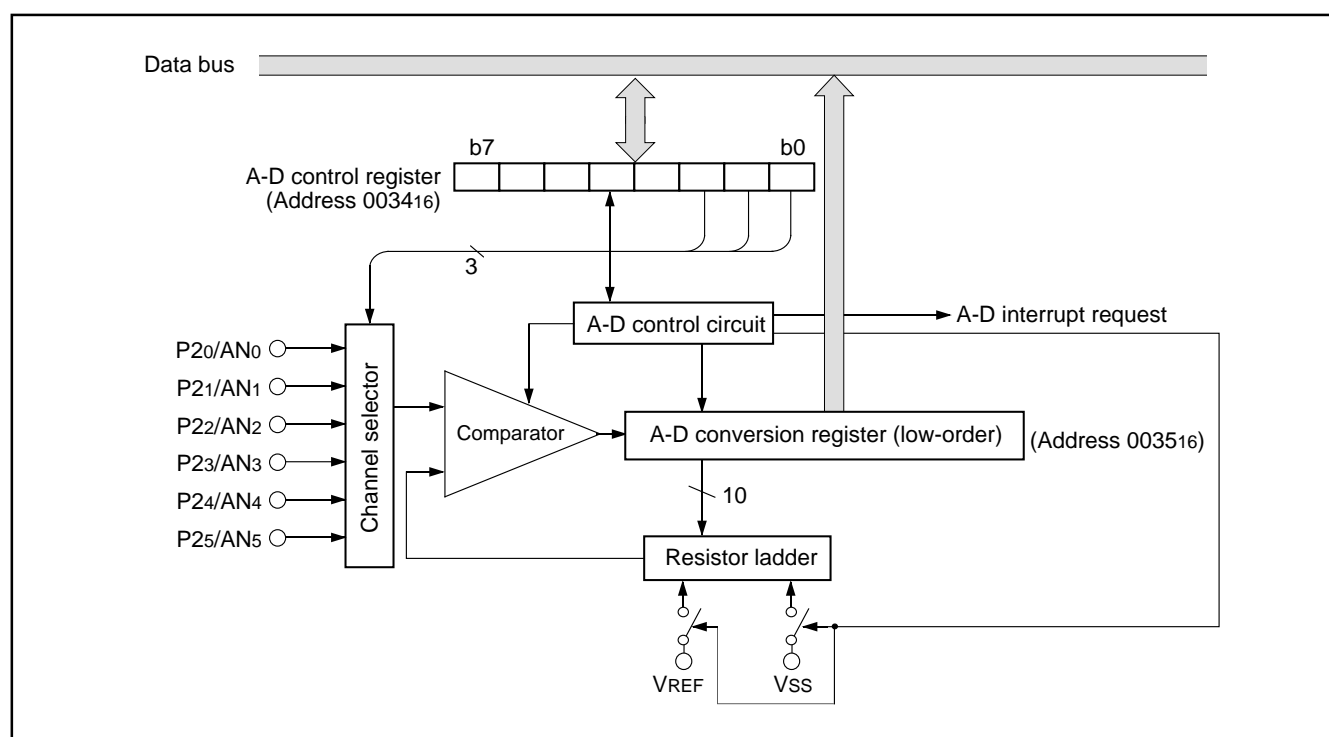
Fig. 32 Block diagram of A-D converter

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Watchdog Timer

The watchdog timer gives a means for returning to a reset status when the program fails to run on its normal loop due to a runaway. The watchdog timer consists of an 8-bit watchdog timer H and an 8-bit watchdog timer L, being a 16-bit counter.

Standard operation of watchdog timer

The watchdog timer stops when the watchdog timer control register (address 0039_{16}) is not set after reset. Writing an optional value to the watchdog timer control register (address 0039_{16}) causes the watchdog timer to start to count down. When the watchdog timer H underflows, an internal reset occurs. Accordingly, it is programmed that the watchdog timer control register (address 0039_{16}) can be set before an underflow occurs.

When the watchdog timer control register (address 0039_{16}) is read, the values of the high-order 6-bit of the watchdog timer H, STP instruction disable bit and watchdog timer H count source selection bit are read.

Initial value of watchdog timer

By a reset or writing to the watchdog timer control register (address 0039_{16}), the watchdog timer H is set to "FF_{16}" and the watchdog timer L is set to "FF_{16}".

Operation of watchdog timer H count source selection bit

A watchdog timer H count source can be selected by bit 7 of the watchdog timer control register (address 0039_{16}). When this bit is "0", the count source becomes a watchdog timer L underflow signal. The detection time is 131.072 ms at f(X_{IN})=8 MHz.
When this bit is "1", the count source becomes f(X_{IN})/16. In this case, the detection time is 512 μs at f(X_{IN})=8 MHz.
This bit is cleared to "0" after reset.

Operation of STP instruction disable bit

When the watchdog timer is in operation, the STP instruction can be disabled by bit 6 of the watchdog timer control register (address 0039_{16}).
When this bit is "0", the STP instruction is enabled.
When this bit is "1", the STP instruction is disabled, and an internal reset occurs if the STP instruction is executed.
Once this bit is set to "1", it cannot be changed to "0" by program.
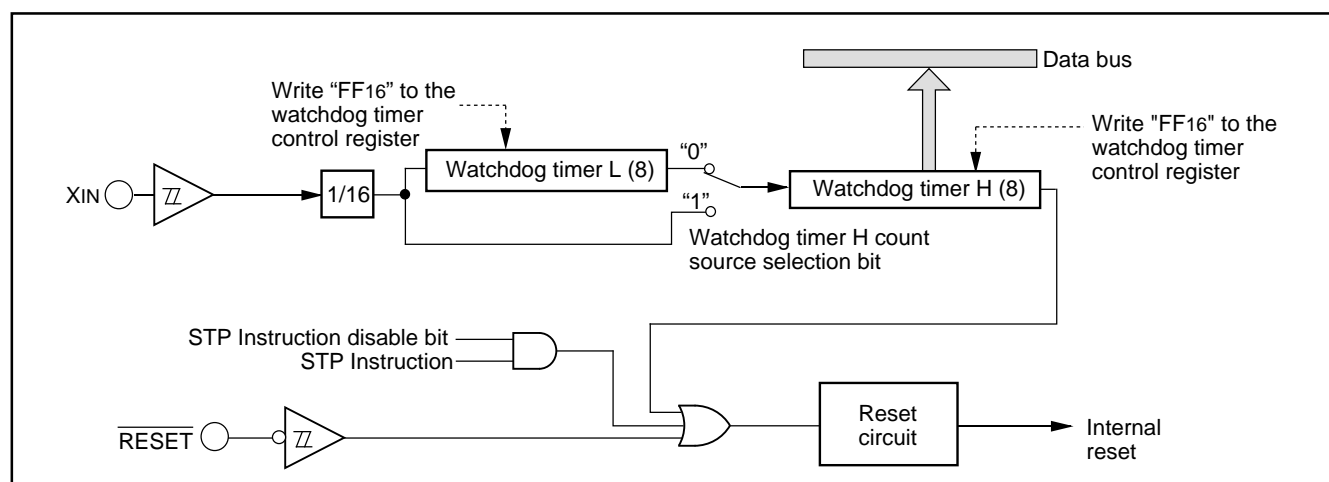This bit is cleared to "0" after reset.

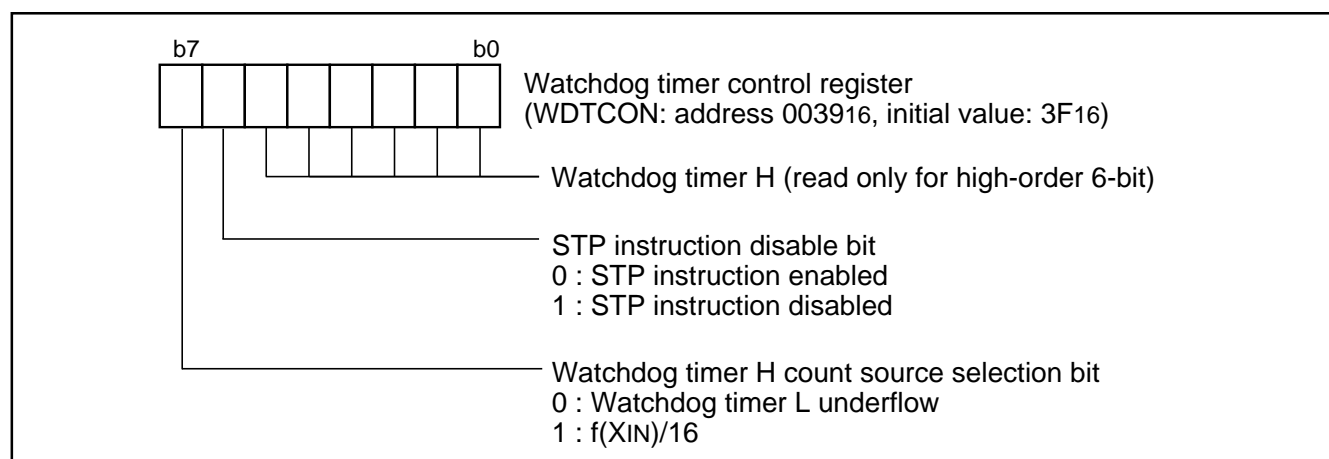**Fig. 33 Block diagram of watchdog timer**

Fig. 34 Structure of watchdog timer control register

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PRELIMINARY
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Reset Circuit

The microcomputer is put into a reset status by holding the $\overline{\text{RESET}}$ pin at the "L" level for 2 μs or more when the power source voltage is 4.5 to 5.5 V and X_{IN} is in stable oscillation.

After that, this reset status is released by returning the $\overline{\text{RESET}}$ pin to the "H" level. The program starts from the address having the contents of address FFFD16 as high-order address and the contents of address FFFC16 as low-order address.

In the case of f(φ) ≤ 8 MHz, the reset input voltage must be 0.9 V or less when the power source voltage passes 4.5 V.
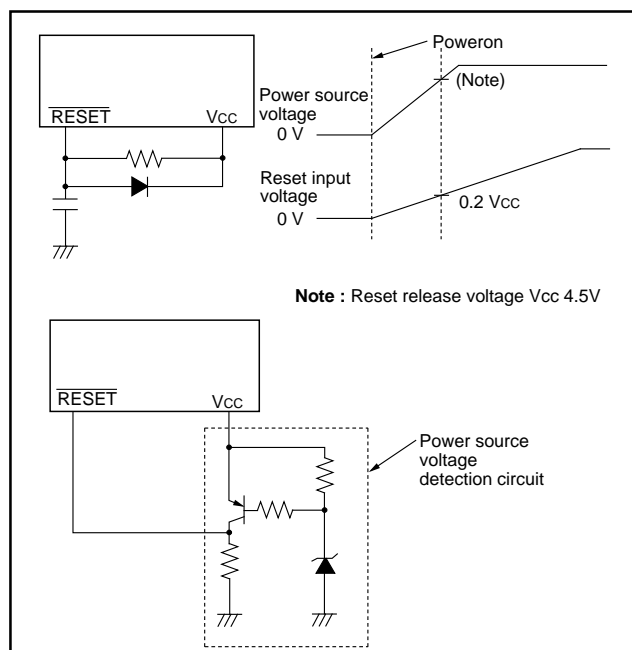
Fig. 35 Example of reset circuit
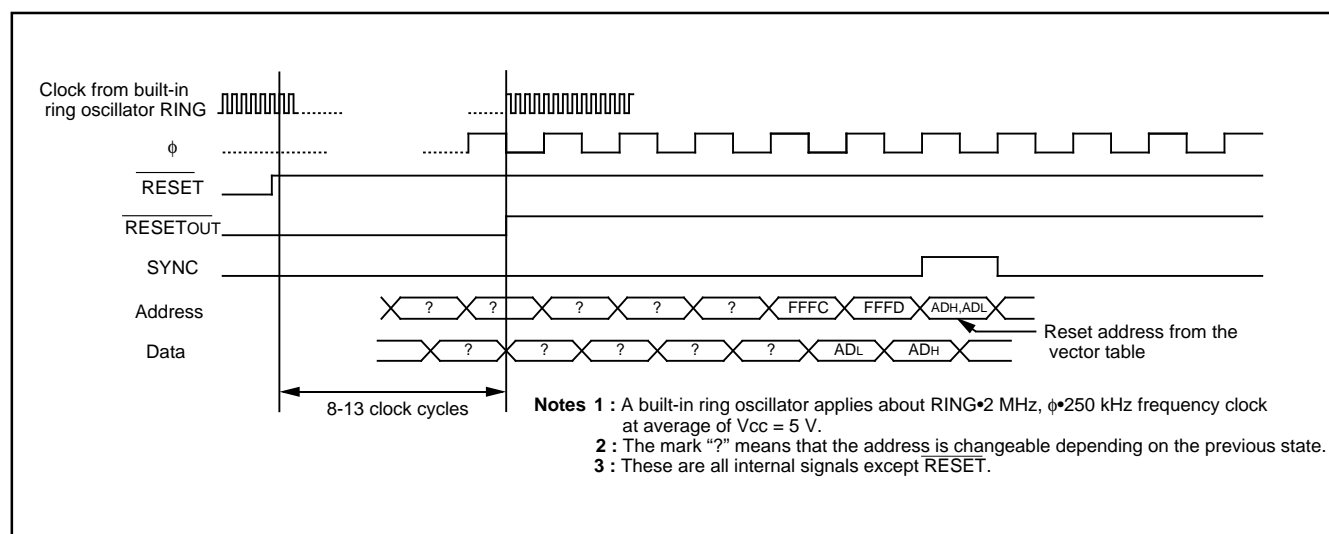
Fig. 36 Timing diagram at reset

Notes 1 : A built-in ring oscillator applies about RING•2 MHz, φ•250 kHz frequency clock at average of Vcc = 5 V.
2 : The mark "?" means that the address is changeable depending on the previous state.
3 : These are all internal signals except $\overline{\text{RESET}}$.

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		Address	Register contents
(1)	Port P0 direction register	0001_{16}	00_{16}
(2)	Port P1 direction register	0003_{16}	X X X 0 0 0 0 0
(3)	Port P2 direction register	0005_{16}	X X 0 0 0 0 0 0
(4)	Port P3 direction register	0007_{16}	0 X X 0 0 0 0 0
(5)	Pull-up control register	0016_{16}	00_{16}
(6)	Port P1P3 control register	0017_{16}	00_{16}
(7)	Serial I/O status register	0019_{16}	1 0 0 0 0 0 0 0
(8)	Serial I/O control register	$001A_{16}$	00_{16}
(9)	UART control registe	$001B_{16}$	1 1 1 0 0 0 0 0
(10)	Timer A mode register	$001D_{16}$	00_{16}
(11)	Timer A (low-order)	$001E_{16}$	FF_{16}
(12)	Timer A (high-order)	$001F_{16}$	FF_{16}
(13)	Prescaler 1	0028_{16}	FF_{16}
(14)	Timer 1	0029_{16}	0 0 0 0 0 0 0 1
(15)	Timer X mode register	$002B_{16}$	00_{16}
(16)	Prescaler X	$002C_{16}$	FF_{16}
(17)	Timer X	$002D_{16}$	FF_{16}
(18)	Timer count source set register 1	$002E_{16}$	00_{16}
(19)	Timer count source set register 2	$002F_{16}$	00_{16}
(20)	A-D control register	0034_{16}	0 0 0 1 0 0 0 0
(21)	MISRG	0038_{16}	00_{16}
(22)	Watchdog timer control register	0039_{16}	0 0 1 1 1 1 1 1
(23)	Interrupt edge selection register	$003A_{16}$	00_{16}
(24)	CPU mode register	$003B_{16}$	1 0 0 0 0 0 0 0
(25)	Interrupt request register 1	$003C_{16}$	00_{16}
(26)	Interrupt request register 2	$003D_{16}$	00_{16}
(27)	Interrupt control register 1	$003E_{16}$	00_{16}
(28)	Interrupt control register 2	$003F_{16}$	00_{16}
(29)	Processor status register	(PS) (	X X X X X 1 X X
(30)	Program counter	PCH)	Contents of address $FFFD_{16}$
		(PCL)	Contents of address $FFFC_{16}$

X : Undefined

The content of other registers is undefined when the microcomputer is reset.
The initial values must be surely set bifore you use it.

Fig. 37 Internal status of microcomputer at reset

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Notice: This is not a final specification.
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Clock Generating Circuit

An oscillation circuit can be formed by connecting a resonator between X_{IN} and X_{OUT}, and an RC oscillation circuit can be formed by connecting a resistor and a capacitor.

Use the circuit constants in accordance with the resonator manufacturer's recommended values.

(1) Ring oscillator operation

When the MCU operates by the ring oscillator for the main clock, connect X_{IN} pin to V_{CC} and leave X_{OUT} pin open.

The clock frequency of the ring oscillator depends on the supply voltage and the operation temperature range.

Be careful that variable frequencies when designing application products.

(2) Ceramic resonator and quartz-crystal oscillator

When the ceramic resonator and quartz-crystal oscillator is used for the main clock, connect the ceramic/quartz-crystal oscillator and the external circuit to pins X_{IN} and X_{OUT} at the shortest distance. A feedback resistor is built in between pins X_{IN} and X_{OUT}.

(3) RC oscillation

When the RC oscillation is used for the main clock, connect the X_{IN} pin and X_{OUT} pin to the external circuit of resistor R and the capacitor C at the shortest distance.

The frequency is affected by a capacitor, a resistor and a microcomputer.

So, set the constants within the range of the frequency limits.

(4) External clock

When the external signal clock is used for the main clock, connect the X_{IN} pin to the clock source and leave X_{OUT} pin open.

Note: The clock frequency of the ring oscillator depends on the supply voltage and the operation temperature range.
Be careful that variable frequencies and obtain the sufficient margin.
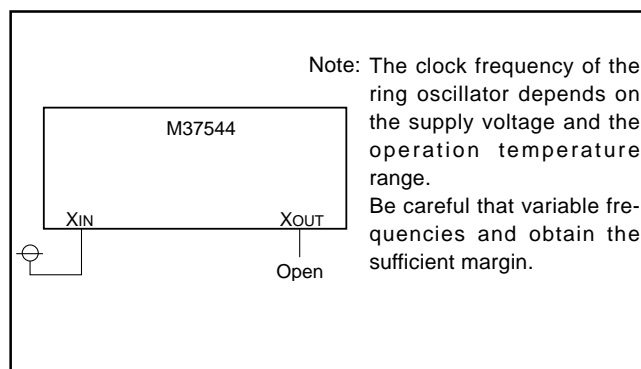
Fig. 38 Processing of X_{IN} and X_{OUT} pins at ring oscillator operation

Note: Externally connect a damping resistor Rd depending on the oscillation frequency.
(A feedback resistor is built-in.)
Use the resonator manufacturer's recommended value because constants such as capacitance depend on the resonator.
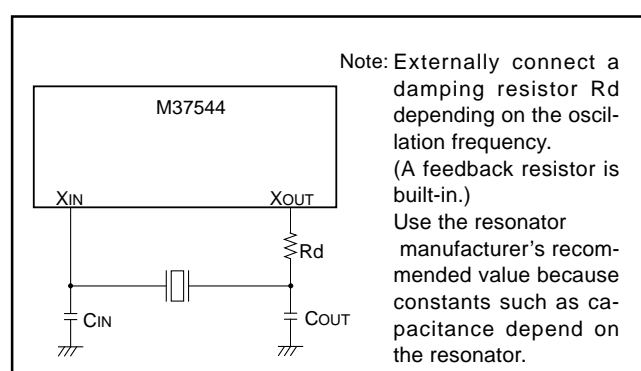
Fig. 39 External circuit of ceramic resonator and quartz-crystal oscillator

Note:
Connect the external circuit of resistor R and the capacitor C at the shortest distance.
The frequency is affected by a capacitor, a resistor and a microcomputer.
So, set the constants within the range of the frequency limits.
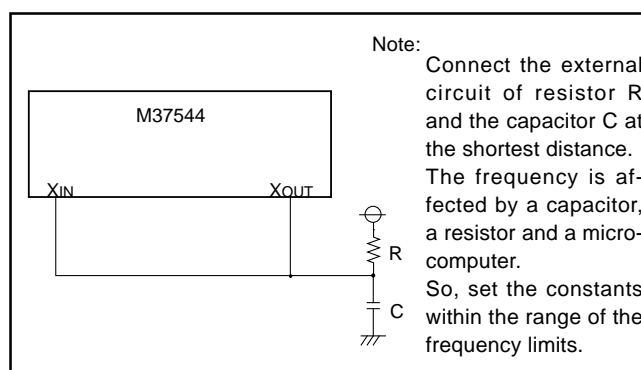
Fig. 40 External circuit of RC oscillation
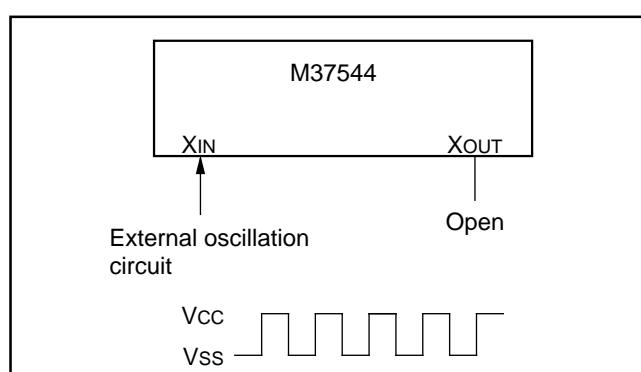
Fig. 41 External clock input circuit

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Notice: This is not a final specification.
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(1) Oscillation control
• Stop mode

When the STP instruction is executed, the internal clock ϕ stops at an "H" level and the X_{IN} oscillator stops. At this time, timer 1 is set to "01$_{16}$" and prescaler 1 is set to "FF$_{16}$" when the oscillation stabilization time set bit after release of the STP instruction is "0". On the other hand, timer 1 and prescaler 1 are not set when the above bit is "1". Accordingly, set the wait time fit for the oscillation stabilization time of the oscillator to be used. Single selected by the timer 1 count source selection bit is connected to the input of prescaler 1. When an external interrupt is accepted, oscillation is restarted but the internal clock ϕ remains at "H" until timer 1 underflows. As soon as timer 1 underflows, the internal clock ϕ is supplied. This is because when a ceramic/qruartz-crystal oscillator is used, some time is required until a start of oscillation. In case oscillation is restarted by reset, no wait time is generated. So apply an "L" level to the $\overline{RESET}$ pin while oscillation becomes stable. Also, the STP instruction cannot be used while CPU is operating by a ring oscillator.

• Wait mode

If the WIT instruction is executed, the internal clock ϕ stops at an "H" level, but the oscillator does not stop. The internal clock restarts if a reset occurs or when an interrupt is received. Since the oscillator does not stop, normal operation can be started immediately after the clock is restarted. To ensure that interrupts will be received to release the STP or WIT state, interrupt enable bits must be set to "1" before the STP or WIT instruction is executed.

■ Notes on clock generating circuit

For use with the oscillation stabilization set bit after release of the STP instruction set to "1", set values in timer 1 and prescaler 1 after fully appreciating the oscillation stabilization time of the oscillator to be used.
• Switch of ceramic/quartz-crystal and RC oscillations
After releasing reset the operation starts by starting a built-in ring oscillator. Then, a ceramic/qruartz-crystal oscillation or an RC oscillation is selected by setting bit 5 of the CPU mode register.
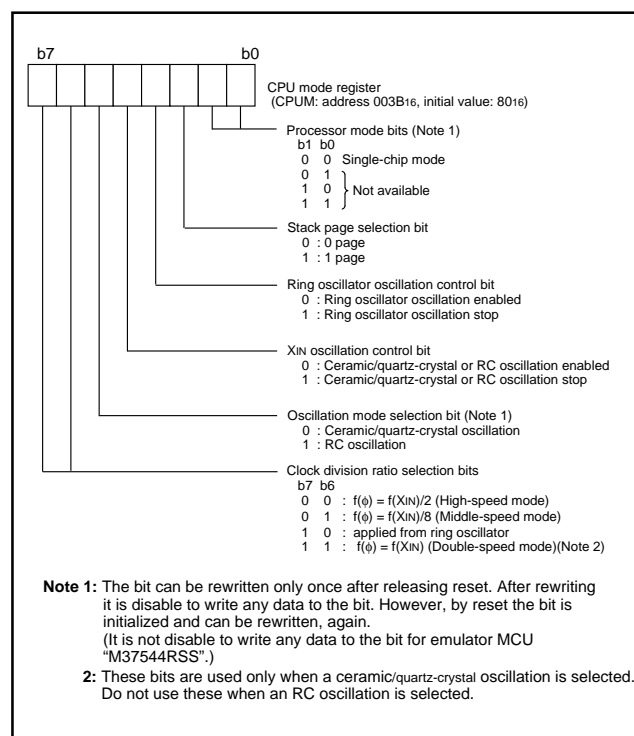
• Double-speed mode
When a ceramic/quartz-crystal oscillation is selected, a double-speed mode can be used. Do not use it when an RC oscillation is selected.

• CPU mode register
Bits 5, 1 and 0 of CPU mode register are used to select oscillation mode and to control operation modes of the microcomputer. In order to prevent the dead-lock by error-writing (ex. program run-away), these bits can be rewritten only once after releasing reset. After rewriting it is disable to write any data to the bit. (The emulator MCU "M37544RSS" is excluded.)
Also, when the read-modify-write instructions (SEB, CLB) are executed to bits 2 to 4, 6 and 7, bits 5, 1 and 0 are locked.

• Clock division ratio, X_{IN} oscillation control, ring oscillator control
The state transition shown in Fig. 46 can be performed by setting the clock division ratio selection bits (bits 7 and 6), X_{IN} oscillation control bit (bit 4), ring oscillator oscillation control bit (bit 3) of CPU mode register. Be careful of notes on use in Fig. 46.

Fig. 42 Structure of CPU mode register

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Notice: This is not a final specification.
Some parametric limits are subject to change.

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● Oscillation stop detection circuit (Note)

The oscillation stop detection circuit is used for reset occurrence when a ceramic resonator or an oscillation circuit stops by disconnection. When internal reset occurs, reset because of oscillation stop can be detected by setting "1" to the oscillation stop detection status bit.

Also, when using the oscillation stop detection circuit, a built-in ring oscillator is required.

Figure 46 shows the state transition.

Note: The oscillation stop detection circuit is not included in the emulator MCU "M37544RSS".

b7   b0

MISRG(address 0038₁₆, initial value: 00₁₆)

Oscillation stabilization time set bit after release of the STP instruction
0: Set "01₁₆" in timer1, and "FF₁₆" in prescaler 1 automatically
1: Not set automatically

Ceramic/quartz-crystal or RC oscillation stop detection function active bit
0: Detection function inactive
1: Detection function active

Reserved bits (return "0" when read)
(Do not write "1" to these bits)

Disable (return "0" when read)

Oscillation stop detection status bit
0: Oscillation stop not detected
1: Oscillation stop detected

Fig. 43 Structure of MISRG

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Notice: This is not a final specification.
Some parametric limits are subject to change.

Fig. 44 Block diagram of internal clock generating circuit (for ceramic/quartz-crystal resonator)

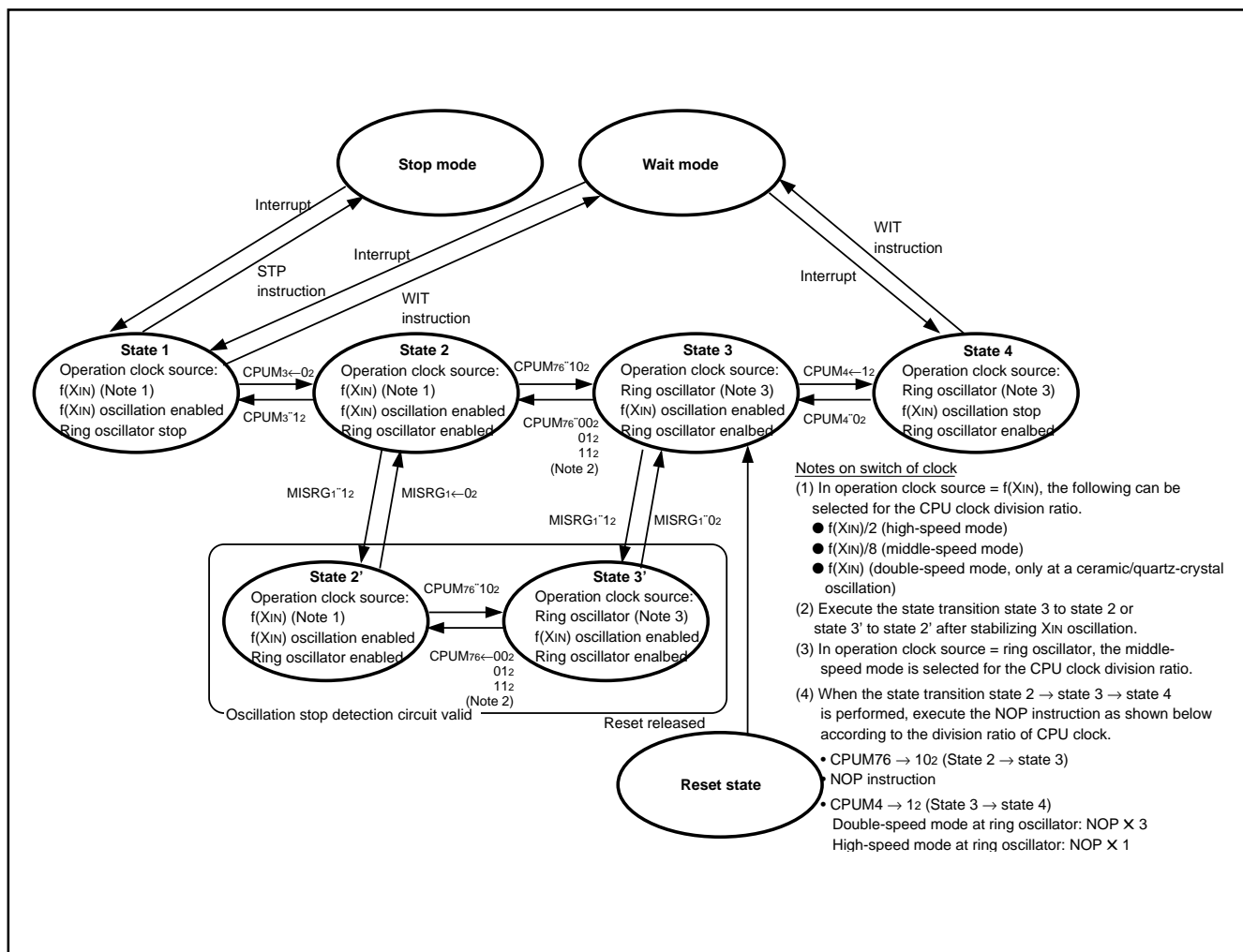**Fig. 45 Block diagram of internal clock generating circuit (for RC oscillation)**

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Notice: This is not a final specification.
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Stop mode

Wait mode

Interrupt

STP instruction

Interrupt

WIT instruction

WIT instruction

Interrupt

State 1
Operation clock source:
f(XIN) (Note 1)
f(XIN) oscillation enabled
Ring oscillator stop

$CPUM3 \leftarrow 0_2$
$CPUM3 \leftarrow 1_2$

State 2
Operation clock source:
f(XIN) (Note 1)
f(XIN) oscillation enabled
Ring oscillator enabled

$CPUM76 \leftarrow 10_2$

$CPUM76 \leftarrow 00_2$
01_2
11_2
(Note 2)

State 3
Operation clock source:
Ring oscillator (Note 3)
f(XIN) oscillation enabled
Ring oscillator enalbed

$CPUM4 \leftarrow 1_2$
$CPUM4 \leftarrow 0_2$

State 4
Operation clock source:
Ring oscillator (Note 3)
f(XIN) oscillation stop
Ring oscillator enalbed

$MISRG1 \leftarrow 1_2$
$MISRG1 \leftarrow 0_2$

$MISRG1 \leftarrow 1_2$
$MISRG1 \leftarrow 0_2$

State 2'
Operation clock source:
f(XIN) (Note 1)
f(XIN) oscillation enabled
Ring oscillator enabled

$CPUM76 \leftarrow 10_2$

State 3'
Operation clock source:
Ring oscillator (Note 3)
f(XIN) oscillation enabled
Ring oscillator enalbed

$CPUM76 \leftarrow 00_2$
01_2
11_2
(Note 2)

Oscillation stop detection circuit valid

Reset released

Reset state

Notes on switch of clock
(1) In operation clock source = f(XIN), the following can be selected for the CPU clock division ratio.
● f(XIN)/2 (high-speed mode)
● f(XIN)/8 (middle-speed mode)
● f(XIN) (double-speed mode, only at a ceramic/quartz-crystal oscillation)
(2) Execute the state transition state 3 to state 2 or state 3' to state 2' after stabilizing XIN oscillation.
(3) In operation clock source = ring oscillator, the middle-speed mode is selected for the CPU clock division ratio.
(4) When the state transition state 2 → state 3 → state 4 is performed, execute the NOP instruction as shown below according to the division ratio of CPU clock.

• $CPUM76 \rightarrow 10_2$ (State 2 → state 3)
• NOP instruction
• $CPUM4 \rightarrow 1_2$ (State 3 → state 4)
  Double-speed mode at ring oscillator: NOP × 3
  High-speed mode at ring oscillator: NOP × 1

Fig. 46 State transition

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7544 Group

NOTES ON PROGRAMMING

Processor Status Register

The contents of the processor status register (PS) after reset are undefined except for the interrupt disable flag I which is "1". After reset, initialize flags which affect program execution. In particular, it is essential to initialize the T flag and the D flag because of their effect on calculations.

Interrupts

The contents of the interrupt request bit do not change even if the BBC or BBS instruction is executed immediately after they are changed by program because this instruction is executed for the previous contents. For executing the instruction for the changed contents, execute one instruction before executing the BBC or BBS instruction.

Decimal Calculations

 • For calculations in decimal notation, set the decimal mode flag D to "1", then execute the ADC instruction or SBC instruction. In this case, execute SEC instruction, CLC instruction or CLD instruction after executing one instruction before the ADC instruction or SBC instruction.
 • In the decimal mode, the values of the N (negative), V (overflow) and Z (zero) flags are invalid.

Ports

 • The values of the port direction registers cannot be read.
That is, it is impossible to use the LDA instruction, memory operation instruction when the T flag is "1", addressing mode using direction register values as qualifiers, and bit test instructions such as BBC and BBS.
It is also impossible to use bit operation instructions such as CLB and SEB and read/modify/write instructions of direction registers for calculations such as ROR.
For setting direction registers, use the LDM instruction, STA instruction, etc.

A-D Conversion

Do not execute the STP instruction during A-D conversion.

Instruction Execution Timing

The instruction execution time can be obtained by multiplying the frequency of the internal clock φ by the number of cycles mentioned in the machine-language instruction table.
The frequency of the internal clock φ is the same as that of the XIN in double-speed mode, twice the XIN cycle in high-speed mode and 8 times the XIN cycle in middle-speed mode.

CPU Mode Register

The oscillation mode selection bit and processor mode bits can be rewritten only once after releasing reset. However, after rewriting it is disable to write any value to the bit. (Emulator MCU is excluded.)
When a ceramic / quartz-crystal oscillation is selected, a double-speed mode of the clock division ratio selection bits can be used. Do not use it when an RC oscillation is selected.

State transition

Do not stop the clock selected as the operation clock because of setting of CM3, 4.

NOTES ON HARDWARE

Handling of Power Source Pin

In order to avoid a latch-up occurrence, connect a capacitor suitable for high frequencies as bypass capacitor between power source pin (Vcc pin) and GND pin (Vss pin). Besides, connect the capacitor to as close as possible. For bypass capacitor which should not be located too far from the pins to be connected, a ceramic capacitor of 0.01 µF to 0.1 µF is recommended.

One Time PROM Version

The CNVss pin is connected to the internal memory circuit block by a low-ohmic resistance, since it has the multiplexed function to be a programmable power source pin (VPP pin) as well.
To improve the noise reduction, connect a track between CNVss pin and Vss pin with 1 to 10 kΩ resistance.
The mask ROM version track of CNVss pin has no operational interference even if it is connected via a resistor.

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Notice: This is not a final specification.
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NOTES ON PERIPHERAL FUNCTIONS

■ Interrupt

When setting the followings, the interrupt request bit may be set to "1".

•When setting external interrupt active edge
Related register: Interrupt edge selection register (address $003A_{16}$)
Timer X mode register (address $2B_{16}$)
Timer A mode register (address $1D_{16}$)

When not requiring the interrupt occurrence synchronized with these setting, take the following sequence.
① Set the corresponding interrupt enable bit to "0" (disabled).
② Set the interrupt edge select bit (active edge switch bit) to "1".
③ Set the corresponding interrupt request bit to "0" after 1 or more instructions have been executed.
④ Set the corresponding interrupt enable bit to "1" (enabled).

■ Timers

• When n (0 to 255) is written to a timer latch, the frequency division ratio is 1/(n+1).
• When a count source of timer X is switched, stop a count of timer X.

■ Timer A

CNTR1 interrupt active edge selection
CNTR1 interrupt active edge depends on the CNTR1 active edge switch bit.
When this bit is "0", the CNTR1 interrupt request bit is set to "1" at the falling edge of the CNTR1 pin input signal. When this bit is "1", the CNTR1 interrupt request bit is set to "1" at the rising edge of the CNTR1 pin input signal.
However, in the pulse width HL continuously measurement mode, CNTR1 interrupt request is generated at both rising and falling edges of CNTR1 pin input signal regardless of the setting of CNTR1 active edge switch bit.

■ Timer X

CNTR0 interrupt active edge selection
CNTR0 interrupt active edge depends on the CNTR0 active edge switch bit.
When this bit is "0", the CNTR0 interrupt request bit is set to "1" at the falling edge of CNTR0 pin input signal. When this bit is "1", the CNTR0 interrupt request bit is set to "1" at the rising edge of CNTR0 pin input signal.

■ Serial I/O

• Serial I/O interrupt
When setting the transmit enable bit to "1", the serial I/O transmit interrupt request bit is automatically set to "1". When not requiring the interrupt occurrence synchronized with the transmission enabled, take the following sequence.
① Set the serial I/O transmit interrupt enable bit to "0" (disabled).
② Set the transmit enable bit to "1".
③ Set the serial I/O transmit interrupt request bit to "0" after 1 or more instructions have been executed.
④ Set the serial I/O transmit interrupt enable bit to "1" (enabled).

• I/O pin function when serial I/O is enabled.
The functions of P12 and P13 are switched with the setting values of a serial I/O mode selection bit and a serial I/O synchronous clock selection bit as follows.

(1) Serial I/O mode selection bit → "1" :
Clock synchronous type serial I/O is selected.
Setup of a serial I/O synchronous clock selection bit
"0" : P12 pin turns into an output pin of a synchronous clock.
"1" : P12 pin turns into an input pin of a synchronous clock.
Setup of a SRDY output enable bit (SRDY)
"0" : P13 pin can be used as a normal I/O pin.
"1" : P13 pin turns into a SRDY output pin.

(2) Serial I/O mode selection bit → "0" :
Clock asynchronous (UART) type serial I/O is selected.
Setup of a serial I/O synchronous clock selection bit
"0": P12 pin can be used as a normal I/O pin.
"1": P12 pin turns into an input pin of an external clock.
When clock asynchronous (UART) type serial I/O is selected, it is P13 pin. It can be used as a normal I/O pin.

■ A-D Converter

The comparator uses internal capacitors whose charge will be lost if the clock frequency is too low.
Make sure that f(XIN) is 500kHz or more during A-D conversion.

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Notice: This is not a final specification.
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PROM Mode

M37544G2SP/GP (referred to as "the MCU") has a PROM Mode as well as the normal operation mode. PROM Mode enables an external device (referred to as "Programmer") to read and program the built-in EPROM via a minimum number of serial I/O pins by sending commands to control the MCU.

To enable PROM Mode, use the pin connection shown in Figure 47 to 48 and apply power (V_{CC}). Then execute the new OTP entry operation, called "Mad Dog Entry".

There are three operation modes in PROM Mode : Read, Program and Program-Verify. Three commands are defined to enable each mode respectively.

The format of the serial I/O is : clock synchronous and LSB-data-first.
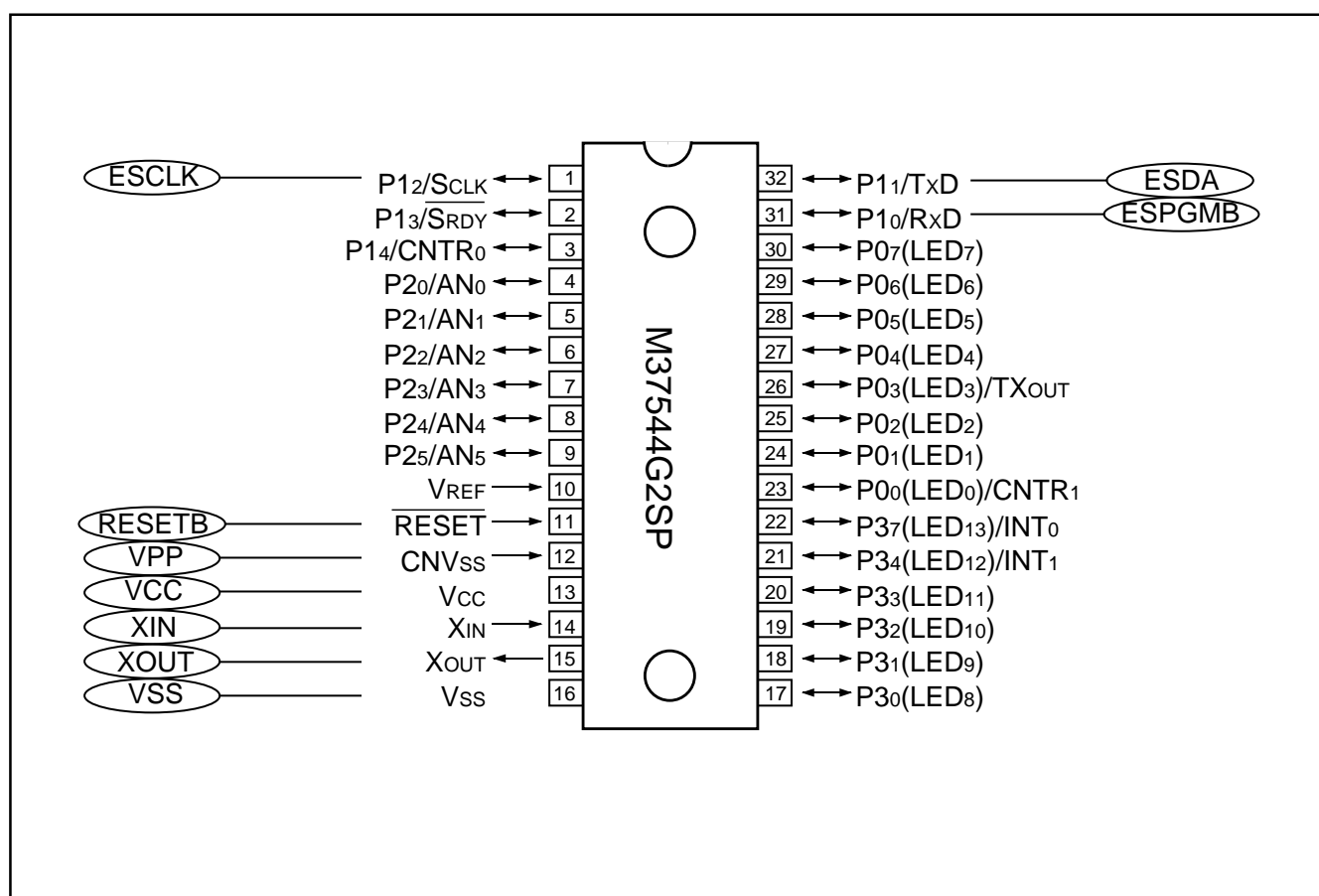
Fig. 47 "Mad Dog Entry" Pin Diagram (32P4B)

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Notice: This is not a final specification.
Some parametric limits are subject to change.

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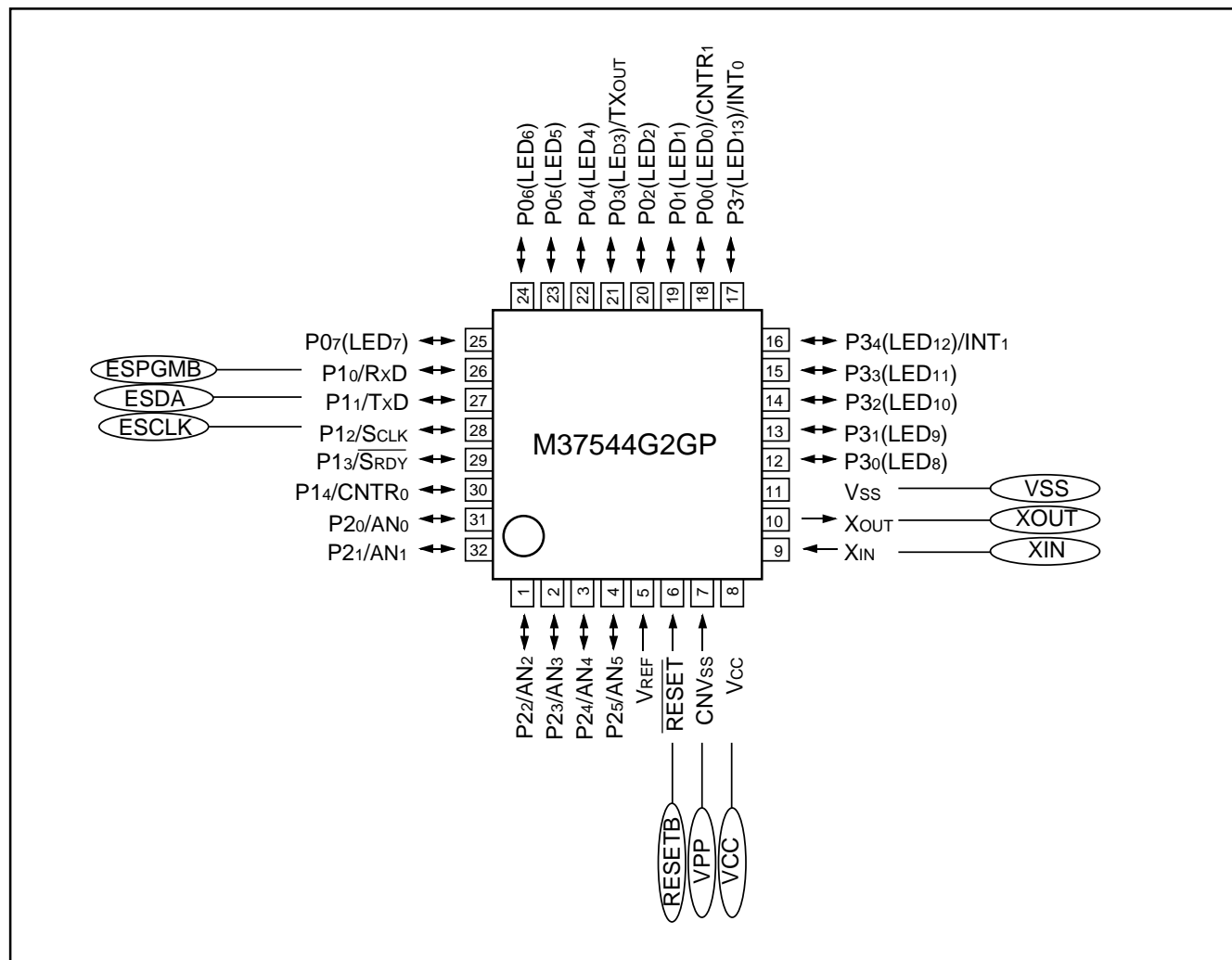
Fig. 48 "Mad Dog Entry" Pin Diagram (32P6U-A)

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Notice: This is not a final specification.
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Precaution for Handling One-Time-Programmable Devices

Our company ships one-time-programmable version MCUs (One-Time PROM MCU) without being screened by the PROM writing test.
To ensure the reliability of the MCU, We recommend that the user performs the program and test procedure shown in Figure 49 before using the MCU.
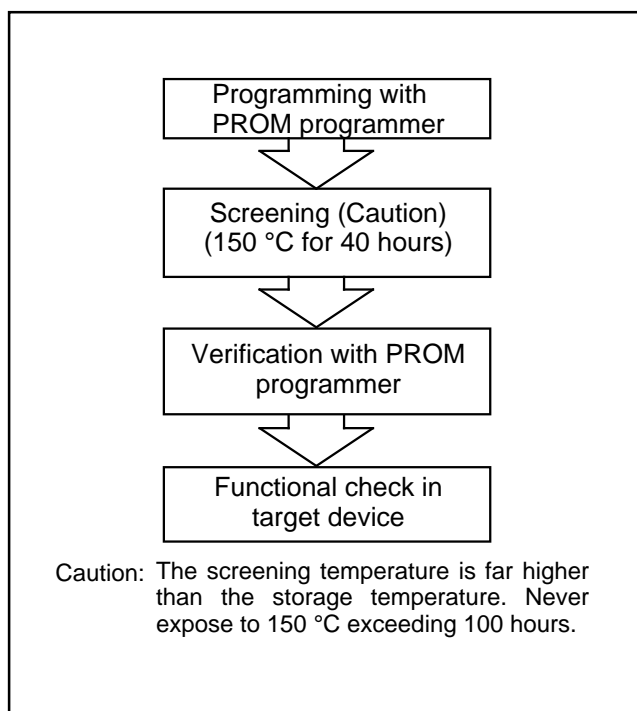
Fig. 49 Programming and testing of One Time PROM

ROM Code Access Protection

We would like to support a simple ROM code protection function that prevents a party other than the ROM-code owner to read and reprogram the builit-in PROM code of the MCU.

The MCU has 7 bytes of dedicated ROM spaces in address 0xFFD4 to 0xFFDA, as an ID-code (referred to as "the ID-code") enabling a Programmer to verify with the input ID-code and validate further operations.

Expected Programmer ID-Code Verification Function

First, Programmer must check the ID-code of the MCU.

If the ID-code is still in blank, Programmer enebles all operations, Read, Program, and Program-Verify.

When Programmer programs the MCU, Programmer also programs the given ID-code as well as the actual firmware.

If the ID-code is not blank, Programmer verifies it with the input ID-code.

When the ID-codes don't mutch, Programmer will reject all further operations.

If they match, Programmer perform operations according to the given command.
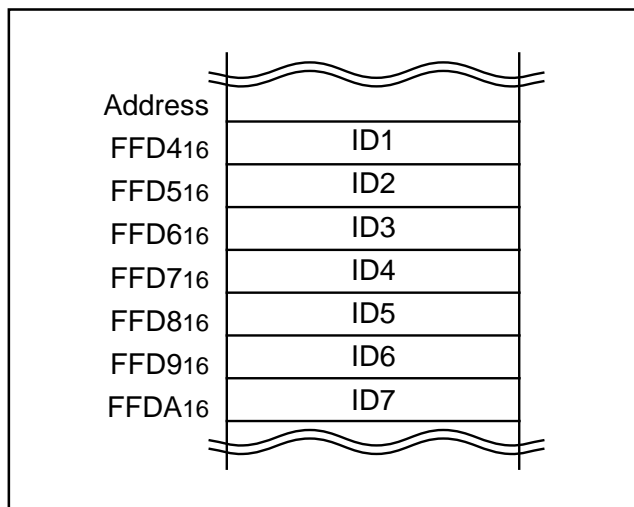
Fig. 50 ROM-Code Protection ID Location

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Notice: This is not a final specification.
Some parametric limits are subject to change.

ELECTRICAL CHARACTERISTICS

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Applied to: M37544M2-XXXSP/GP, M37544G2SP/GP

Absolute Maximum Ratings

Table 9 Absolute maximum ratings

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Power source voltage		−0.3 to 6.5	V
V_I	Input voltage $P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_5$, $P3_0$–$P3_4$,$P3_7$, V_{REF}	All voltages are based on V_{SS}. Output transistors are cut off.	−0.3 to V_{CC} + 0.3	V
V_I	Input voltage $\overline{RESET}$, X_{IN}		−0.3 to V_{CC} + 0.3	V
V_I	Input voltage CNV$_{SS}$ (**Note**)		−0.3 to 7.0	V
V_O	Output voltage $P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_5$, $P3_0$–$P3_4$,$P3_7$, X_{OUT}		−0.3 to V_{CC} + 0.3	V
P_d	Power dissipation	T_a = 25°C	200	mW
T_{opr}	Operating temperature		−20 to 85	°C
T_{stg}	Storage temperature		−40 to 125	°C

Notes : It is a rating only for the One Time PROM version. Connect to V_{SS} for the mask ROM version.

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Notice: This is not a final specification.
Some parametric limits are subject to change.

Recommended Operating Conditions

Table 10 Recommended operating conditions (1) (Vcc = 4.0 to 5.5 V, Ta = −20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
V_{CC}	Power source voltage (ceramic)	f(X_{IN}) = 8 MHz (High-, Middle-speed mode)	4.0	5.0	5.5	V
		f(X_{IN}) = 8 MHz (Double-speed mode)	4.5	5.0	5.5	V
	Power source voltage (RC)	f(X_{IN}) = 4 MHz (High-, Middle-speed mode)	4.0	5.0	5.5	V
V_{SS}	Power source voltage			0		V
V_{REF}	Analog reference voltage		2.0		V_{CC}	V
V_{IH}	"H" input voltage $P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_5$, $P3_0$–$P3_4$, $P3_7$		0.8V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage (TTL input level selected) $P1_0$, $P1_2$, $P3_4$, $P3_7$		2.0		V_{CC}	V
V_{IH}	"H" input voltage $\overline{RESET}$, X_{IN}		0.8V_{CC}		V_{CC}	V
V_{IL}	"L" input voltage $P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_5$, $P3_0$–$P3_4$, $P3_7$		0		0.3V_{CC}	V
V_{IL}	"L" input voltage (TTL input level selected) $P1_0$, $P1_2$, $P3_4$, $P3_7$		0		0.8	V
V_{IL}	"L" input voltage $\overline{RESET}$, CNV_{SS}		0		0.2V_{CC}	V
V_{IL}	"L" input voltage X_{IN}		0		0.16V_{CC}	V
$\sum I_{OH(peak)}$	"H" total peak output current (**Note**) $P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_5$, $P3_0$–$P3_4$, $P3_7$				−80	mA
$\sum I_{OL(peak)}$	"L" total peak output current (**Note**) $P1_0$–$P1_4$, $P2_0$–$P2_5$				80	mA
$\sum I_{OL(peak)}$	"L" total peak output current (**Note**) $P0_0$–$P0_7$, $P3_0$–$P3_4$, $P3_7$				60	mA
$\sum I_{OH(avg)}$	"H" total average output current (**Note**) $P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_5$, $P3_0$–$P3_4$, $P3_7$				−40	mA
$\sum I_{OL(avg)}$	"L" total average output current (**Note**) $P1_0$–$P1_4$, $P2_0$–$P2_5$				40	mA
$\sum I_{OL(avg)}$	"L" total average output current (**Note**) $P0_0$–$P0_7$, $P3_0$–$P3_4$, $P3_7$				30	mA

Note : The total output current is the sum of all the currents flowing through all the applicable ports. The total average current is an average value measured over 100 ms. The total peak current is the peak value of all the currents.

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Notice: This is not a final specification.
Some parametric limits are subject to change.

Recommended Operating Conditions (continued)

Table 11 Recommended operating conditions (2) (V_{CC} = 4.0 to 5.5 V, Ta = −20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
$I_{OH(peak)}$	"H" peak output current (**Note 1**) P00–P07, P10–P14, P20–P25, P30–P34, P37				−10	mA
$I_{OL(peak)}$	"L" peak output current (**Note 1**) P10–P14, P20–P25				10	mA
$I_{OL(peak)}$	"L" peak output current (**Note 1**) P00–P07, P30–P34, P37				30	mA
$I_{OH(avg)}$	"H" average output current (**Note 2**) P00–P07, P10–P14, P20–P25, P30–P34, P37				−5	mA
$I_{OL(avg)}$	"L" average output current (**Note 2**) P10–P14, P20–P25				5	mA
$I_{OL(avg)}$	"L" average output current (**Note 2**) P00–P07, P30–P34, P37				15	mA
$f(X_{IN})$	Internal clock oscillation frequency (**Note 3**) at ceramic oscillation or external clock input	V_{CC} = 4.5 to 5.5 V Double-speed mode			8	MHz
	Internal clock oscillation frequency (**Note 3**) at ceramic oscillation or external clock input	V_{CC} = 4.0 to 5.5 V High-, Middle-speed mode			8	MHz
	Internal clock oscillation frequency (**Note 3**) at RC oscillation	V_{CC} = 4.0 to 5.5 V High-, Middle-speed mode			4	MHz

Notes 1: The peak output current is the peak current flowing in each port.
    2: The average output current I_{OL} (avg), I_{OH} (avg) in an average value measured over 100 ms.
    3: When the oscillation frequency has a duty cycle of 50 %.

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Notice: This is not a final specification.
Some parametric limits are subject to change.

Electrical Characteristics

Table 12 Electrical characteristics (1) (Vcc = 4.0 to 5.5 V, Vss = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{OH}	"H" output voltage P00–P07, P10–P14, P20–P25, P30–P34, P37 (**Note 1**)	I_{OH} = –5 mA V_{CC} = 4.0 to 5.5 V	V_{CC}–1.5			V
		I_{OH} = –1.0 mA V_{CC} = 2.2 to 5.5 V	V_{CC}–1.0			V
V_{OL}	"L" output voltage P10–P14, P20–P25	I_{OL} = 5 mA V_{CC} = 4.0 to 5.5 V			1.5	V
		I_{OL} = 1.5 mA V_{CC} = 4.0 to 5.5 V			0.3	V
		I_{OL} = 1.0 mA V_{CC} = 2.2 to 5.5 V			1.0	V
V_{OL}	"L" output voltage P00–P07, P30–P34, P37	I_{OL} = 15 mA V_{CC} = 4.0 to 5.5 V			2.0	V
		I_{OL} = 1.5 mA V_{CC} = 4.0 to 5.5 V			0.3	V
		I_{OL} = 10 mA V_{CC} = 2.2 to 5.5 V			1.0	V
V_{T+}–V_{T-}	Hysteresis CNTR0, CNTR1, INT0, INT1 (**Note 2**) P00–P07 (**Note 3**)			0.4		V
V_{T+}–V_{T-}	Hysteresis RxD, SCLK (**Note 2**)			0.5		V
V_{T+}–V_{T-}	Hysteresis $\overline{RESET}$			0.5		V
I_{IH}	"H" input current P00–P07, P10–P14, P20–P25, P30–P34, P37	V_I = V_{CC} (Pin floating. Pull up transistors "off")			5.0	μA
I_{IH}	"H" input current $\overline{RESET}$	V_I = V_{CC}			5.0	μA
I_{IH}	"H" input current X_{IN}	V_I = V_{CC}		4.0		μA
I_{IL}	"L" input current P00–P07, P10–P14, P20–P25, P30–P34, P37	V_I = V_{SS} (Pin floating. Pull up transistors "off")			–5.0	μA
I_{IL}	"L" input current $\overline{RESET}$, CNVss	V_I = V_{SS}			–5.0	μA
I_{IL}	"L" input current X_{IN}	V_I = V_{SS}		–4.0		μA
I_{IL}	"L" input current P00–P07, P30–P34, P37	V_I = V_{SS} (Pull up transistors "on")		–0.2	–0.5	mA
V_{RAM}	RAM hold voltage	When clock stopped	2.0		5.5	V
R_{OSC}	Ring oscillator oscillation frequency	V_{CC} = 5.0 V, Ta = 25 °C	1000	2000	3000	kHz
D_{OSC}	Oscillation stop detection circuit detection frequency	V_{CC} = 5.0 V, Ta = 25 °C	62.5	125	187.5	kHz

Notes 1: P11 is measured when the P11/TxD P-channel output disable bit of the UART control register (bit 4 of address 001B16) is "0".
    2: RxD, SCLK, INT0, and INT1 have hystereses only when bits 0 to 2 of the port P1P3 control register are set to "0" (CMOS level).
    3: It is available only when operating key-on wake up.

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Notice: This is not a final specification.
Some parametric limits are subject to change.

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Electrical Characteristics (continued)

Table 13 Electrical characteristics (2) (V$_{CC}$ = 4.0 to 5.5 V, V$_{SS}$ = 0 V, Ta = −20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min.	Typ.	Max.	
I$_{CC}$	Power source current	High-speed mode, f(X$_{IN}$) = 8 MHz Output transistors "off"			3.3	8.0	mA
		Double-speed mode, f(X$_{IN}$) = 8 MHz Output transistors "off"			4.8	10.0	mA
		Middle-speed mode, f(X$_{IN}$) = 8 MHz Output transistors "off"			1.8	5.0	mA
		Ring oscillator operation mode, V$_{CC}$ = 5 V Output transistors "off"			250	900	µA
		f(X$_{IN}$) = 8 MHz (in WIT state), functions except timer 1 disabled, Output transistors "off"			1.3	3.2	mA
		Ring oscillator operation mode(in WIT state), V$_{CC}$ = 5V functions except timer 1 disabled, Output transistors "off"			140	450	µA
		Increment when A-D conversion is executed f(X$_{IN}$) = 8 MHz, V$_{CC}$ = 5 V			0.45		mA
		All oscillation stopped (in STP state) Output transistors "off"	Ta = 25 °C		0.1	1.0	µA
			Ta = 85 °C			10.0	µA

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Notice: This is not a final specification.
Some parametric limits are subject to change.

A-D Converter Characteristics

Table 14 A-D Converter characteristics (Vcc = 4.0 to 5.5 V, Vss = 0 V, Ta = −20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution				8	Bits
ABS	Absolute accuracy (quantification error excluded)				±3	LSB
t_{CONV}	Conversion time				109	$t_c(X_{IN})$
R_{LADDER}	Ladder resistor			37		kΩ
I_{VREF}	Reference power source input current	V_{REF} = 5.0 V	50	135	200	μA
		V_{REF} = 3.0 V	30	80	120	
$I_{I(AD)}$	A-D port input current				5.0	μA

Timing Requirements

Table 15 Timing requirements (Vcc = 4.0 to 5.5 V, Vss = 0 V, Ta = −20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_W(\overline{RESET})$	Reset input "L" pulse width	2			μs
$t_C(X_{IN})$	External clock input cycle time	125			ns
$t_{WH}(X_{IN})$	External clock input "H" pulse width	50			ns
$t_{WL}(X_{IN})$	External clock input "L" pulse width	50			ns
$t_C(CNTR_0)$	CNTR0 input cycle time	200			ns
$t_{WH}(CNTR_0)$	CNTR0, INT0, INT1, input "H" pulse width	80			ns
$t_{WL}(CNTR_0)$	CNTR0, INT0, INT1, input "L" pulse width	80			ns
$t_C(CNTR_1)$	CNTR1 input cycle time	2000			ns
$t_{WH}(CNTR_1)$	CNTR1 input "H" pulse width	800			ns
$t_{WL}(CNTR_1)$	CNTR1 input "L" pulse width	800			ns
$t_C(S_{CLK})$	Serial I/O clock input cycle time (Note)	800			ns
$t_{WH}(S_{CLK})$	Serial I/O clock input "H" pulse width (Note)	370			ns
$t_{WL}(S_{CLK})$	Serial I/O clock input "L" pulse width (Note)	370			ns
$t_{su}(RxD–S_{CLK})$	Serial I/O input set up time	220			ns
$t_h(S_{CLK}–RxD)$	Serial I/O input hold time	100			ns

Note: In this time, bit 6 of the serial I/O control register (address 001A16) is set to "1" (clock synchronous serial I/O is selected).
When bit 6 of the serial I/O control register is "0" (clock asynchronous serial I/O is selected), the rating values are divided by 4.

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Notice: This is not a final specification.
Some parametric limits are subject to change.

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Switching Characteristics

Table 16 Switching characteristics (Vcc = 4.0 to 5.5 V, Vss = 0 V, Ta = −20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t_{WH}(SCLK)	Serial I/O clock output "H" pulse width	t_C(SCLK)/2–30			ns
t_{WL}(SCLK)	Serial I/O clock output "L" pulse width	t_C(SCLK)/2–30			ns
t_d(SCLK–TxD)	Serial I/O output delay time			140	ns
t_v(SCLK–TxD)	Serial I/O output valid time	−30			ns
t_r(SCLK)	Serial I/O clock output rising time			30	ns
t_f(SCLK)	Serial I/O clock output falling time			30	ns
t_r(CMOS)	CMOS output rising time (**Note**)		10	30	ns
t_f(CMOS)	CMOS output falling time (**Note**)		10	30	ns

Note : Pin XOUT is excluded.
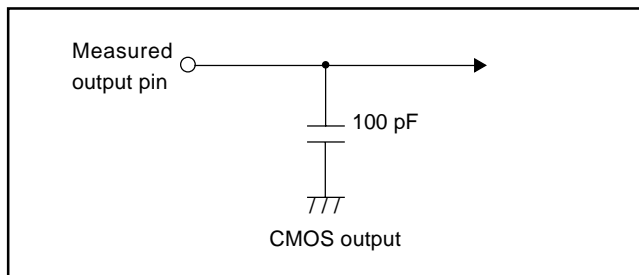
Fig. 51 Switching characteristics measurement circuit diagram

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Notice: This is not a final specification.
Some parametric limits are subject to change.
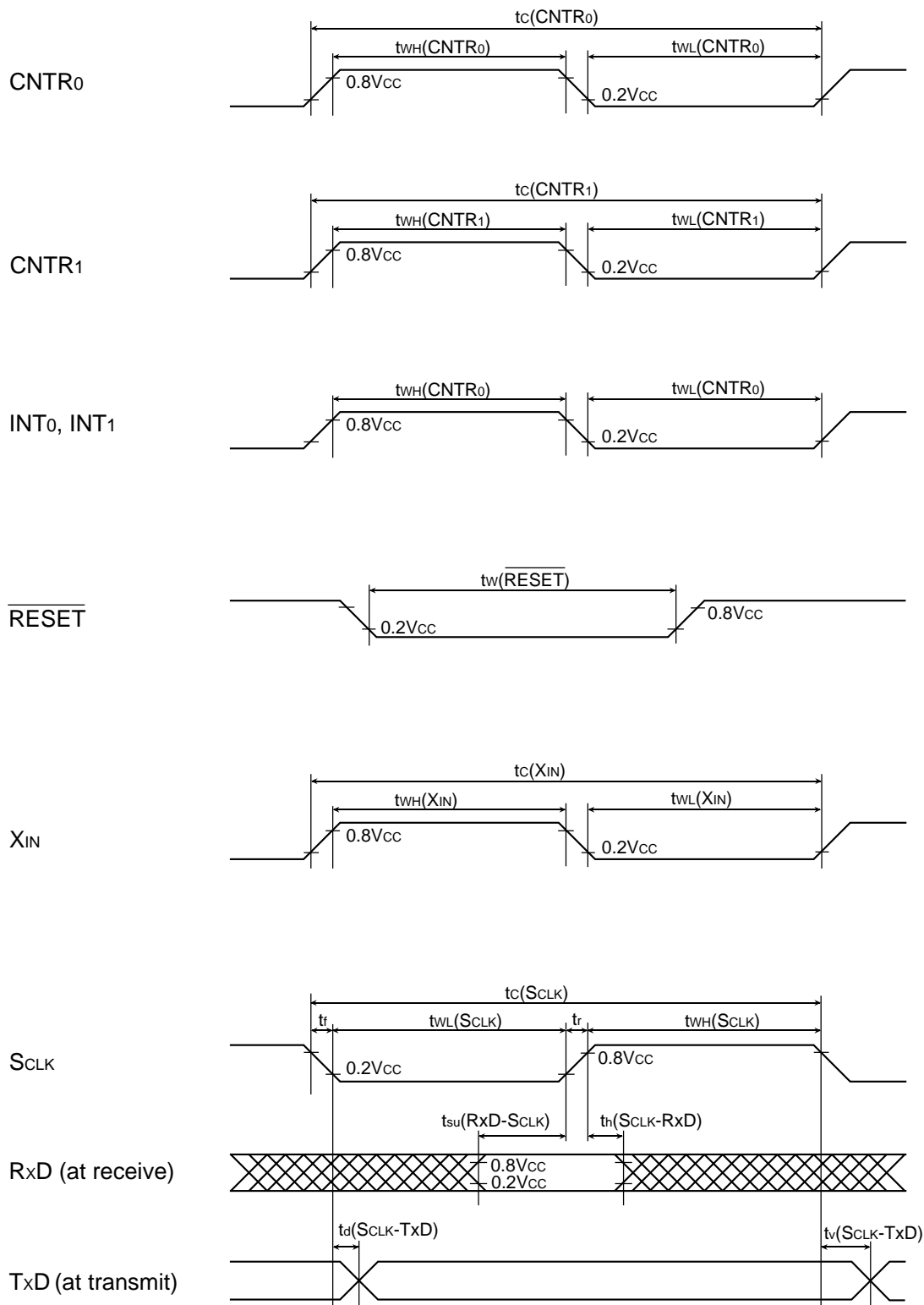
Fig. 52 Timing chart

PACKAGE OUTLINE

32P4B (Recomended) **Plastic 32pin 400mil SDIP**

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
SDIP32-P-400-1.78	–	2.2	Alloy 42/Cu Alloy

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	5.08
A1	0.51	–	–
A2	–	3.8	–
b	0.35	0.45	0.55
b1	0.9	1.0	1.3
b2	0.63	0.73	1.03
c	0.22	0.27	0.34
D	27.8	28.0	28.2
E	8.75	8.9	9.05
e	–	1.778	–
e1	–	10.16	–
L	3.0	–	–
θ	0°	–	15°

SEATING PLANE

32P6U-A (Recomended) **Plastic 32pin 7×7mm body LQFP**

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
LQFP32-P-0707-0.80	–		Cu Alloy

Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	1.7
A1	0	0.1	0.2
A2	–	1.4	–
b	0.32	0.37	0.45
c	0.105	0.125	0.175
D	6.9	7.0	7.1
E	6.9	7.0	7.1
e	–	0.8	–
HD	8.8	9.0	9.2
HE	8.8	9.0	9.2
L	0.3	0.5	0.7
L1	–	1.0	–
Lp	0.45	0.6	0.75
A3	–	0.25	–
x	–	–	0.2
y	–	–	0.1
θ	0°	–	10°
b2	–	0.5	–
l2	1.0	–	–
MD	–	7.4	–
ME	–	7.4	–

Detail F

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REVISION HISTORY			7544 Group Data Sheet

Rev.	Date	Description	
		Page	Summary
1.00	Nov. 8, 2002	–	First edition issued
1.01	May. 6, 2003	44-48	Added to Electrical Characteristics

1.02	June. 25, 2003	48	Enterd to Limits
			  ICC Power source current Ring oscillator operation mode,
			                              Ring oscillator operation mode(in WIT state)

		49	Enterd to Limits A-D Converter characteristics