



# DLD-100B PULSED LASER DIODE DRIVER

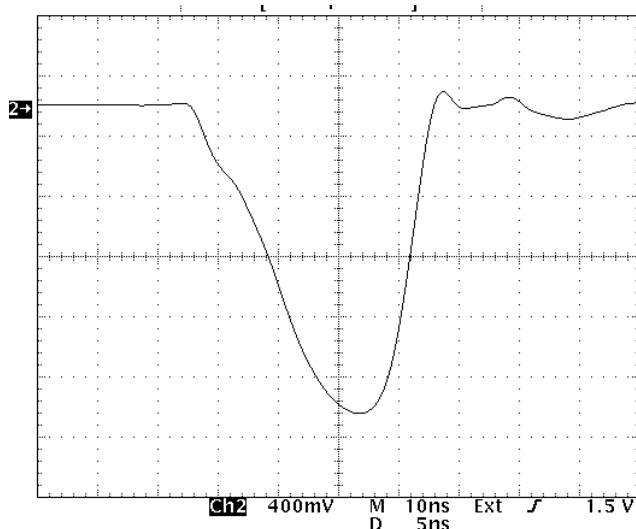
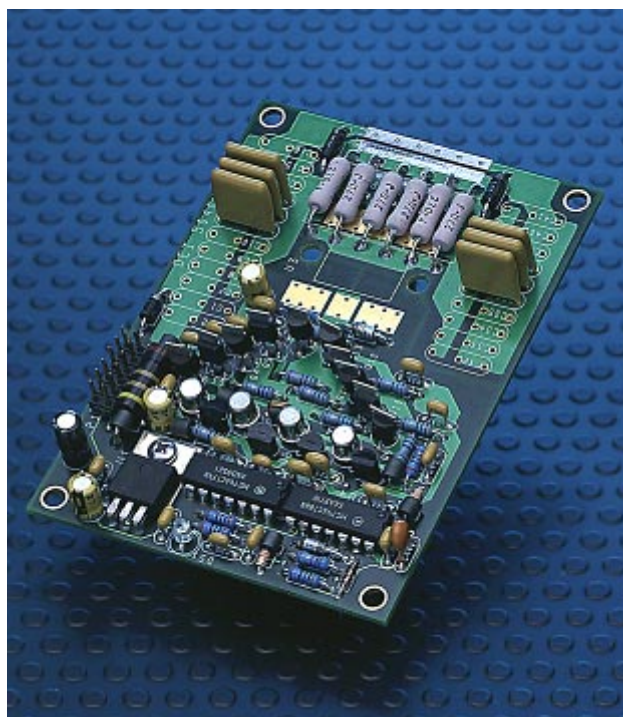
- Output Current <5A To 40A
- Repetition Frequency To 1 MHz
- Variable Pulse Width From 12ns to 1 $\mu$ s
- Economical OEM Module

The DLD-100B is a high speed, high current pulsed laser diode driver designed to operate at 5A to 40A output current with continuously variable pulse widths from 12ns to 1 $\mu$ s (Option A), and frequencies up to 1MHz.

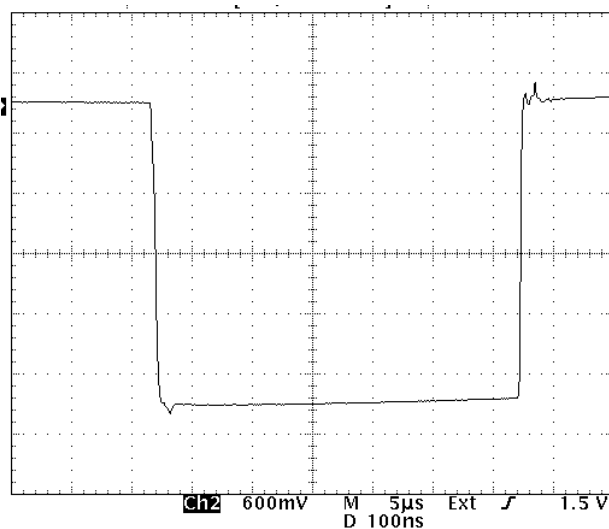
The DLD-100B is available in two models. Option A is optimized for fast rise and fall times and a narrower minimum pulse width than Option B. Option B is optimized for maximum duty cycle and efficiency, with a slower rise time and longer minimum pulse width than Option A. (See specific performance data on the following pages.)

The output pulse is launched on low inductance pads. The laser diode can be mounted directly on the driver, or connected via a low inductance stripline interconnect.

The driver is supplied mounted on a 1/4" aluminum heat spreader to provide the cooling needed for the switching transistor, and to simplify mounting or installation of the driver.



DLD-100B Option A  
20A Output, 12ns Pulse Width



DLD-100B Option A  
30A Output, 600ns Pulse Width



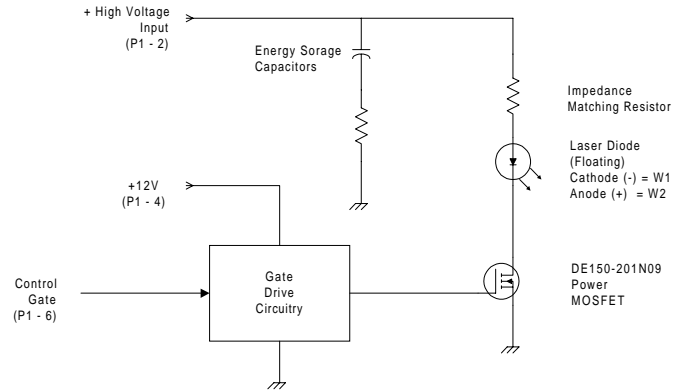
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## Technical Description

The DLD-100B is an open-frame, OEM module designed for integration into the user's equipment.

The driver requires +12 to +15VDC support power, a high voltage DC input (150VDC maximum for Option A, 60VDC maximum for Option B), and a +5V gate signal. The amplitude of the high voltage DC supply controls the amplitude of the output current pulse. The output pulse width and frequency follow the input gate's width and frequency.

To minimize cost, the driver is designed so that the laser diode is floating on the voltage of the drain of the output transistor. **The diode must be electrically isolated from earth (chassis) ground.** The cathode (-) connects to W1, and the anode (+) connects to W2.



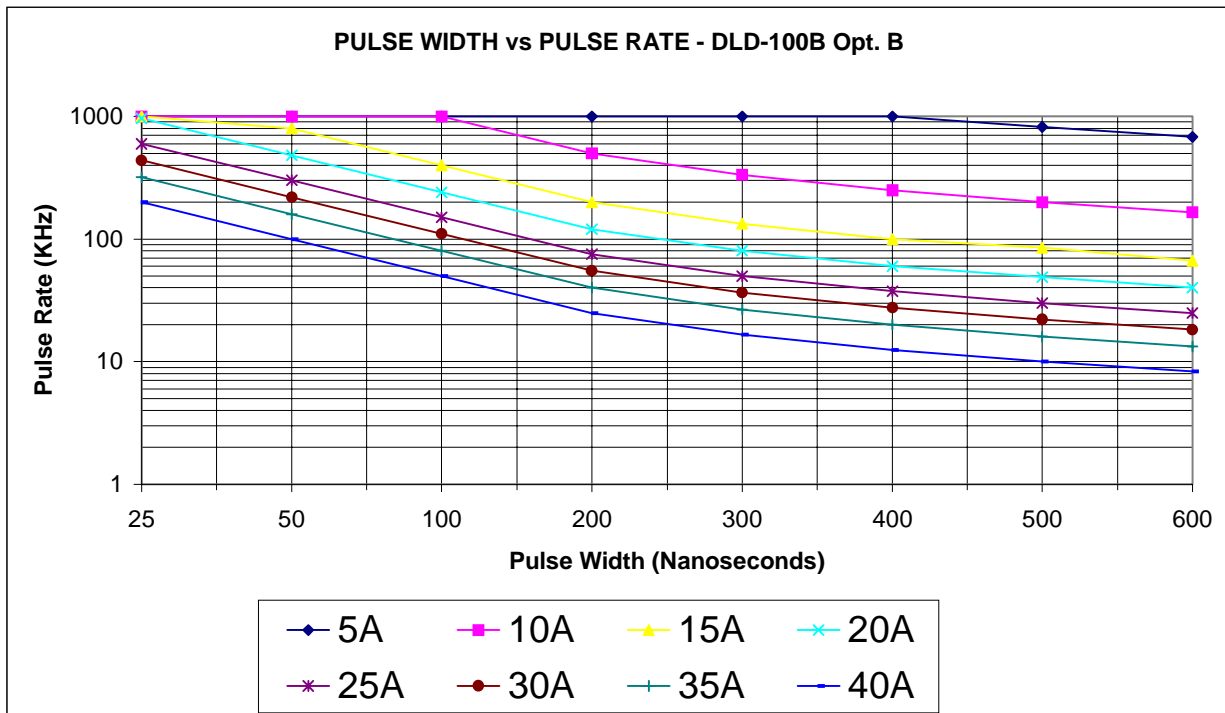
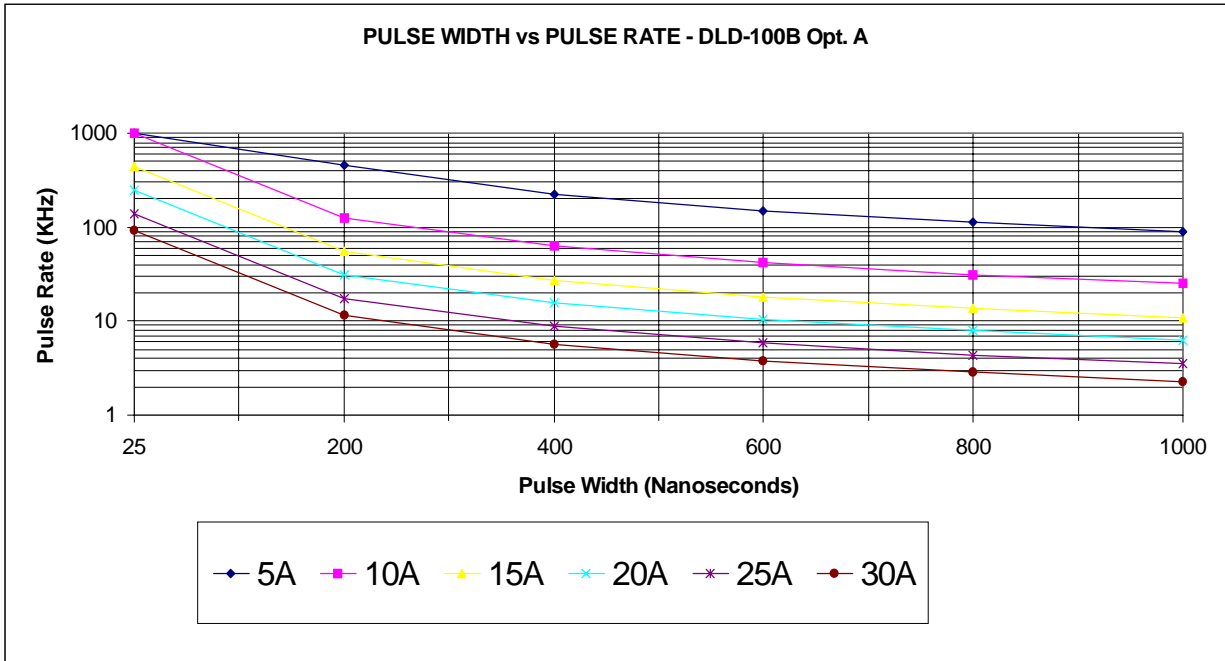
DLD-100B Simplified Block Diagram

SPECIFICATIONS		
PARAMETER	DLD-100B Option A	DLD-100B Option B
Peak Output Current	30A, controlled by input high voltage amplitude	40A, controlled by input high voltage amplitude
Minimum Pulse Width (Typical)	12ns (12E-9S)	15ns (15E-9S)
Maximum Pulse Width at 5% Droop	1 $\mu$ s (1E-6S)	600ns (6E-7S)
Pulse Rise Time (10% to 90%) (Typical)	11ns (11E-9S)	18ns (18E-9S)
PRF (Pulse Recurrence Frequency), CW	Single Shot to 1MHz, limited by maximum average current, controlled by input trigger frequency (see tables below)	
Gate (Trigger) In	+5V/50 $\Omega$ Output pulse width and frequency follow gate's width and frequency	
Support Power	+12VDC to +15VDC at 60mA typical	
DC HV Input	150V Maximum	60V Maximum
Throughput (Propagation) Delay	<40ns, typically 35ns	
MECHANICAL		
Size	70mm (2.75") W x 100mm (3.9") L	
ALL SPECIFICATIONS MEASURED INTO A SHORTED OUTPUT. SPECIFICATIONS SUBJECT TO CHANGE WITHOUT NOTICE.		

Output Current (A)	Maximum Duty Cycle		Typical Input Voltage (VDC)	
	Option A	Option B	Option A	Option B
5	0.09	0.40	25	6
10	0.025	0.1	50	12
15	0.01	0.04	75	20
20	0.006	0.024	100	25
25	0.0035	0.015	125	32
30	0.002	0.01	150	40
35	—	0.008	—	47
40	—	0.005	—	60

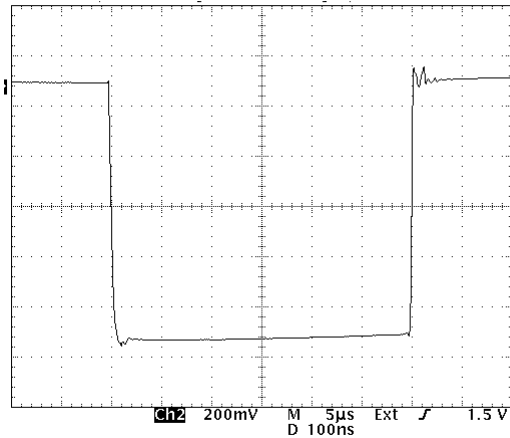
## Maximum Frequency Versus Pulse Width

The graphs below show the maximum pulse repetition frequency (PRF) versus pulse width at various output current levels. These graphs can be used to determine the maximum safe operating area for a given output current.

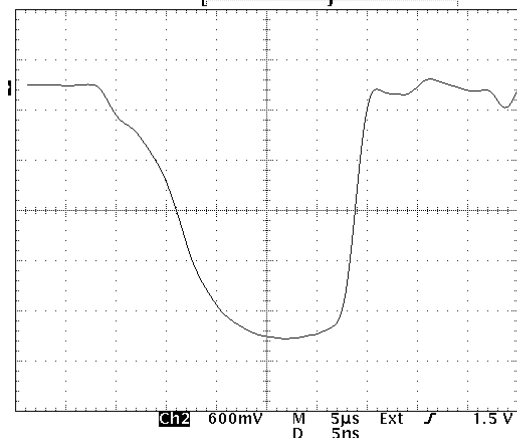


## Typical Performance Waveforms

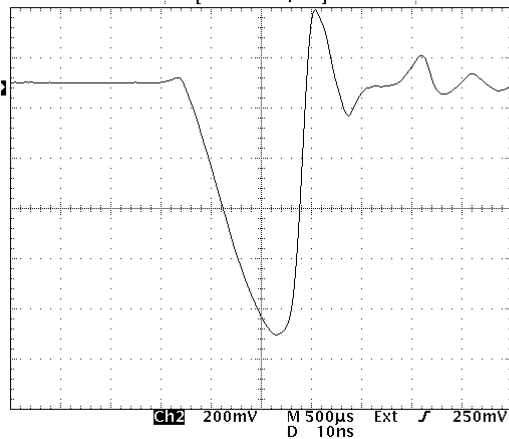
The oscilloscope photos below show typical output waveforms of the DLD-100B. All waveforms are driving a shorted output.



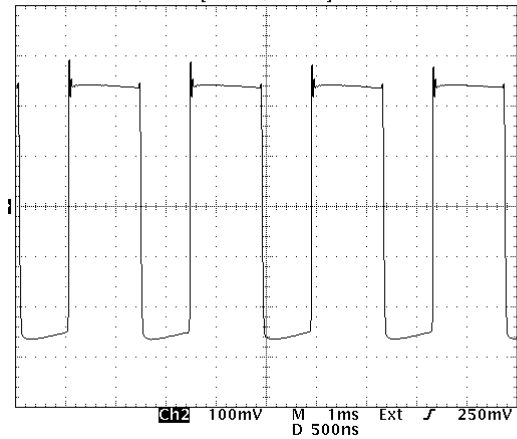
*DLD-100B Option A*  
10A Output, 600ns Pulse Width



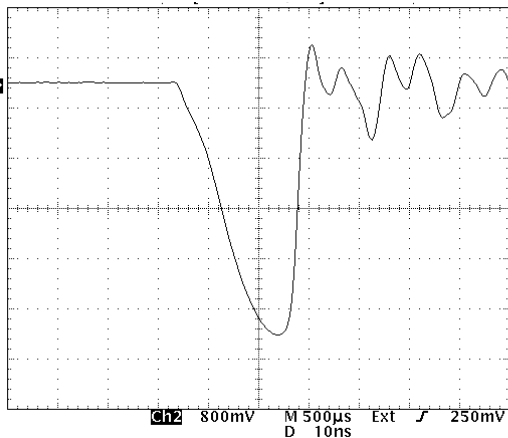
*DLD-100B Option A*  
30A Output, 18ns Pulse Width



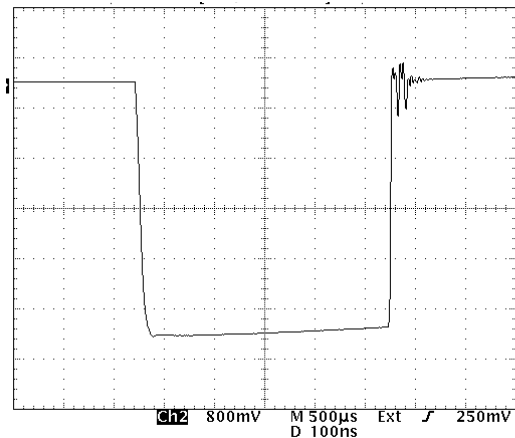
*DLD-100B Option B*  
10A Output, 15ns Pulse Width



*DLD-100B Option B*  
5A Output, 40% Duty Cycle At 826KHz



*DLD-100B Option B*  
40A Output, 15ns Pulse Width



*DLD-100B Option B*  
40A Output, 500ns Pulse Width



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DLD-100B 0299