Multimedia 16-bit Stereo Audio Codec

Features

- 16-bit ΣΔ stereo audio codec
- Serial interface with DSPs as well as Yamaha OPL3-L, OPL4 FM Synthesizers, and YSS225 effect processor
- Support Microsoft Windows Sound System®
- Versatile MPC Level 2 compatible mixers
- On-chip ADPCM, μ-Law, and A-Law compression / decompression
- Programmable analog and digital mixer gain-scaling
- Programmable timer for audio / video synchronization
- Sampling rates from 5.5 kHz to 48 kHz
- On-chip 32-sample FIFOs with programmable request control
- 16 mA bus driver
- Backward compatible to Crystal CS4231 / 4248 and Analog Devices AD1848
- CMOS technology in 68-pin PLCC and 100-pin TQFP
- Digital 5V and 3.3V operation

Description

Chrontel CH6357 is a complete audio subsystem IC that incorporates audio data conversions and control functions to provide CD-quality audio in personal computers. The CH6357 offers 16-bit stereo ADCs and DACs with on-chip digital filters, analog and digital mixers with programmable gain and attenuation, a selectable serial interface, and full duplex channels for simultaneous record and playback capabilities.

CH6357's additional decimator and interpolator allows the codec's ADCs and DACs to run at 44.1 kHz while maintaining support of external AT bus data rates at 22.05 kHz, 11.025 kHz, and 5.51 kHz. This key feature enables the codec to receive from, and output audio data to, the AT bus at these rates while still being able to interface, for example, directly with the Yamaha OPL4/OPL3-L music synthesizers or effect processor without requiring an external serial DAC.

CH6357 meets the Microsoft Windows Sound System® requirements and provides interface to both ISA and EISA buses. In addition, CH6357 has built-in capture and playback FIFOs with programmable CDRQ and PDRQ controls that allow efficient utilization of the CPU bus while reducing the possibility of losing audio data.

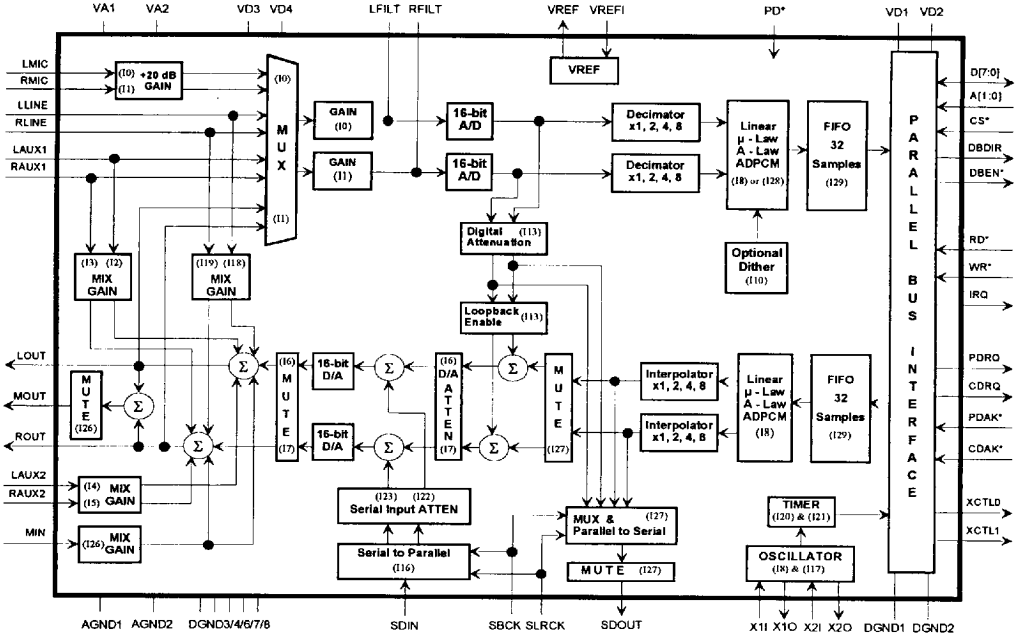

Figure 1: Detailed Functional Block Diagram

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Pinout Diagrams

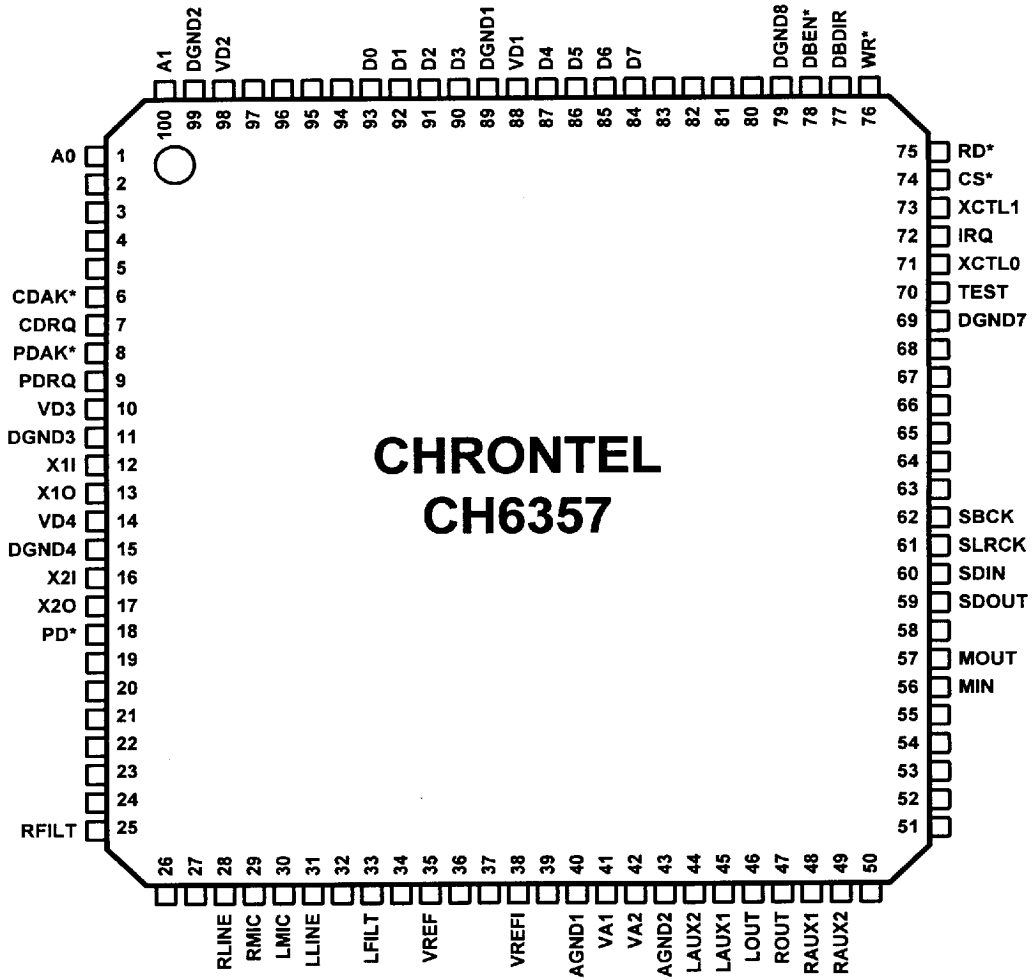

Figure 2: 100-pin TQFP

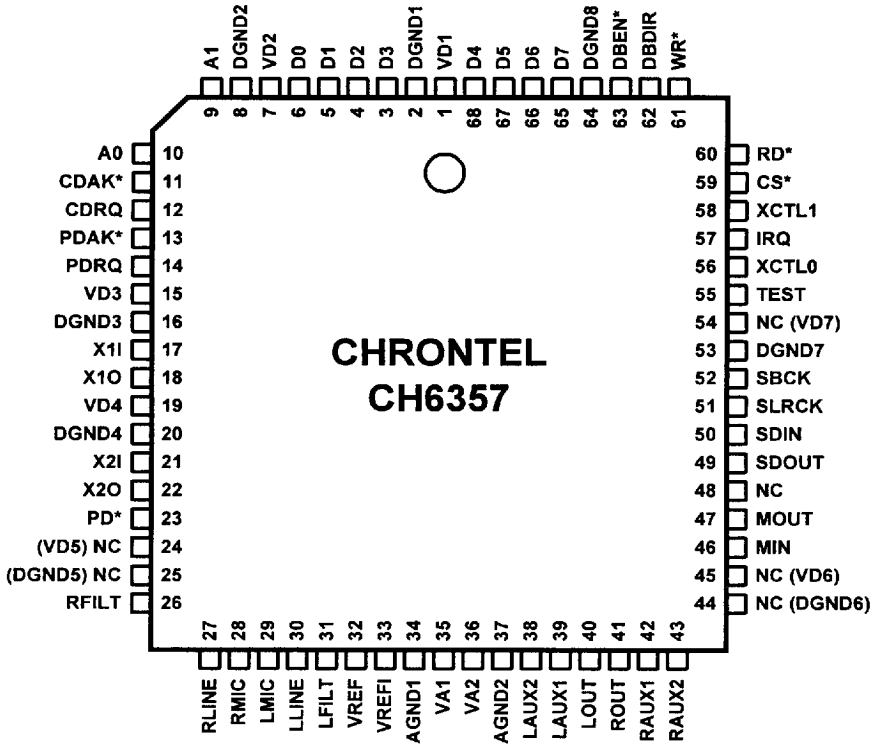

Figure 3: 68-pin PLCC

Table 1 • Summary of Pin Description

Symbol	Pin #		Type	Description	Symbol	Pin #		Type	Description
	PLCC	TQFP				PLCC	TQFP		
VD1	1	88	P	Digital Supply Voltage #1	VA1	35	41	P	Analog Supply Voltage #1
DGND1	2	89	P	Digital Ground #1	VA2	36	42	P	Analog Supply Voltage #2
D3	3	90	I / O	Bi-directional Data Bus Line	AGND2	37	43	P	Analog Ground #2
D2	4	91	I / O	Bi-directional Data Bus Line	LAUX2	38	44	I	Left Channel Auxiliary #2 Input
D1	5	92	I / O	Bi-directional Data Bus Line	LAUX1	39	45	I	Left Channel Auxiliary #1 Input
D0	6	93	I / O	Bi-directional Data Bus Line	LOUT	40	46	O	Left Channel Audio Output
VD2	7	98	P	Digital Supply Voltage #2	ROUT	41	47	O	Right Channel Audio Output
DGND2	8	99	P	Digital Ground #2	RAUX1	42	48	I	Right Channel Auxiliary #1 Input
A1	9	100	I	Address Bus Line	RAUX2	43	49	I	Right Channel Auxiliary #2 Input
A0	10	1	I	Address Bus Line	NC (DGND6)	44		–	No Connect (Digital Ground #6)
CDAK*	11	6	I	Capture Data Acknowledge (active low)	NC (VD6)	45		–	No Connect (Digital Supply Voltage #6)
CDRQ	12	7	O	Capture Data Request	MIN	46	56	I	Mono Input
PDAK*	13	8	I	Playback Data Acknowledge (active low)	MOUT	47	57	O	Mono Output
PDRQ	14	9	O	Playback Data Request	NC	48		–	No Connect
VD3	15	10	P	Digital Supply Voltage #3	SDOUT	49	59	O	Digital Serial Data Output
DGND3	16	11	P	Digital Ground #3	SDIN	50	60	I	Digital Serial Data Input
X1I	17	12	I	Crystal #1 Input	SLRCK	51	61	I	Serial Left / Right Channel Clock
X1O	18	13	O	Crystal #1 Output	SBCK	52	62	I	Serial Bit Clock
VD4	19	14	P	Digital Supply Voltage #4	DGND7	53	69	P	Digital Ground #7
DGND4	20	15	P	Digital Ground #4	NC (VD7)	54		–	Digital Supply Voltage #7
X2I	21	16	I	Crystal #2 Input	TEST	55	70	–	Test Pin (for Internal use only)
X2O	22	17	O	Crystal #2 Output	XCTL0	56	71	O	External Control Pin #0
PD*	23	18	I	Power Down (active low)	IRQ	57	72	O	Interrupt Request
NC (VD5)	24		–	No Connect (Digital Supply Voltage #5)	XCTL1	58	73	O	External Control Pin #1
NC (DGND5)	25		–	No Connect (Digital Ground #5)	CS*	59	74	I	CH6357 Chip Select (active low)
RFILT	26	25	I	Right Channel Filter	RD*	60	75	I	Read Signal (active low)
RLINE	27	28	I	Right Channel Line Input	WR*	61	76	I	Write Signal (active low)
RMIC	28	29	I	Right Channel Microphone Input	DBDIR	62	77	O	Data Bus Direction Control Signal
LMIC	29	30	I	Left Channel Microphone Input	DBEN*	63	78	O	Data Bus Enable (active low)
LLINE	30	31	I	Left Channel Line Input	DGND8	64	79	P	Digital Ground #8
LFILT	31	33	I	Left Channel Filter Input	D7	65	84	I / O	Bi-directional Data Bus Line
VREF	32	35	O	Voltage Reference	D6	66	85	I / O	Bi-directional Data Bus Line
VREFI	33	38	I	Voltage Reference Internal	D5	67	86	I / O	Bi-directional Data Bus Line
AGND1	34	40	P	Analog Ground #1	D4	68	87	I / O	Bi-directional Data Bus Line

Detailed Pin Description †

Table 2 • Parallel Bus Interface Signals

Symbol	Pin #	Type	Description
A[1:0]	9, 10	Input	**Address Bus** The two external address pins required for accessing all the direct and indirect registers of the CH6357.
CS*	59	Input	**CH6357 Chip Select (active low)** The input select pin asserted whenever a data transfer phase of a bus cycle needs to access the CH6357. This signal is ignored during DMA transfer.
RD*	60	Input	**Read Signal (active low)** Whenever asserted, this pin will indicate a read bus cycle to CH6357. The read cycle may be a programmed I/O read cycle or a DMA read cycle.
WR*	61	Input	**Write Signal (active low)** Whenever asserted, this pin will indicate a write bus cycle to CH6357. The write cycle may be a programmed I/O write cycle or a DMA write cycle.
CDAK*	11	Input	**Capture Data Acknowledge (active low)** The assertion of this signal indicates a DMA read cycle occuring from the capture FIFO.
PDAK*	13	Input	**Playback Data Acknowledge (active low)** The assertion of this signal indicates a DMA write cycle occuring to the playback FIFO.
D[7:0]	65 – 68, 3 – 6	Input / Output	**Bi-directional Data Bus** These data bus pins are used to transfer data to and from CH6357.
DBEN*	63	Output	**Data Bus Enable (active low, internal pull-up)** This pin enables the external bus drivers. This signal is normally high.
DBDIR	62	Output	**Data Bus Direction Control Signal (internal pull-up)** This pin controls the direction of the data bus transceiver. Logic high enables write access from the host to the CH6357, whereas logic low enables read access from CH6357 to the host bus. This signal is normally high.
CDRQ	12	Output	**Capture Data Request** The assertion of this signal indicates CH6357 has a captured sample from the ADCs ready for transfer. This signal will remain asserted until all bytes from the capture sample buffer are transferred.
PDRQ	14	Output	**Playback Data Request** The assertion of this signal indicates CH6357 is ready for more DAC playback data. The signal will remain asserted until all bytes needed from the playback sample buffer are transferred.
IRQ	57	Output	**Host Interrupt Signal** This signal is used to notify the host of events which need servicing.

Note: † Pinout descriptions are based on the PLCC pinout diagram

Table 3 • Analog Signals

Symbol	Pin #	Type	Description
LLINE	30	Input	**Left Line** A line-level input to the left LINE channel. This pin can accept a maximum (nominal) analog input value of 1 Vrms, centered around VREF.
RLINE	27	Input	**Right Line** A line-level input to the right LINE channel. This pin can accept a maximum (nominal) analog input value of 1 Vrms, centered around VREF.
LMIC	29	Input	**Left Microphone** Microphone input for the left channel. A +20 dB gain stage is available which can be enabled for a 0.1 Vrms input signal or disabled for a 1 Vrms input signal. This control is available through index register (I0).
RMIC	28	Input	**Right Microphone** Microphone input for the right channel. A +20 dB gain stage is available which can be enabled for a 0.1 Vrms input signal or disabled for a 1 Vrms input signal. This control is available through index register (I1).
LAUX1	39	Input	**Left Auxiliary #1** A line-level input to the Left AUX1 channel. This pin can accept a maximum (nominal) analog input value of 1 Vrms, centered around VREF.
RAUX1	42	Input	**Right Auxiliary #1** A line-level input to the Right AUX1 channel. This pin can accept a maximum (nominal) analog input value of 1 Vrms, centered around VREF.
LAUX2	38	Input	**Left Auxiliary #2** A line-level input to the left AUX2 channel. The input to this pin can be a maximum (nominal) analog input value of 1 Vrms, centered around VREF.
RAUX2	43	Input	**Right Auxiliary #2** A line-level input to the right AUX2 channel. The input to this pin can be a maximum (nominal) analog input value of 1 Vrms, centered around VREF.
MIN	46	Input	**Mono Input** A general purpose mono input. The input to this pin can be a maximum (nominal) analog input value of 1 Vrms, centered around VREF.
LOUT	40	Output	**Stereo Left Output** Line-level output from the left channel analog mixer. The Alternate Feature Enable I Register (I16) allows control of the output level of LOUT via the analog output level register bit (OLB).
ROUT	41	Output	**Stereo Right Output** Line-level output from the right channel analog mixer. The Alternate Feature Enable I Register (I16) allows control of the output level of ROUT via the analog output level register bit (OLB).
MOUT	47	Output	**Mono Output** Represents the summed output from the left and right channels of the analog mixer. The output from this pin can be muted, independent of the stereo line outputs, via the MOM register bit of the Mono Input and Output Control Register (I26).

Table 4 • Digital Serial Interface Signals

Symbol	Pin #	Type	Description
SDOUT	49	Output	**Serial Data Out** This pin outputs audio data to audio signal processors. The output data from SDOUT can be a multiplexed output from either: a captured digital audio data from the ADCs or a playback digital audio data from the parallel bus. This pin must be left unconnected when it is not used.
SDIN	50	Input	**Serial Data In (internal pull-up)** This serial interface input accepts digital audio data from an external source, such as DSPs, music synthesizers, or an effect processor. When this pin is not in use, it must be left unconnected or tied to VDD.
SLRCK	51	Input	**Left / Right Clock for Serial Digital Data (internal pull-up)** This pin accepts the left / right clock signal for SDIN and SDOUT. This clock is used to synchronize the transfer of the left and right channel audio data to and from the CH6357. When this pin is not in use, it must be left unconnected or tied to VDD.
SBCK	52	Input	**Bit Clock for Serial Digital Data (internal pull-up)** This pin accepts the bit clock signal for SDIN and SDOUT. This bit clock is used to synchronize serial audio data movement in and out of the CH6357. When this pin is not in use, it must be left unconnected or tied to VDD.

Table 5 • Power Supplies

ANALOG SUPPLY		
Symbol	**Pin #**	**Description**
VA1 VA2	35, 36	**Analog Supply Voltage** These pins supply the 5V power to the analog section of CH6357.
AGND1 AGND2	34, 37	**Analog Ground** These pins provide the ground reference to the analog section of CH6357. These pins MUST be connected to the system ground.
DIGITAL SUPPLY		
Symbol	**Pin #**	**Description**
VD1 VD2	1, 7	**Digital Supply Voltage** These pins must be connected to a 5V or 3.3V supply. These pins supply power to the parallel interface data bus section of CH6357.
VD3 VD4	15, 19	**Digital Supply Voltage** These pins must be connected to a 5V or 3.3V supply. Except for the parallel interface data bus, these pins supply power to the internal digital section of CH6357.
DGND1 DGND2	2, 8	**Digital Ground** These pins provide the ground reference for the parallel data bus section of CH6357. These pins SHOULD be isolated from the other digital grounds (DGND3/4/6/7/8) and MUST be connected to the digital section of the board.
DGND3 DGND4 DGND7 DGND8	16, 20, 53, 64	**Digital Ground** Except for the parallel interface data bus, these pins provide the ground reference for the internal digital section of CH6357. These pins MUST be connected to the system ground.

Table 6 • Miscellaneous Signals

Symbol	Pin #	Type	Description
X1I	17	Input	**Crystal #1 Input** This pin accepts a standard 24.576 MHz crystal. A crystal or an external CMOS compatible clock source MUST always be connected to this pin for proper operation.
X1O	18	Output	**Crystal #1 Output** A 24.576 MHz crystal should be connected between X1O and X1I. This pin will normally be left open when an external CMOS compatible clock input to the X1I pin is used.
X2I	21	Input	**Crystal #2 Input** This pin accepts a standard 16.9344 MHz crystal. A crystal or an external CMOS compatible clock source MUST always be connected to this pin for proper operation.
X2O	22	Output	**Crystal #2 Output** A 16.9344 MHz crystal should be connected between X2O and X2I. This pin will normally be left open when an external CMOS compatible clock input to the X1I pin is used.
PD*	23	Input	**Power Down (active low)** Asserting this signal places CH6357 into a miminum power consumption state.
VREF	32	Output	**Voltage Reference** All analog inputs and outputs are centered around VREF (2.25V, nominally).
VREFI	33	Input	**Voltage Reference Internal** This pin supplies the internal voltage reference of the CH6357.
LFILT, RFILT	31 26	Input	**Left & Right Anti-alias Filter** A 1000 pF NPO capacitor should be connected across each of these pins and analog ground. Combined with the internal resistor at each pin, these capacitors provide CH6357 with single-pole low-pass filters at the inputs to the ADCs, thereby eliminating the need for external low-pass filter components.
XCTL0 XCTL1	56 58	Output	**External Control** These pins can be used to control external logic via TTL levels. These signals are controlled by the XCTL0 and XCTL1 register bits in Index Register I10.
TEST	55	–	**Test** This pin must be tied to ground for proper operation.
NC	48	–	**No Connect** This pin must be left unconnected.
NC (VD5, VD6, VD7)	24 45 54	–	**No Connect** These pins are no connects for CH6357. These pins should be connected to the digital supply when compatibility with AD1848 is desired.
NC (DGND5, DGND6)	25 44	–	**No Connect** These pins are no connects for CH6357. These pins should be connected to digital ground when compatibility with AD1848 is desired.

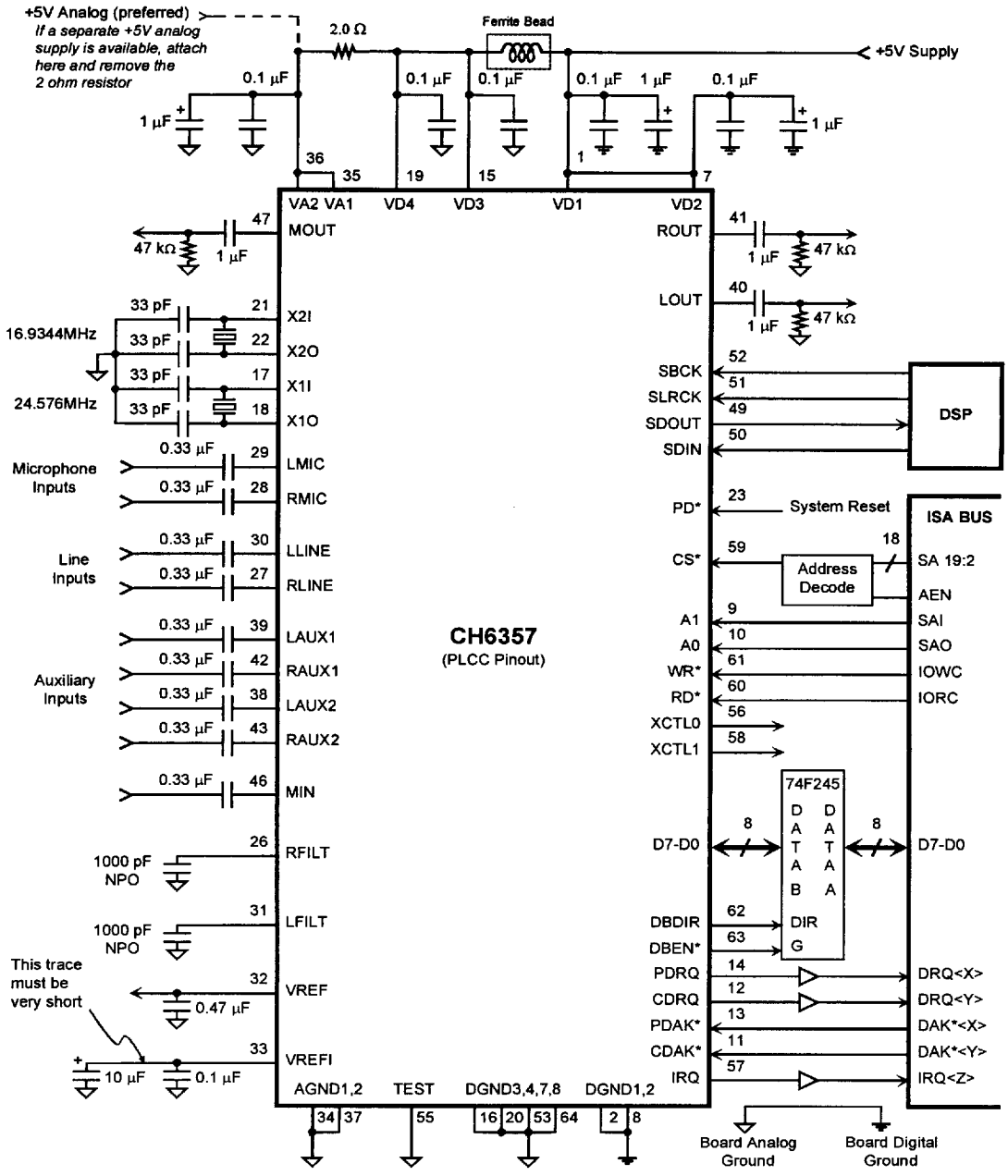

Figure 4: Recommended Connection Diagram

Analog Hardware Description

The following paragraphs describe the input, output, and miscellaneous analog signals that make up CH6357's analog hardware. In particular, this section focuses on the analog hardware needed to interface with the input and output of CH6357. **Figure 4** on page 2-11 is used as a reference to illustrate how components are interfaced to CH6357. Wherever applicable, a reference is made to other sections with details about the function being performed.

Analog Inputs

The analog inputs include four stereo line-level inputs and a mono input. As shown in **Figure 1**, these inputs consist of three analog stereo line-level inputs (LINE, AUX1, MIC) multiplexed to the ADC, and a stereo line-level input AUX2 and a mono input MIN fed to the output analog mixer, whose output is multiplexed to the ADC as well. Additional inputs to the output analog mixer include output from the DACs and inputs from separate and volume-controllable paths of the LINE and AUX1 inputs. For information on LINE and AUX1 programmable mix gain, please refer to index registers I18, I19, I2, and I3.

Line-Level Inputs

Three line-level inputs of CH6357 (LINE, AUX1, AUX2) are rated to accept a nominal maximum analog input of 1 Vrms, centered around VREF. Since some analog inputs can be as large as 2 Vrms, the circuit shown in **Figure 5** below can be used to attenuate the analog input to the maximum allowable input voltage (1 Vrms) for these line-level inputs.

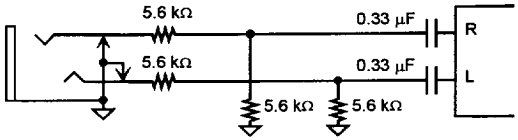

Figure 5: Line Inputs

Microphone-Level Inputs

The microphone inputs come with a selectable +20 dB gain stage prior to multiplexing them to the ADC. Depending on the level of the microphone input signal, the +20 dB gain stage can be enabled or disabled. For a 1 Vrms mic input signal, the gain stage should be disabled and bypassed. On the other hand, for a 0.1 Vrms mic input signal, the gain stage should be enabled. Disabling the gain stage also allows the left and right microphone inputs to be used as additional line-level inputs. (Please refer to the LMGE bit in index register I0 and the RMGE bit in index registers I1 on page 2-36 for details on the selectable gain stage).

For lower gain microphones, the circuit shown in **Figure 6** below can be used as a single-ended microphone input buffer.

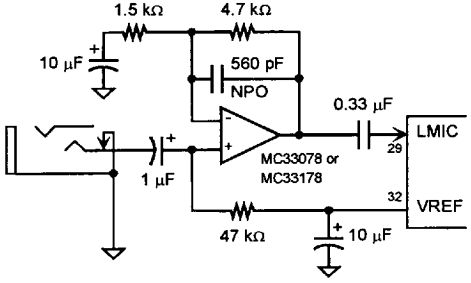

Figure 6: Left or Mono Microphone Input

Mono Input

This input allows the "beeper" signal included in most computer systems to be integrated into the audio system. It comes with an attenuation control, allowing 16 levels in 3 dB steps, and a selectable mute control. Please refer to the **Mono Input and Output Control (I26)** on page 2-56 for details. The mute control bit upon power-up, by default, is disabled (as with the mono output) so the initial "beeps" when the computer is initializing is allowed to pass through. The single-channel attenuator block also allows the resulting signal to be mixed with the left and right channel outputs.

This pin is rated to accept a nominal maximum analog input of 1 Vrms. **Figure 7** below shows a typical input circuit for the mono input

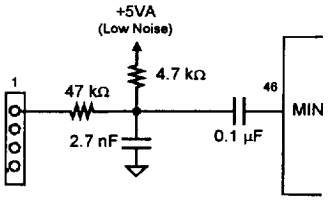

Figure 7: Mono Input

Analog Output

The analog output section of CH6357 consists of a stereo line-level output and a mono output.

Line-Level Output

The output from LOUT and ROUT represents the output from the mixer for the left and right channels, respectively. It comes with output level control (see the **Alternate Feature Enable I (I16)** on page 2-49 regarding output level control), but requires external circuitry to drive other output types such as headphones or speakers. The outputs should be capacitively coupled in such case. **Figure 8** below illustrates a drive circuit for headphones.

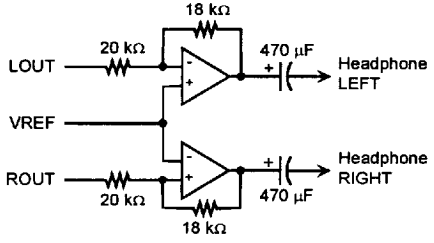

Figure 8: Headphone Drive Connections

Mono Output

This output represents the summed analog output from the left and right channels of the mixer, attenuated by 6 dB to avoid clipping at full scale. It comes with output level control as well as a mute control independent of the stereo line outputs. That is, muting the mono output can be allowed without muting the stereo line outputs. Please refer the MIM and MOM bits of the **Mono Input and Output Control (I26) Mono Input and Output Control (I26)**on page 2-56 for details.

Given the appropriate driver circuit such as that shown in **Figure 9** on page 2-15, the mono output can be used to drive the internal speakers available in most computer systems. As with the mono input, the mute control bit upon power-up, by default, is disabled so that the initial "beeps" during the computer's initialization is incorporated into the audio system.

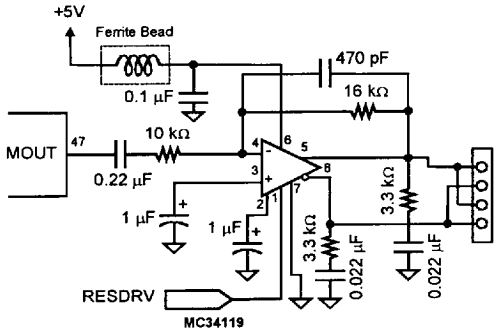

Figure 9: Mono Output

Analog Mixer Gain-Scaling

To prevent clipping at the output of the CH6357, each of the inputs to the analog mixer includes a programmable mixer gain-scaler, as shown in **Figure 10** below. The gain scale can be selected via the MXGS[2:0] bits in the Alternate Feature Enable III register (I27), and one of the selection provided includes automatic gain-scaling. In this mode, the CH6357 automatically detects the total number of inputs applied to the analog mixer and applies the corresponding gain scale necessary to avoid output clipping. The gain scale in automatic mode is determined as follows:

$$G = Automatic = \frac{1}{total\ \#\ of\ inputs\ applied\ to\ the\ mixer}$$

For additional information, please refer to the **Alternate Feature Enable III (I27)** on page 2-57.

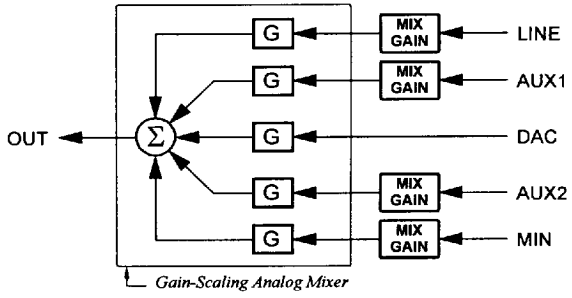

Figure 10: Analog Mixer Gain-Scaling

Miscellaneous Analog Signals

The following paragraphs cover anti-aliasing filter capacitors, voltage references, crystal connections, and power supply decoupling.

Anti-Aliasing Filter Capacitors

The LFILT and RFILT pins, as illustrated in **Figure 4** on page 2-11, should each be connected to a 1000 pF NPO capacitor to ground. Combined with the internal resistor at each pin, these capacitors provide CH6357 with single-pole low-pass filters at the inputs to the ADCs. Therefore the need for external low-pass components is thus eliminated.

Voltage Reference Internal

A 10 µF and a 0.1 µF capacitor (with short wide traces) to analog ground should be connected to the VREFI pin to lower the noise of the internal voltage reference. Digital signals should be placed away from this pin, as with other connections, to avoid degrading the analog performance of the codec. **Figure 4** illustrates this reference bypassing.

Voltage Reference

All analog inputs and outputs are centered around VREF (2.25V nominally). This pin may be used to level shift external circuitry to support DC loads; however, any AC loads must be buffered. Placing a 10 µF capacitor on VREF improves high internal-gain microphone circuits.

Crystals

The crystals shown connected in **Figure 4** should be designed for fundamental mode, parallel resonance operation, with a load capacitance between 10 and 20 pF. The capacitors shown connected with the crystals should have twice the load capacitance specified by the crystal manufacturer. For proper operation, always connect the crystal input pins (X1I & X2I) to a crystal or to an external CMOS compatible clock source. If an external CMOS clock is used the crystal output pins (X1O & X2O) should be left open.

Power Supply Decoupling

Decoupling capacitors should be placed as close as possible to the package pins. **Figure 4** shows the recommended connections when using only a single +5V power supply. The circuitry should be as close to the power supply pins as possible.

Digital Hardware Description

Parallel Data Interface

The CH6357 provides an 8-bit parallel port interface compatible with most computer peripheral busses. This interface is designed to operate on the Industry Standard Architecture (ISA) bus, but will operate on the Extended Industry Standard Architecture (EISA) and Microchannel busses as well with minimal board level logic. Programmed I/O (PIO) and direct memory access (DMA) constitute the two types of accesses that may occur through the parallel bus interface.

The CH6357 has no provision to "hold off" or extend a cycle taking place on the parallel interface. The CH6357, therefore, can accept asynchronous parallel bus cycles without interfering with the flow of data to or from the ADC and DAC sections.

Programmed I/O Registers Interface

The first and simplest method of data exchange on the parallel bus is known as programmed I/O (PIO). This cycle is defined in CH6357 by asserting the chip select (CS*) signal while holding the DMA acknowledge signals PDAK* and CDAK* inactive. For READ cycles, the host strobes the RD* signal and CH6357 places data on the DATA lines. For WRITE cycles, however, the host places the data on the DATA lines and then strobes the WR* signal. The CH6357 then latches the data into the PIO register on the rising edge of the WR* strobe. CS* should remain asserted until all of the READ and WRITE cycles are completed. The programmed I/O capture and playback enable bits (CPIO and PPIO) in the Interface Configuration register (I9) should also be set to allow data transfers using the PIO scheme. Please refer to the **Programmed I/O Timing Diagrams** on page 2-67 for the read and write cycles described above.

Although PIO is the simplest kind of data interchange between CH6357 and the system, digital audio data transfer is usually performed using DMA schemes. PIO is the only cycle that can access the four direct registers and all the indirect registers of CH6357; therefore, it is the only cycle used in accessing the internal control and the status registers of CH6357.

DMA Interface

The second type of parallel bus cycle and scheme most typically used in transferring digital audio data is DMA (Direct Memory Access) transfer. The CH6357's DMA cycles are distinguished from its PIO cycles in that "*handshaking*" occurs between the DMA controller and CH6357. The CH6357 asserts a DMA request signal CDRQ (or PDRQ) while the DMA controller responds with the assertion of an acknowledgement signal CDAK* (or PDAK*). To enable DMA transfers to occur, register bits CPIO and PPIO of the Interface Configuration register (I9) must be cleared. The PEN and/or CEN register bits must be set in order to enable, respectively, any playback and/or capture DMA transfers. Any cycles occuring in this mode are assumed to be DMA cycles and any information present in the addresses, address lines, and CS* line are all ignored.

The CH6357 supports up to two DMA channels and it may assert the DMA request signal at any time. Once asserted, the DMA request remains asserted until a DMA cycle occurs to CH6357. As soon as the falling edge of the last of a full sample's RD* or WR* strobe occurs, the DMA request signal is immediately de-asserted. Depending on which DMA transfer is in progress (capture, playback, or both), transfers can be terminated by resetting the PEN and/or CEN bits in the Interface Configuration register (I9). Termination of DMA transfers may only occur between sample transfers. In the event where a PDRQ (and/or a CDRQ) request signal is asserted while the register bit PEN (and/or CEN) is being reset, the request needs to be acknowledged, and a final sample transfer is completed before PDRQ (and/or CDRQ) is de-asserted.

Dual DMA Channel Mode

In dual DMA channel mode, simultaneous capture and playback is allowed since playback and capture DMA requests and acknowledges occur on independent DMA channels. To operate in this mode, the SDC register bit in the Interface Configuration register (I9) must be reset (SDC=0) while setting the PEN and CEN register bits (PEN=CEN=1). The PEN, CEN, and SDC register bits can be readily changed without asserting Mode Change Enable (MCE) in the index address register, R0, thereby allowing proper full duplex control in applications using playback and capture independently.

Single DMA Channel Mode

In single DMA channel mode, playback and capture occur only on the playback DMA channel. The playback DMA transfer occurs exactly as in dual channel mode. However, since only a single DMA channel is available, the capture DMA transfer occurs on the playback DMA channel as well. As a result, capture DMA requests and acknowledges now occur, respectively, in the PDRQ and PDAK* pins. Simultaneous capture and playback cannot be performed in the single DMA channel mode but playback and capture can be distinguished in this mode by the state of the playback enable (PEN) or capture enable (CEN) bits in the Interface Configuration register (I9). If both PEN and CEN are set simultaneously during the single DMA channel mode, playback acts as the default mode. The CDRQ during this mode is inactive (logic low) while the CDAK* pin is ignored by CH6357. Single channel mode has no effect on PIO accesses.

FIFOs

There is a 32-sample FIFO available in both playback and capture paths of CH6357. These FIFOs are transparent and provide a useful method for buffering asynchronous data. Having these 32-sample FIFOs in both paths reduce the likeliness of experiencing underrun and overrun errors. For more information on underrun and overrun errors, please refer to **"Error Conditions"** on page 2-31.

Playback FIFO

During playback mode, the playback FIFO tries to remain as full as possible as it continuously requests data whenever positions inside the 32-sample FIFO becomes available. If the system cannot provide data within a sample period, data from the FIFO is emptied to avoid a momentary loss of audio data. If the FIFO, however, runs out of data, CH6357 either: (a) continuously outputs the last valid sample to the DACs to eliminate any pops from occurring, or (b) forces the output to the DACs to be zero (at center scale) until the next complete sample arrives. This option can be accessed through the DACZ register bit of the Alternate Feature Enable I register (I16).

Capture FIFO

During capture mode, the capture FIFO tries to remain as empty as possible to provide sufficient space for incoming data. However, if the system cannot receive data before the next data arrives (i.e. within a sample period), the 32-sample FIFO starts filling, to prevent the loss of data in the audio data stream. In the case when the FIFO is full and incoming data arrives, the new sample will be discarded and the FIFO contents will be retained until transferred.

Programmable FIFO Request Control

The efficiency of the CH6357 FIFOs is further increased by the availability of the programmable request control. This control allows both the capture and playback FIFOs to generate DMA transfer requests when the FIFOs reach a predefined capacity. For instance, the FIFOs can be programmed to request DMA transfers whenever it is 50% full (capture) or 50% empty (playback). As a result, the CPU bus can be used efficiently by controlling the condition in which DMA transfers are conducted.

The FIFO request control is available only in Chrontel mode and is programmable via the FT[1:0] bits in the ID & FIFO Control register (I29). Please refer to the ID & FIFO register on page 2-59 for the FIFO capacity threshold selections available.

Digital Audio Serial Interface

Serial Port

CH6357's serial interface mode is available only in Chrontel mode and is software selectable via the Alternate Feature Enable I register (I16). The serial interface is enabled by setting the serial interface enable bit SIE (i.e., SIE=1) while the MCE bit is asserted high. Once enabled, the serial port will support serial data at the sampling frequency defined in the Fs and Playback Data Format register (I8).

Serial Port with Rate Conversion

CH6357's serial interface mode with data rate conversion is available in Chrontel mode only. To enter this mode, the rate change enable register bit, RCE, of the Capture Data Format register (I28) is set first (RCE=1) followed by setting the SIE register bit (SIE=1) of index register I16. MCE must be asserted high before RCE and SIE bits are modified.

Entering the serial interface mode with rate conversion automatically sets the ADCs and DACs' sampling frequencies to 44.1 kHz while maintaining the codec's parallel interface sampling frequency to the selected rate in index register (I8). The sampling frequencies supported at the interface include 44.1 kHz, 22.05 kHz, 11.025 kHz and 5.51 kHz. Having this feature allows CH6357 to interface, for example, to the Yamaha OPL4/OPL3-L music synthesizers or effect processor directly without using an external serial DAC.

While in this mode, the ADCs are constantly sampling input signal at 44.1 kHz. The digital decimator can down-convert this sampling rate to the rates required of audio data at the parallel bus. Likewise, the DACs are constantly running at 44.1 kHz. The digital interpolator, however, up-converts the sampling frequency of the audio data received from the parallel bus from rates lower than 44.1 kHz back to 44.1 kHz to match the sampling rate of the DACs.

Serial Output

The serial interface mode allows audio data to be directed to the serial port for audio signal processing. A captured microphone input and an accompanying background sound, for instance, can be processed for sound effects (e.g. reverb, echo, pitch change, etc.) as shown in the karaoke example in **Figure 11** below. The captured microphone input from the ADCs is first directed through SDOUT to an effect processor. The effect processor then adds sound effects to the microphone data and the accompanying sound data from the OPL4. The CH6357 receives the effect processor's output through SDIN and directs it to the DACs for playback. For some of the functions described, please refer to **Figure 1** on page 2-1.

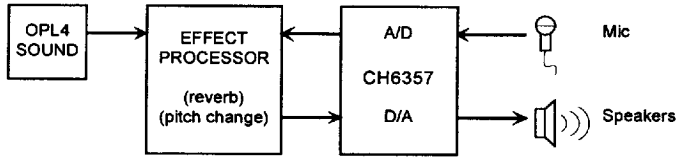

Figure 11: Karaoke Example

Digital Mixer Gain-Scaling

To prevent clipping the output of the digital mixer, programmable gain-scaling is included with the digital mixer, as shown in **Figure 12** below, similar to that of the analog mixer. The digital mixer gain scale can be programmed as one (K=1) or one-half (K=0.5), and is selected via the SIGS bit in the Alternate Feature Enable III register (I27). For additional information, please refer to the **Alternate Feature Enable III (I27)** register on page 2-57.

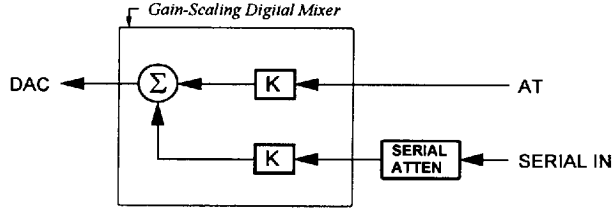

Figure 12: Digital Mixer Gain-Scaling

Serial Port Data Formats

CH6357's serial audio data formats are illustrated in **Figures 13** and **14**. Only 16-bit formats are supported and these formats are selected through the serial format select bits, SFL[1:0], of the Alternate Feature Enable I register (I16).

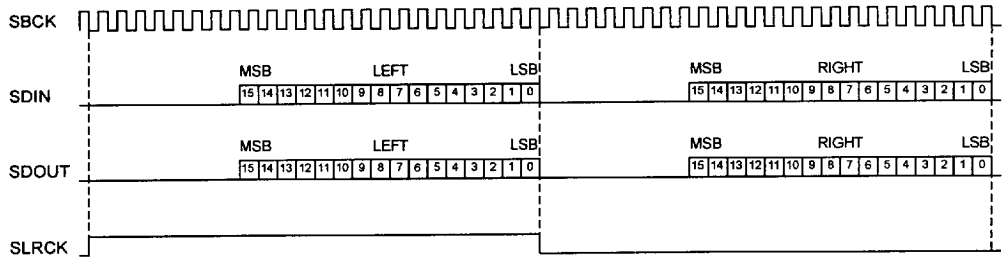

Figure 13: Serial Data Format 1 (SBCK = 48Fs)

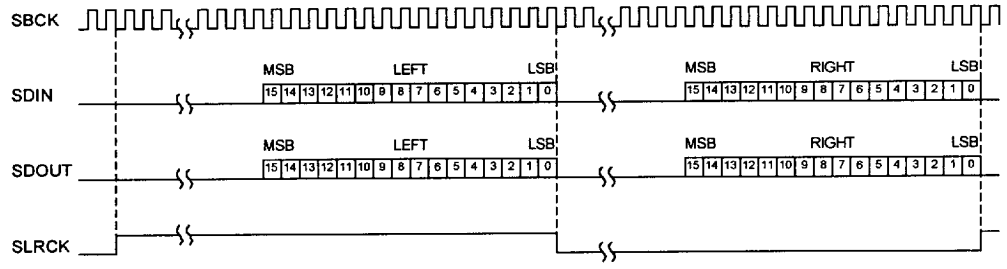

Figure 14: Serial Data Format 2 (SBCK = 64Fs)

Figures 15 through **17** provide examples of how CH6357 interfaces with the Yamaha OPL4/OPL3 music synthesizers or the Yamaha YS225 effect processor

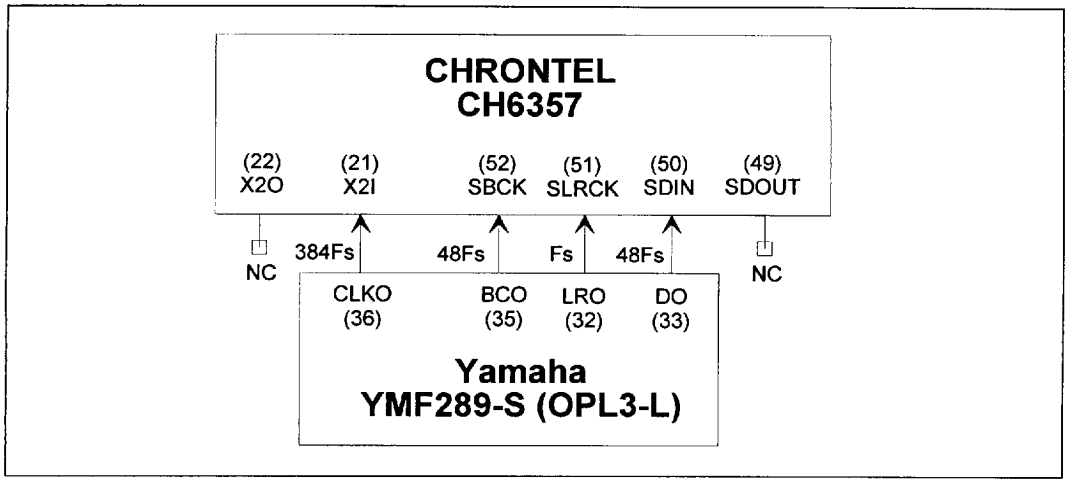

Figure 15: CH6357 Interface with Yamaha YMF289-S (OPL3-L) in 48-pin SQFP

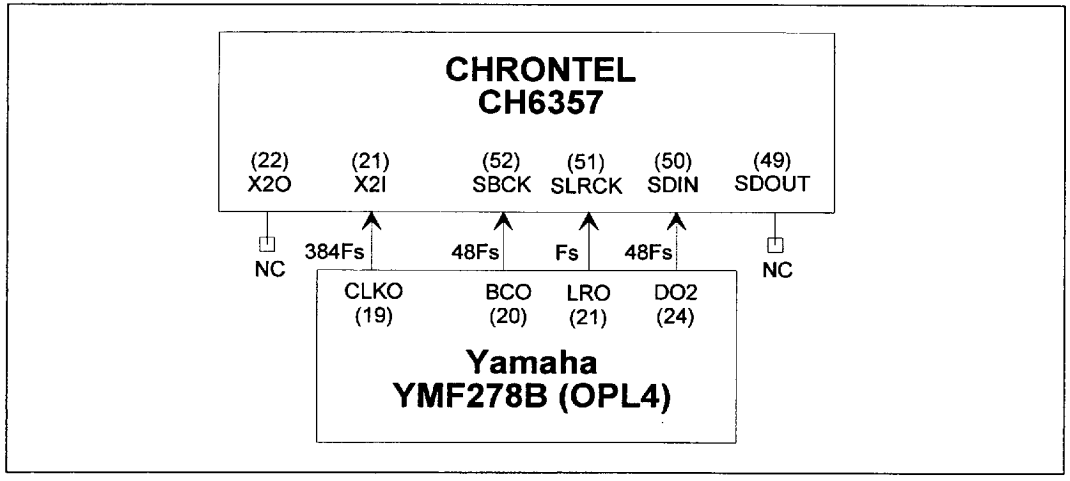

Figure 16: CH6357 Interface with Yamaha YMF278B (OPL4)

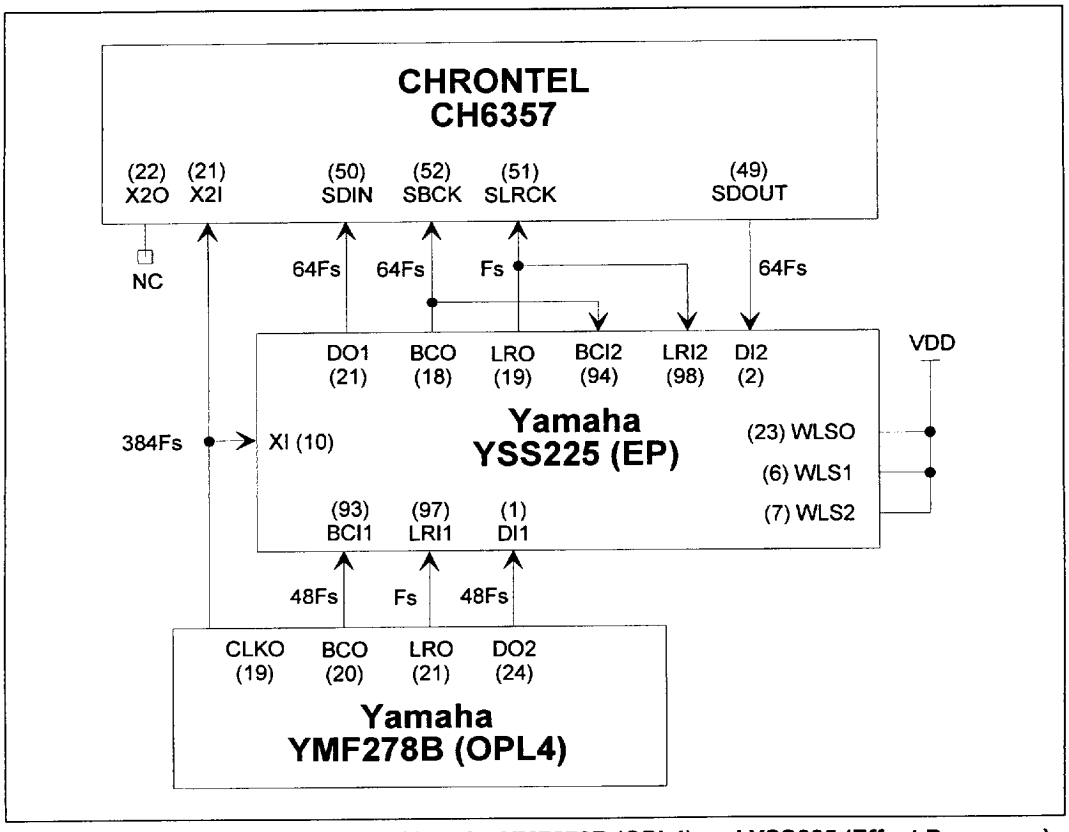

Figure 17: CH6357 Interface with Yamaha YMF278B (OPL4) and YSS225 (Effect Processor)

High Current Bus Drivers

The CH6357 has built-in 16 mA bus drivers which in many cases eliminate the need for off-chip drivers. However, if a full 24 mA drive is required, CH6357 generates the appropriate driver DIRECTION and ENABLE control signals for external IC buffers such as the 74F245. The built-in current drivers provide the drive needed for the data bus, the DMA request line, and the interrupt request line.

Miscellaneous Signals

Optimum performance of CH6357 requires isolating some power supply pins from each other. For instance, the VD1 and VD2 pins should be isolated from the rest of the digital power supply pins since they provide the power to the asynchronous parallel bus of the codec. These pins can be directly connected to the digital power supply. VD3 and VD4 digital power supply pins, on the other hand, supply power to the internal digital section of CH6357 and should optimally remain more noise-free than VD1 and VD2. To accomplish this, a typical connection using a ferrite bead is recommended (as shown in **Figure 4** on page 2-11). The analog power supplies VA1 and VA2, similarly, should be as clean as possible to reduce coupling and performance degradation of CH6357's analog section.

Programming Consideration

Changes to CH6357's functional modes are only allowed when one or a combination of the following bits are asserted: MCE (R0), PMCE (I16), and CMCE (I16).

- changes to the SFSL[1:0], SIE bits of the Alternate Feature Enable I register (I16) and the RCE bit of the Capture Data Format register (I28) can only occur when MCE is asserted and when the CH6357 is in Chrontel programming mode.
- changes to the four least significant bits (CSF[2:0], C2SL) of the Fs and Playback Data Format register (I8) can only occur when MCE is asserted. Changes to the four most significant bits (FMT[1:0], C/L*, S/M*) of the Fs and Playback Data Format register (I8) can occur when either the MCE or PMCE bit is asserted.
- Changes to the four most significant bits (FMT[1:0], C/L*, S/M*) of the Capture Data Format register (I28) can occur when either the MCE or CMCE bit is asserted.
- except for the CEN and PEN bits, changes to the Interface Configuration register (I9) can only occur when MCE is asserted. The CEN and PEN bits can be changed *on-the-fly* through programmed I/O writes.

  In DMA mode, the new values of CEN or PEN bits are *only* recognized once the pending DMA sample is transferred.

Chrontel Programming Mode

Some functions provided with the CH6357, such as the digital audio serial interface, FIFO request control, and analog and digital mixer gain-scaling, are programmable only through Chrontel programming mode. To enter or exit this mode, a read must be first performed to the Version and ID register (I25), followed by a write of the content's bit-wise negation back to the Version and ID register. For example, if 0x80H was read from the Version and ID register, 0x7FH must be written back to the Version and ID register.

Chrontel programming mode functions are activated by entering Chrontel programming mode, programming the register bits that control these functions, and exiting Chrontel programming mode. The functions remain active until Chrontel programming mode is entered again to deactivate them.

The CTMODE bit of the Alternate Features Enable III register (I27) will be set (i.e., CTMODE=1) once the CH6357 is in Chrontel programming mode. For a summary of the specific bits programmable through Chrontel programming mode, please refer to **Table 10** on page 2-33.

Power Down and Initialization

The CH6357 is placed into power down mode by pulling the PD* pin low. During this mode, the codec returns 80H for all reads by the host computer indicating that the codec is currently unable to respond. All analog circuits are turned off while in this mode.

Initialization takes place when CH6357 exits from power down mode. The low-to-high transition of the PD* signal triggers the beginning of the initialization process wherein a full calibration of CH6357 takes place. As soon as initialization is completed, all registers are set to their default values as defined in the register definition section. As in the power down mode, CH6357 returns 80H for all READs and ignores all WRITEs by the host computer while in initialization.

Auto-Calibration

The CH6357 automatically calibrates the offset of its ADCs. Auto-calibration is enabled whenever CH6357 returns from the Mode Change Enable (MCE) state *and* the auto-calibrate enable bit, ACAL, in the Interface Configuration register (I9) has been set.

Polling the Auto-Calibrate In-Progress bit (ACI) in the Error Status & Initialization register (I11) will indicate whether calibration has been completed: ACI=1 will indicate "calibration is still in progress" whereas ACI=0 will indicate "calibration is completed." Auto-calibration takes at least 168 sample periods to complete and in the event data transfer is enabled during this cycle, auto-calibration will be completed first before data is transferred.

To enable auto-calibration, complete the following steps:

1. Assert the mode change enable bit (MCE=1) in the Index Address register (R0).
2. Set the ACAL bit (ACAL=1) in the Interface Configuration register (I9).
3. Reset the MCE bit of the Index Address register (R0) to exit from the Mode Change Enable.
4. Wait until 80H is *NOT* returned to the host computer.
5. Wait until "calibration is completed" (i.e. when ACI=0 in register (I11)) to proceed.

Changing the Sampling Rate

The sampling frequency selected in the Data Format register (I8) is important in synchronizing the internal states of CH6357. Changing the clock source or the clock frequency divisor, therefore, requires a special sequence of operation to assure proper operation of the CH6357.

To change the Sampling Rate, complete the following steps:

1. Assert the mode change enable bit (MCE=1) in the Index Address register (R0).
2. In a single write cycle, set the Clock Frequency Divide Select (CFS) and/or Clock 2 Source Select (C2SL) bits of the Fs & Playback Data Format register (I8) to the desired value. Data format may also be changed if necessary.
3. Allow CH6357 to resynchronize its internal states to the new clock. The codec will return 80H for all READs while ignoring all WRITEs by the host computer. (In order to minimize the start-up time when switching between crystal clock sources, the XTALE bit, as described in the **Alternate Feature Enable II (I17)** on page 2-51, could be set high).
4. Poll the Index Address register (R0) until 80H is *NOT* returned to the host computer. Normal operation resumes as soon as the CH6357 no longer returns this value.
5. Exit from Mode Change Enable by resetting the MCE bit of the Index Address register (R0).

Note: MCE must be asserted before changes to CFS[2:0] and C2SL bits of the Fs and Playback Data Format register (I8) can occur. Changes to the FMT[1:0], C/L*, and S/M* bits of the Fs and Playback Data Format register (I8) can take place, however, when either MCE or PMCE is asserted.

Audio Data Formats

Depending on the mode selected, CH6357 supports up to six digital audio data formats. Regardless of the format, however, the left channel data is always transferred before the right channel data. Similarly, the left sample always comes first in the data stream regardless of its size (8-bit or 16-bit).

MODE 1	MODE 2
Audio Data Formats: • 16-bit Signed "Little Endian" • 8-bit Unsigned • 8-bit Companded, μ-Law • 8-bit Companded, A-Law	Audio Data Formats: • 16-bit Signed "Little Endian" • 8-bit Unsigned • 8-bit Companded, μ-Law • 8-bit Companded, A-Law • 4-bit ADPCM • 16-bit Signed "Big Endian"
Fs & Playback Data Format register (I8) determines audio data format for both capture and playback.	Fs & Playback Data Format register (I8) determines audio data format for playback while Capture Data Format register (I28) determines the audio data format for capture.

Note: 1. "Little Endian" format refers to the byte ordering of a multiple word as having the least significant byte occupying the lowest memory address.
2. "Big Endian" format is similar to the Little Endian format except the upper byte is transferred first before the lower byte.

16-bit Signed

The 16-bit signed format (also called 16-bit 2's complement) is the standard method of representing 16-bit digital audio. This format delivers a theoretical 96 dB dynamic range and is the standard format for compact disk audio players. This format represents numbers with values ranging from –32,768 (8000H) to +32,767 (7FFFH) with –32,768 (8000H) and +32,767 (7FFFH) representing, respectively, the minimum and maximum analog amplitudes.

8-bit Unsigned

The 8-bit unsigned format is the format commonly used in the personal computer industry. This format delivers a theoretical 48 dB dynamic range and it represents the minimum and maximum analog amplitudes using numbers ranging from 0 (00H) to 255 (FFH).

8-bit Companded

The 8-bit companded format (A-Law and μ-Law) comes from the telephone industry. The United States and Japan use the μ-Law as the standard, whereas the A-Law is the European standard. This format uses a non-linear companding transfer function to assign more digitalization codes to lower amplitude analog signals while sacrificing precision on the higher amplitude signals. Companded audio, as a result, allows delivery of either 64 or 72 dB of dynamic range using only 8 bits per sample. The CH6357 uses A-Law and μ-Law formats conforming to the CCITT G.711 specifications. Please refer to the A-Law and μ-Law standards for exact definitions.

ADPCM Compression / Decompression

In MODE 2, CH6357 comes with Adaptive Differential Pulse Code Modulation (ADPCM) for improved performance and compression ratios over the μ-Law or A-Law formats. The ADPCM format complies with the IMA standard and provides a 4-to-1 compression ratio (i.e., 4 bits are saved for each 16-bit sample captured). Note that since samples are compressed in the ADPCM data format, the DMA Base register count no longer on a per sample basis. For specific information regarding this format, contact IMA.

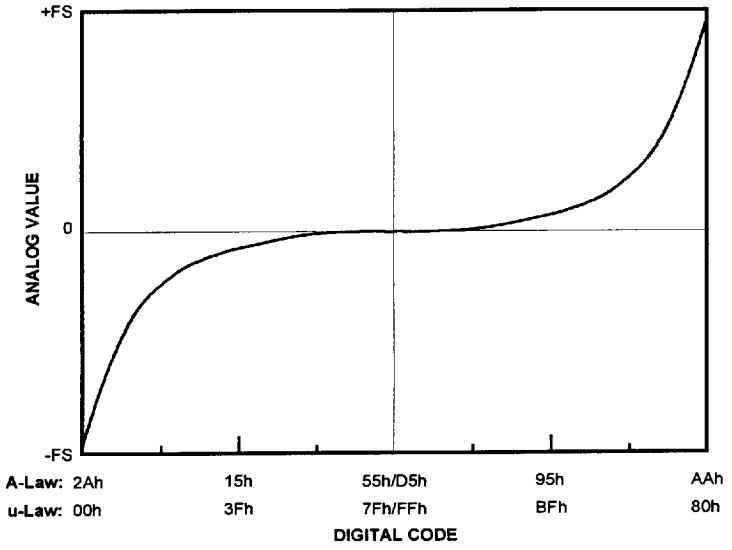

Figure 18: Companded Transfer Function

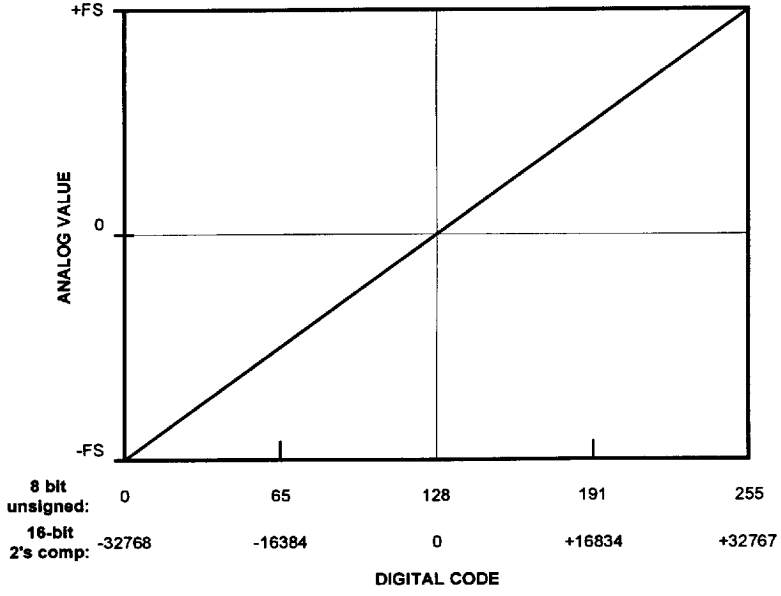

Figure 19: Linear Transfer Function

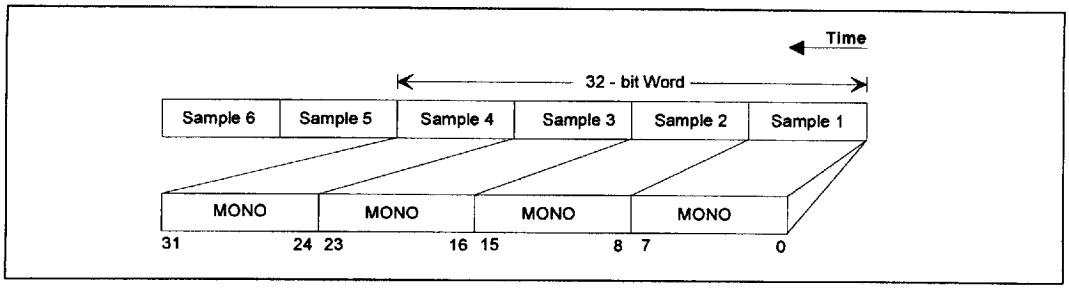

Figure 20: 8-bit Mono, Unsigned Audio Data

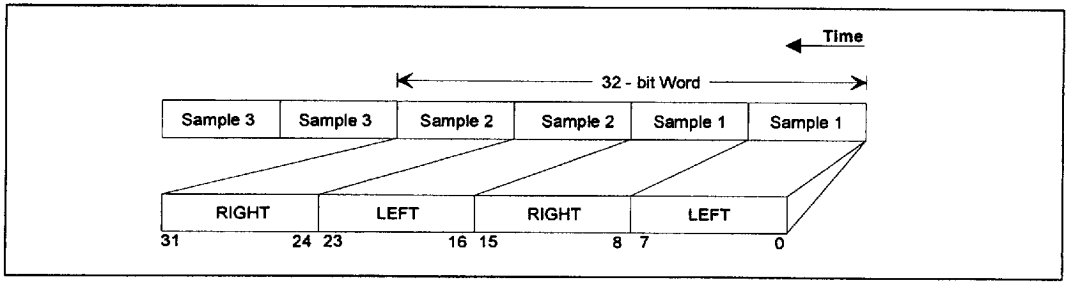

Figure 21: 8-bit Stereo, Unsigned Audio Data

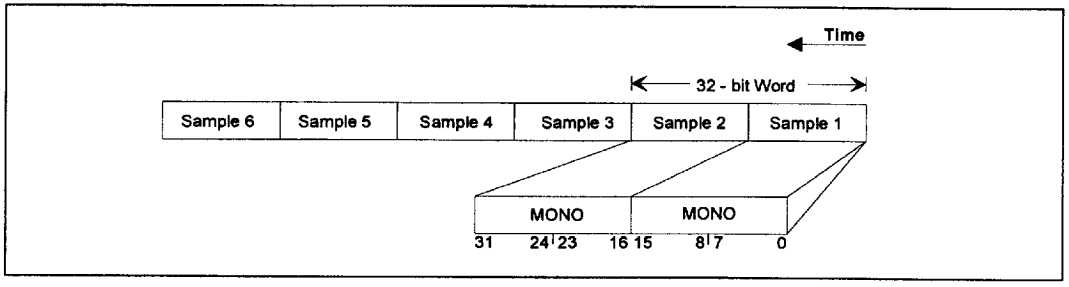

Figure 22: 16-bit Mono, Signed Little Endian Audio Data

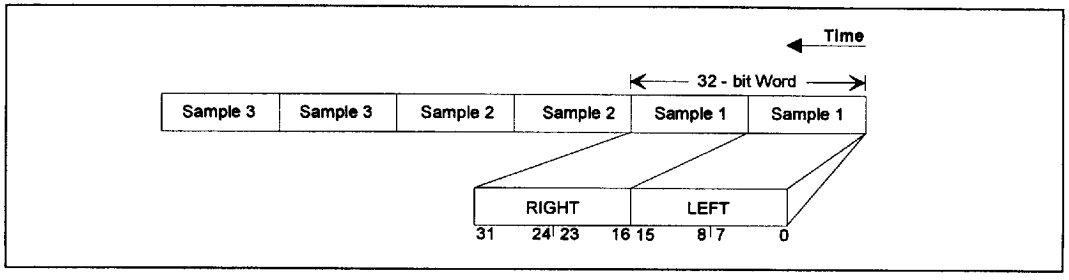

Figure 23: 16-bit Stereo, Signed Little Endian Audio

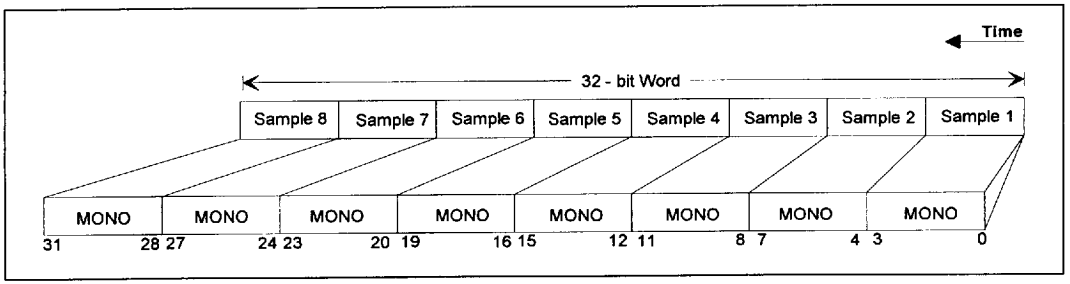

Figure 24: 4-bit Mono, ADPCM Audio Data

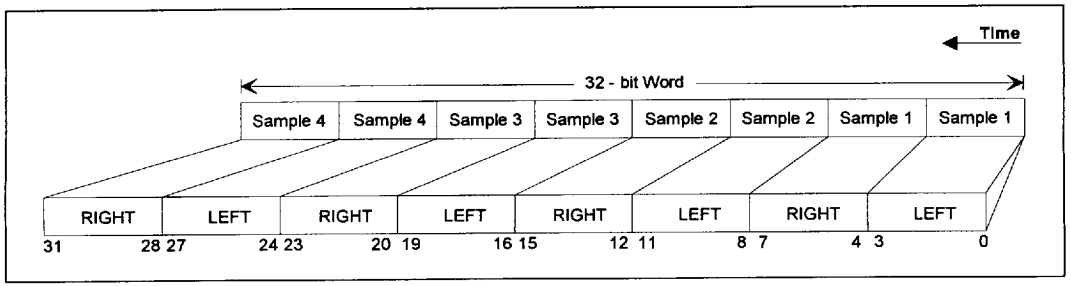

Figure 25: 4-bit Stereo, ADPCM Audio Data

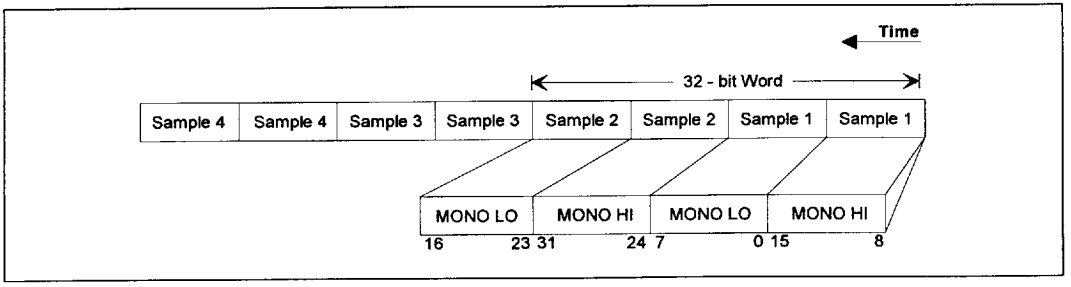

Figure 26: 16-bit Mono, Signed Big Endian Audio Data

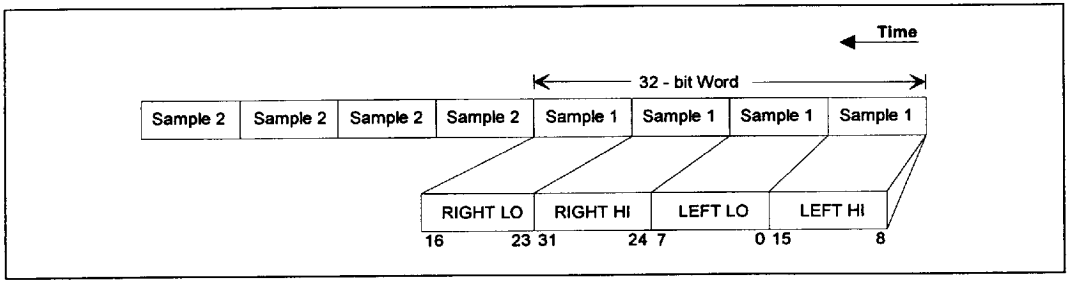

Figure 27: 16-bit Stereo, Signed Big Endian Audio Data

DMA Registers

The CH6357 is equipped with programmable DMA Base registers that provide an external count mechanism required by the ISA DMA controller for notifying the host CPU, via interrupt, of a full DMA buffer. These DMA base registers allow such interrupts to occur and they allow easier integration of CH6357 into ISA systems.

These DMA base registers are used for containing the count value for the number of DMA samples to be transferred per interrupt. To load the count value, the lower byte of the count value must be first written into the Lower Base Count register and then followed by the count value's upper byte written into the Upper Base Count register. Once a value is written into the Upper Base register, the value in both Base registers is loaded into the Current Count register. As soon as transfers are enabled, the Current Count register is decremented for every sample transferred by a DMA cycle (except in the ADPCM format) until zero is reached. The sample transferred immediately after zero will generate the interrupt and reinitialize the Current Count register with the count value contained in the DMA base registers. (DMA transfers are enabled by setting the PEN/CEN bits in the Interface Configuration (I9) register while clearing the PPIO/CPIO bits. Changes to PPIO/CPIO can only be performed if the MCE bit is set)

The count value loaded in the DMA registers for all data formats (excluding ADPCM) is calculated as follows:

DMA Base Register = Ns - 1

where: **Ns** = *the number of samples transferred per DMA interrupt*

DMA Base Register = *the concatenation of the upper and lower DMA Base registers*

Note that stereo data contain samples twice as many as mono data, whereas 8-bit data contains the same number of samples as 16-bit data.

For the ADPCM data format, keeping track of the transfer of compressed data is much more significant than keeping track of the number of samples transferred. The count value loaded in the DMA base registers, therefore, is calculated differently from the other data formats and is calculated as follows::

DMA Base Register = (NB / 4) - 1

where: **NB** = *the number of bytes transferred per DMA interrupt*

DMA Base Register = *the concatenation of the upper and lower DMA Base registers*

Playback DMA Registers

In MODE 2, these playback DMA registers (I14 & I15) are dedicated for playback operation only. They contain the count value for the number of *playback* samples that will be transferred between interrupts. In MODE 1, however, where a single DMA channel exists for both playback and capture, these registers are used for loading the count value for both capture and playback operation.

Whenever the playback Current Count register *rolls under*, the Playback Interrupt bit of Indirect Register (I24) is set (PI=1) causing the INT bit of Status Register R2 to be set as well. The interrupt can be cleared by clearing the Playback Interrupt bit in register I24 (PI=0), or by writing any value to the Status Register R2.

Capture DMA Registers

The capture DMA Base registers (I30 & I31) in MODE 2 provide a second pair of Base registers dedicated for capture use only. These registers contain the count value for the number of *capture* samples that will be transferred between interrupts. By having this second pair of registers, full-duplex operation is allowed. That is, by having one base register dedicated for capture and another for playback, as it is in this mode, simultaneous capture and playback operations can occur independently.

Whenever the Capture Current Count register *rolls under*, the Capture Interrupt bit of Indirect Register (I24) is set (CI=1) causing the INT bit of Status Register R2 to be set as well. The interrupt can be cleared by clearing the Capture Interrupt bit in register I24 (CI=0), or by writing any value to the Status Register R2.

Digital Loopback

Digital loopback is enabled by setting the loopback enable bit, LBE, in register (I13). Loopback allows digital data from the ADCs to get routed to the DACs. For example, incoming microphone data can be mixed with playback music data supplied to the DACs using loopback. The output from the ADCs is first digitally attenuated by an amount specified by the control bits LBA5-LBA0 of the Loopback Control register (I13) and then summed with the data supplied to the input of the DACs. In case the sum exceeds full scale, the appropriate full scale (clipped) value is sent to the DACs. The DACs will output the summed data attenuated by an amount specified, this time, by the control bits of DAC Output Control registers (I16 & I17).

Since CH6357 allows different data format selection to exist between capture and playback, if the capture channel was set to mono while the playback channel was set to stereo, the mono input will be looped back to both DAC channels.

Timer Registers

A 16-bit programmable timer is provided for audio/video synchronization and for applications where a precise, high resolution time reference is required. The timer registers contain the desired count length value; however, the crystal selected determines the exact time base available. To load the count value, the upper byte of the count value must be first written into the Timer Upper Byte register and then followed by the count value's lower byte written into the Timer Lower Byte register. Once a value is written into the Timer Lower Byte register, the value in both timer registers is loaded into the Current Count register. For more information, please refer to the **Timer registers (I20 & I21)** on page 2-53 and the **Fs and Playback Data Format (I8)** on page 2-43.

To set the Timer registers, the Timer Enable bit, TE, in the Alternate Feature Enable register (I16) must be set while the Timer registers must be loaded with the value of the desired count length. This value gets written into the internal Current Count register where it will be decremented, approximately, every 10 µs. When the Current Count register goes down to zero, the Timer Interrupt bit (TI) is set in the Alternate Feature Status register (I24) causing the INT bit of Status register (R2) to be set as well. On the next timer clock, the Timer register's count value once again gets written into the internal Current Count register and the process is repeated. The interrupt is cleared by clearing the Timer Interrupt bit (TI) or by writing any value to the Status register (R2).

Interrupts

The interrupt bit, INT, of the Status register (R2) always reflects the internal interrupt state of CH6357. This INT bit will be set (INT=1) whenever any of the Current Count registers (DMA playback, DMA capture, Timer) *rolls under*, and it will remain set until cleared. Clearing the INT bit can be accomplished by a write of **ANY** value to the Status Register (R2), or by clearing the appropriate interrupt bit(s) (PI, CI, TI) in the Alternate Feature Status Register (I24).

The Interrupt Enable (IEN) bit in the Pin Control register (I10) conveniently controls whether the internal interrupt event is reflected to the interrupt pin (IRQ) of the CH6357. When IEN = logic "high", the status of the IRQ pin corresponds to the status of the INT bit. On the other hand, if IEN = logic "low", the IRQ pin will be forced low and it will not reflect the status of the INT bit. The internal INT bit of CH6357 functions regardless of IEN bit's status.

Error Conditions

Data overrun or underrun conditions occur whenever data is not removed from or supplied to CH6357 in the appropriate amount of time. The appropriate amount of time needed to transfer this data is dependent on the frequency selected within CH6357 and/or, in some cases, how fast the system can respond to such data transfers.

Capture overrun error occurs whenever the host fails to read the capture data from CH6357 before the next data arrives. If an overrun occurs, new data will be ignored while keeping the last whole sample available for the DMA interface to read. The DMA samples being transferred will not be overwritten.

Likewise, playback underrun error occurs whenever the host fails to supply to CH6357 playback data in time for it to be played. If an underrun occurs, the CH6357 has the capability to either force the input to the DACs to zero (at center scale) or continuously output the last valid sample until the next complete sample arrives. For this option, please refer to the DACZ bit of the **Alternate Feature Enable I (I16)** register on page 2-49.

Register Map

There are four locations of direct registers and 32 locations (MODE 2) or 16 locations (MODE 1) of indirect registers as described in **Tables 7** and **8**. Only two address pins are required to access these registers. The first two direct registers give access to the indirect registers which are indexed by the value most recently written to the index address register. The last two direct registers provide status information and allow audio data to be transferred to and from CH6357 without using DMA cycles or indexing.

Table 7 • Direct Registers (R0 - R3)

	Address		Description
R0	0	0	Index Address Register
R1	0	1	Indexed Data Register
R2	1	0	Status Register (Read only)
R3	1	1	PIO Data Register

Table 8 • Indirect Registers (I0 - I31)

Index	Register Name
I0	Left ADC Input Control
I1	Right ADC Input Control
I2	Left Auxiliary #1 Input Control
I3	Right Auxiliary #1 Input Control
I4	Left Auxiliary #2 Input Control
I5	Right Auxiliary #2 Input Control
I6	Left DAC Output Control
I7	Right DAC Output Control
I8	Fs and Playback Data Format
I9	Interface Configuration
I10	Pin Control
I11	Error Status and Initialization
I12	MODE and ID (MODE 2 bit)
I13	Loopback Control
I14	Playback Upper Base Count
I15	Playback Lower Base Count
I16	Alternate Feature Enable I
I17	Alternate Feature Enable II
I18	Left Line Input Control
I19	Right Line Input Control
I20	Timer Low Byte
I21	Timer High Byte
I22	Left Serial Input Control
I23	Right Serial Input Control
I24	Alternate Feature Status
I25	Version and Chip ID
I26	Mono Input and Output Control
I27	Alternate Feature Enable III
I28	Capture Data Format
I29	ID and FIFO Control Register
I30	Capture Upper Base Count
I31	Capture Lower Base Count

Table 9 • Summary of Direct Registers

	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R0	0	0	INIT	MCE	TRD	IA4 [1]	IA3	IA2	IA1	IA0
R1	0	1	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
R2	1	0	CU/L*	CL/R*	CRDY	SER	PU/L*	PL/R*	PRDY	INT
R3	1	1	D7	D6	D5	D4	D3	D2	D1	D0

Table 10 • Summary of Indirect Registers

IA4 - IA0	D7	D6	D5	D4	D3	D2	D1	D0
0	LSS1	LSS0	LMGE	–	LAG3	LAG2	LAG1	LAG0
1	RSS1	RSS0	RMGE	–	RAG3	RAG2	RAG1	RAG0
2	LX1M	–	–	LX1G4	LX1G3	LX1G2	LX1G1	LX1G0
3	RX1M	–	–	RX1G4	RX1G3	RX1G2	RX1G1	RX1G0
4	LX2M	–	–	LX2G4	LX2G3	LX2G2	LX2G1	LX2G0
5	RX2M	–	–	RX2G4	RX2G3	RX2G2	RX2G1	RX2G0
6	LDM	–	LDA5	LDA4	LDA3	LDA2	LDA1	LDA0
7	RDM	–	RDA5	RDA4	RDA3	RDA2	RDA1	RDA0
8 [3]	FMT1 [1, 6]	FMT0 [6]	C/L* [6]	S/M* [6]	CSF2	CSF1	CSF0	C2SL
9 [3]	CPIO	PPIO	–	–	ACAL	SDC	CEN	PEN
10	XCTL1	XCTL0	–	–	DEN	–	IEN	–
11	COR	PUR	ACI	DRS	ORR1	ORR0	ORL1	ORL0
12	1	MODE2	–	–	ID3	ID2	ID1	ID0
13	LBA5	LBA4	LBA3	LBA2	LBA1	LBA0	–	LBE
14 [2]	PUB7	PUB6	PUB5	PUB4	PUB3	PUB2	PUB1	PUB0
15 [2]	PLB7	PLB6	PLB5	PLB4	PLB3	PLB2	PLB1	PLB0
16	OLB	TE	CMCE [5]	PMCE [5]	SFSL1 [4]	SFSL0 [4]	SIE [4]	DACZ
17	–	DGRST [5]	–	–	–	–	XTALE [5]	HPF
18	LLM	–	–	LLG4	LLG3	LLG2	LLG1	LLG0
19	RLM	–	–	RLG4	RLG3	RLG2	RLG1	RLG0
20	TL7	TL6	TL5	TL4	TL3	TL2	TL1	TL0
21	TU7	TU6	TU5	TU4	TU3	TU2	TU1	TU0
22	LSIM [5]	–	–	LSIA4 [5]	LSIA3 [5]	LSIA2 [5]	LSIA1 [5]	LSIA0 [5]
23	RSIM [5]	–	–	RSIA4 [5]	RSIA3 [5]	RSIA2 [5]	RSIA1 [5]	RSIA0 [5]
24	–	TI	CI	PI	CU	CO	PO	PU
25	V2	V1	V0	–	–	CID2	CID1	CID0
26	MIM	MOM	–	–	MIA3	MIA2	MIA1	MIA0
27	SOM [5]	SOSL [5]	ATM [5]	SIGS [5]	MXGS2 [5]	MXGS1 [5]	MXGS0 [5]	CTMODE
28 [3]	FMT1 [7]	FMT0 [7]	C/L* [7]	S/M* [7]	–	–	–	RCE [4]
29	CTID2	CTID1	CTID0	CTIV1	CTIV0	BDBUD [5]	FT1 [5]	FT0 [5]
30	CUB7	CUB6	CUB5	CUB4	CUB3	CUB2	CUB1	CUB0
31	CLB7	CLB6	CLB5	CLB4	CLB3	CLB2	CLB1	CLB0

Note:
1. IA4 and FMT1 bits are only available in Mode 2 (IA = 12, bit 6 = 1). Since IA4 is only available in Mode 2, registers 16 - 31 are only available in Mode 2 also.
2. In Mode 1, the playback base registers (upper and lower) are used for both playback and capture.
3. MCE must be set before changing any bits in these registers (Except CEN and PEN, which may be changed on-the-fly).
4. CH6357 must be in Chrontel programming mode along with the MCE bit set high before changes to these bits can occur.
5. CH6357 must be in Chrontel programming mode before changes to these bits can occur.
6. These bits may be modified independently when the PMCE bit in index register I16 is set (PMCE=1).
7. These bits may be modified independently when the CMCE bit in index register I16 is set (CMCE=1).

Direct Registers Description

Index Address Register (R0)

D7	D6	D5	D4	D3	D2	D1	D0
INIT	MCE	TRD	IA4	IA3	IA2	IA1	IA0

The initial value of this register upon power up is 010x 0000. During initialization and power down, this register ignores all writes and returns 1000 0000 (80H) for all reads by the host computer.

INIT **Initialization bit for CH6357**

"1" : indicates CH6357 is in a state where it cannot respond to the parallel interface cycles. This bit is read only.

"0" : normal operation.

MCE **Mode Change Enable**

"1" : enables functional mode changes to the CH6357. This bit must be asserted high whenever:

- changes to the Data Format (I8 & I28) and the Interface Configuration (I9) registers are needed. The CEN (Capture Enable) and PEN (Playback Enable) bits of index register I9 are exceptions since they can be changed *on-the-fly*.
- the SIE and SFSL[1:0] bits of index register I16 needs to be modified.
- the rate change enable bit RCE is to be activated.

MCE should be cleared at the completion of changes to the register.

"0" : mode change disabled

TRD **Transfer Request Disable**

This bit determines whether DMA transfers and requests can be ceased whenever the INT bit of the status register is asserted.

"1" : The DMA transfer will be disabled when the INT bit asserted HIGH. CDRQ and PDRQ can be generated only if the INT bit is LOW.

"0" : DMA requests (CDRQ and PDRQ) can occur regardless of INT bit's status.

IA4 **Index Address**

In MODE 1, this bit is RESERVED.

In MODE 2, this bit allows access to additional Indirect registers 16 - 31.

"1" : Enables access to indirect registers 16-31.

"0" : Disables access to indirect registers 16-31.

IA3 - IA0 **Index Address**

These bits specify the address of the CH6357 register accessed by the Indexed Data register (R1). These bits allow read/write access to Indirect Registers 0 - 15.

Indexed Data Register (R1)

D7	D6	D5	D4	D3	D2	D1	D0
ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

ID7 - ID0 **Indexed Data Register**

These bits are the indirect register referenced by the Indexed Address Register (R0). During initialization and power down, this register ignores all writes and returns 10000000 (80H) for all reads by the host computer.

Status Register (R2, Read Only)

D7	D6	D5	D4	D3	D2	D1	D0
CU/L*	CL/R*	CRDY	SER	PU/L*	PL/R*	PRDY	INT

CU/L* **Capture Upper / Lower Byte**

"1" : the capture data ready is for the upper byte, or any 8-bit mode

"0" : the capture data ready is for the lower byte

CL/R* **Capture Left / Right Sample**

"1" : the capture data waiting is for the left channel or for MONO data

"0" : the capture data waiting is for the right channel

CRDY **Capture Data Ready**

This bit indicates that the Capture I/O Data Register (R3) contains data ready for the host to read. This bit is used for direct programmed I/O data transfers only.

"1" : data is new. Ready for the next host data read

"0" : data is old. Do not re-read the information

SER **Sample Error**

This bit indicates that a playback underrun or a capture overrun has occurred. If both playback and capture are enabled, the capture overrun (CO) and playback underrun (PU) bits of the Alternate Feature Status Register (I24) will indicate the exact source of the error that set this bit.

"1" : sample was not serviced in time and an error occurred

"0" : default value upon power up

PU/L* **Playback Upper / Lower Byte**

"1" : the playback data needed is for the upper byte, or any 8-bit mode

"0" : the playback data needed is for the lower byte

PL/R* **Playback Left / Right Sample**

"1" : the playback data needed is for the left channel

"0" : the playback data needed is for the right channel

PRDY **Playback Data Ready**

This bit indicates that the Playback I/O Data Register (R3) is ready for more data. This bit is used for direct programmed I/O data transfers only.

"1" : data is old. Ready for the next data write value from the host.

"0" : data is still valid. Do not overwrite.

INT **Interrupt Status**

This bit indicates the status of the internal interrupt logic of CH6357. Although the Status Register (R2) is a read only, writing any value to this register will clear the INT bit. The IEN bit of the Pin Control register (I10) determines whether the state of this bit is reflected on the IRQ pin of CH6357.

"1" : interrupt active

"0" : interrupt inactive

Programmed I/O Data Registers (R3)

The PIO data registers are two registers mapped into the same address:

- Capture I/O Data register
- Playback I/O Data register

Reading from the PIO data register will receive data from the capture data register, while writing to it will send data to the playback data register. During initialization and power down, this register **CANNOT** receive any writes and it will return 1000 0000 (80H) for all reads by the host computer.

Capture I/O Data Register (R3, Read Only)

D7	D6	D5	D4	D3	D2	D1	D0
CD7	CD6	CD5	CD4	CD3	CD2	CD1	CD0

CD7 - CD0 **Capture Data Port**

This register is where capture data is read during programmed I/O data transfers.

Assuming a new sample is available, the reading of this register will increment the state machine so that the following read will be from the next appropriate byte in the sample. The exact byte which is next to be read can be determined by reading the Status Register (R2). Once all relevant bytes have been read, the state machine will point to the last byte of the sample until a new sample is received from the ADCs. The state machine and Status Register (R2) will then point to the first byte of the new sample.

Playback I/O Data Register (R3, Write Only)

D7	D6	D5	D4	D3	D2	D1	D0
PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

PD7 - PD0 **Playback Data Port**

This register is where Playback data is written during programmed I/O data transfers.

Writing data to this register will increment the playback byte tracking state machine so that the following write will be to the correct byte of the sample. Once all bytes of a sample have been written and the FIFO is full, subsequent byte writes to this port are ignored. The state machine is reset when the current sample is sent to the DACs.

Indirect Registers Descriptions

The following indirect registers are accessed by writing the appropriate values to the Index Address Register (R0) and then accessing the Indexed Data Register (R1). Note that indirect registers 16 – 31 are available in MODE 2 only.

Left ADC Input Control (I0)

D7	D6	D5	D4	D3	D2	D1	D0
LSS1	LSS0	LMGE	res	LAG3	LAG2	LAG1	LAG0

The initial value of this register upon power up is 000x 0000. The reserved bit should be written zero and may be 0 or 1 when read.

LSS1 - LSS0 **Left ADC Input Select**

These bits select the input source for the left ADC channel

LSS1	LSS0	SOURCE
0	0	Selects LLINE (Left LINE Input)
0	1	Selects LAUX1 (Left Auxiliary #1)
1	0	Selects LMIC (Left Microphone)
1	1	Selects Left LINE Output Loopback

LMGE **Left MIC Gain Enable**

This bit enables the +20 dB gain stage of the LMIC (Left Microphone input signal).

LAG3 - LAG0 **Left ADC Gain**

These four bits select the amount of gain for the left ADC. The gain can be controlled from 0 dB to 22.5 dB in 1.5 dB steps. For details, please refer to **Table 11** below.

Right ADC Input Control (I1)

D7	D6	D5	D4	D3	D2	D1	D0
RSS1	RSS0	RMGE	res	RAG3	RAG2	RAG1	RAG0

The initial value of this register upon power up is 000x 0000. The reserved bit should be written zero and may be 0 or 1 when read.

Table 11 • ADC Input Gain

AG3	AG2	AG1	AG0	Level(dB)
0	0	0	0	0.0
0	0	0	1	1.5
0	0	1	0	3.0
0	0	1	1	4.5
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.
1	1	0	0	18.0
1	1	0	1	19.5
1	1	1	0	21.0
1	1	1	1	22.5

RSS1 - RSS0 **Right ADC Input Select**

These bits select the input source for the right ADC channel.

RSS1	RSSO	SOURCE
0	0	Selects RLINE (Right LINE Input)
0	1	Selects RAUX1 (Right Auxiliary #1)
1	0	Selects RMIC (Right Microphone)
1	1	Selects Right Line Output Loopback

RMGE **Right MIC Gain Enable**

This bit enables the +20 dB gain stage of the RMIC (Right Microphone input signal).

RAG3 - RAG0 **Right ADC Gain**

These four bits select the amount of gain for the right ADC. The gain can be controlled from 0 dB to 22.5 dB in 1.5 dB steps. For details, please refer to **Table 11**.

Left Auxiliary #1 Input Control (I2)

D7	D6	D5	D4	D3	D2	D1	D0
LX1M	res	res	LX1G4	LX1G3	LX1G2	LX1G1	LX1G0

The initial value of this register upon power up is 1xx0 1000. All reserved bits should be written zero and may be 0 or 1 when read.

LX1M **Left Auxiliary #1 Mute Control (LAUX1)**

"1" : LAUX1 input to the mixer is muted

"0" : LAUX1 input to the mixer is passed through (not muted)

LX1G4 - LX1G0 **Left Auxiliary #1 Mix Gain (LAUX1)**

These five bits select the mix gain for the left AUX #1 input signal. The gain can be controlled from -34.5 dB to 12 dB in 1.5 dB steps. For more details, please refer to **Table 12** on page 2-41 for more details.

Right Auxiliary #1 Input Control (I3)

D7	D6	D5	D4	D3	D2	D1	D0
RX1M	res	res	RX1G4	RX1G3	RX1G2	RX1G1	RX1G0

The initial value of this register upon power up is 1xx0 1000. All reserved bits should be written zero and may be 0 or 1 when read.

RX1M **Right Auxiliary #1 Mute Control (RAUX1)**

"1" : RAUX1 input to the mixer is muted

"0" : RAUX1 input to the mixer is passed through (not muted)

RX1G4 - RX1F0 **Right Auxiliary #1 Mix Gain (RAUX1)**

These five bits select the mix gain for the right AUX #1 input signal. The gain can be controlled from -34.5 dB to 12 dB in 1.5 dB steps. For more details, please refer to **Table 12** on page 2-41 for more details.

Left Auxiliary #2 Input Control (I4)

D7	D6	D5	D4	D3	D2	D1	D0
LX2M	res	res	LX2G4	LX2G3	LX2G2	LX2G1	LX2G0

The initial value of this register upon power up is 1xx0 1000. All reserved bits should be written zero and may be 0 or 1 when read.

LX2M **Left Auxiliary #2 Mute Control (LAUX2)**

"1" : LAUX2 input to the mixer is muted

"0" : LAUX2 input to the mixer is passed through (not muted)

LX2G4 - LX2G0 **Left Auxiliary #2 Mix Gain (LAUX2)**

These five bits select the mix gain for the left AUX #2 input signal. The gain can be controlled from -34.5 dB to 12 dB in 1.5 dB steps. For more details, please refer to **Table 12** on page 2-41 for more details.

Right Auxiliary #2 Input Control (I5)

D7	D6	D5	D4	D3	D2	D1	D0
RX2M	res	res	RX2G4	RX2G3	RX2G2	RX2G1	RX2G0

The initial value of this register upon power up is 1xx0 1000. All reserved bits should be written zero and may be 0 or 1 when read.

RX2M **Right Auxiliary #2 Mute Control (RAUX2)**

"1" : RAUX2 input to the mixer is muted

"0" : RAUX2 input to the mixer is passed through (not muted)

RX2G4 - RX2G0 **Right Auxiliary #2 Mix Gain (RAUX2)**

These five bits select the mix gain for the right AUX #2 input signal. The gain can be controlled from -34.5 dB to 12 dB in 1.5 dB steps. For more details, please refer to **Table 12** below.

Table 12 • AUX1, AUX2 & Line Mixer Gain

	G4	G3	G2	G1	G0	Level (dB)
0	0	0	0	0	0	12.0
1	0	0	0	0	1	10.5
2	0	0	0	1	0	9.0
3	0	0	0	1	1	7.5
4	0	0	1	0	0	6.0
5	0	0	1	0	1	4.5
6	0	0	1	1	0	3.0
7	0	0	1	1	1	1.5
8	0	1	0	0	0	0.0
9	0	1	0	0	1	-1.5
10	0	1	0	1	0	-3.0
11	0	1	0	1	1	-4.5
12	0	1	1	0	0	-6.0
13	0	1	1	0	1	-7.5
14	0	1	1	1	0	-9.0
15	0	1	1	1	1	-10.5
16	1	0	0	0	0	-12.0
17	1	0	0	0	1	-13.5
18	1	0	0	1	0	-15.0
19	1	0	0	1	1	-16.5
20	1	0	1	0	0	-18.0
21	1	0	1	0	1	-19.5
22	1	0	1	1	0	-21.0
23	1	0	1	1	1	-22.5
24	1	1	0	0	0	-24.0
25	1	1	0	0	1	-25.5
26	1	1	0	1	0	-27.0
27	1	1	0	1	1	-28.5
28	1	1	1	0	0	-30.0
29	1	1	1	0	1	-31.5
30	1	1	1	1	0	-33.0
31	1	1	1	1	1	-34.5

Note: Output level relative to input level assuming OLB = 1
If OLB = 1, the output will reflect the gain setting
If OLB = 0, the output will be attenuated by 3 dB

Left DAC Output Control (I6)

D7	D6	D5	D4	D3	D2	D1	D0
LDM	res	LDA5	LDA4	LDA3	LDA2	LDA1	LDA0

The initial value of this register upon power up is 1x00 0000. All reserved bits should be written zero and may be 0 or 1 when read.

LDM **Left DAC Mute Control**

"1" : Left DAC output to the mixer is muted

"0" : Left DAC output to the mixer is passed through (not muted)

LDA5 - LDA0 **Left DAC Attenuator Control**

These six bits select the amount of attenuation applied to the left DAC. The amount of attenuation can be controlled from -94.5 dB to 0 dB in 1.5 dB steps. For more details, please refer to **Table 13** below.

Right DAC Output Control (I7)

D7	D6	D5	D4	D3	D2	D1	D0
RDM	res	RDA5	RDA4	RDA3	RDA2	RDA1	RDA0

The initial value of this register upon power up is 1x00 0000. The reserved bit should be written zero and may be 0 or 1 when read.

RDM **Right DAC Mute Control**

"1" : Right DAC output to the mixer is muted

"0" : Right DAC output to the mixer is passed through (not muted)

RDA5 - RDA0 **Right DAC Attenuator Control**

These six bits select the amount of attenuation applied to the right DAC. The amount of attenuation can be controlled from -94.5 dB to 0 dB in 1.5 dB steps. For more details, please refer to **Table 13** below.

Table 13 • DAC and Loopback Attenuation

	A5	A4	A3	A2	A1	A0	Level (dB)
0	0	0	0	0	0	0	0.0
1	0	0	0	0	0	1	-1.5
2	0	0	0	0	1	0	-3.0
3	0	0	0	0	1	1	-4.5
4	0	0	0	1	0	0	-6.0
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
60	1	1	1	1	0	0	-90.0
61	1	1	1	1	0	1	-91.5
62	1	1	1	1	1	0	-93.0
63	1	1	1	1	1	1	-94.5

Note: Output level relative to input level assuming OLB = 1
If OLB = 1, the output will reflect the gain setting
If OLB = 0, the output will be attenuated by 3 dB

Fs and Playback Data Format (I8)

D7	D6	D5	D4	D3	D2	D1	D0
FMT1	FMT0	C/L*	S/M*	CSF2	CSF1	CSF0	C2SL

The initial value of this register upon power up is 0000 0000.

Note *The mode change enable (MCE) bit in index address register (R0) must be asserted high before the contents of this register can be modified. FMT[1:0], C/L*, and S/M* can be independently modified if the playback mode change enable bit (PMCE) in index register I16 is asserted.*

FMT1 - FMT0 **Format Select**

These bits along with C/L* bit select the audio data format.

MODE 1:FMT0 and C/L* bits are used for selecting the audio data format for both the playback and capture operations. In this mode, FMT1 is not available and is forced to logic "0."

MODE 2:FMT1, FMT0 and C/L* bits are dedicated for selecting the audio data format for the playback ONLY. The capture data format is selected independently through the Capture Data Format register (I28).

C/L* **Companded or Linear Select**

This bit along with FMT0 and FMT1 (FMT1 is only available in MODE 2), selects the audio data format. The following table shows the audio data formats available in both modes.

MODE 2

FMT1	FMT0	C/L*	Audio Data Format
0	0	0	Linear, 8-bit unsigned
0	0	1	μ-Law, 8-bit companded
0	1	0	Linear, 16-bit two's complement, Little Endian
0	1	1	A-Law, 8-bit companded
1	0	0	RESERVED
1	0	1	ADPCM, 4-bit, IMA compatible
1	1	0	Linear, 16-bit two's complement, Big Endian
1	1	1	RESERVED

MODE 1

FMT0	C/L*	Audio Data Format
0	0	Linear, 8-bit unsigned
0	1	μ-Law, 8-bit companded
1	0	Linear, 16-bit two's complement, Little Endian
1	1	A-Law, 8-bit companded

S/M* **Stereo / Mono Select**

MODE 1:This bit is used for both playback and capture

MODE 2:This bit is used for playback ONLY. The capture data format is selected independently through the Capture Data Format register (I28).

"1" : Selects stereo data format. Stereo format alternates samples to represent the left and right audio channels.

"0" : Selects mono data format. Mono playback format plays the same audio sample on both channels. Mono capture format captures audio data from the left channel.

CSF2 - CSF0 **Clock Frequency Divisor Select**

These three bits select the audio sampling frequency for both playback and capture. The table below lists the sampling frequencies for X1 = 24.576 MHz and X2 = 16.9344 MHz crystal clock sources. As the table implies, the actual sampling frequency depends on which crystal source is selected.

Frequencies listed with N/A are not available because they violate the maximum sampling frequency specified; however, the decodes may still be used for crystals that produce sampling frequencies falling within specifications.

CSF2	CSF1	CSF0	Divisor	X1 = 24.576 MHz	X2 = 16.9344 MHz
0	0	0	3072	8.0 kHz	5.51 kHz †
0	0	1	1536	16.0 kHz	11.025 kHz †
0	1	0	896	27.42 kHz	18.9 kHz
0	1	1	768	32.0 kHz	22.05 kHz †
1	0	0	448	N/A	37.8 kHz
1	0	1	384	N/A	44.1 kHz †
1	1	0	512	48.0 kHz	33.075 kHz
1	1	1	2560	9.6 kHz	6.62 kHz

Note: † The following frequencies are supported when SIE (serial interface enable) and RCE (rate change enable) register bits of index registers I16 and I28, respectively, are high. For additional information, please refer to the respective index registers and the **Digital Audio Serial Interface** section on page 2-19.

C2SL **Clock 2 Source Select**

This bit selects which crystal clock source will be used for deriving the audio sampling frequency for both playback and capture.

"1" : Selects X2 (Crystal #2) with a typical value of 16.9344 MHz
"0" : Selects X1 (Crystal #1) with a typical value of 24.576 MHz

Interface Configuration (I9)

D7	D6	D5	D4	D3	D2	D1	D0
CPIO	PPIO	res	res	ACAL	SDC	CEN	PEN

The initial value of this register upon power up is 00x0 1000. All reserved bits should be written zero and may be 0 or 1 when read.

Note *Except for the CEN and PEN bits, the MCE bit must be asserted before any changes to these register bits can occur.*

CPIO **Capture PIO Enable**

"1" : Capture data is transferred via PIO

"0" : Capture data is transferred via DMA

PPIO **Playback PIO Enable**

"1" : Playback data is transferred via PIO

"0" : Playback data is transferred via DMA

ACAL **Auto-Calibrate Enable**

This bit selects whether CH6357 will calibrate the ADCs whenever the MCE (Mode Change Enable) bit changes from 1 to 0. This bit is always set high by default upon power up.

"1" : Auto-calibration is enabled

"0" : Auto-calibration is disabled. Previous calibration values are used

SDC **Single DMA Channel**

"1" : Single DMA Channel Mode

This bit forces BOTH playback and capture DMA requests to occur on the playback DMA channel. Capture DMA requests and acknowledges now occur, respectively, in the PDRQ and the PDAK* pins. The capture CDRQ pin, however, is forced low. If playback and capture are enabled simultaneously, playback mode will occur by default. See the DMA Interface section for more information.

"0" : Dual DMA Channel Mode (in MODE 2 only)

CEN **Capture Enable**

Writes to this bit can be performed without the assertion of the MCE bit.

"1" : Capture is enabled

DMA capture mode is enabled if:
CEN = 1 & CPIO = 0

Programmed I/O capture mode is enabled if:
CEN = 1 & CPIO = 1

"0" : Capture is disabled (CDRQ and PIO are inactive)

PEN **Playback Enable**

Writes to this bit can be performed without the assertion of the MCE bit.

"1" : Playback is enabled

DMA playback mode is enabled if:
PEN = 1 & PPIO = 0

Programmed I/O playback mode is enabled if:
PEN = 1 & PPIO = 1

"0" : Playback is disabled (PDRQ and PIO are inactive)

Pin Control (I10)

D7	D6	D5	D4	D3	D2	D1	D0
XCTL1	XCTL0	res	res	DEN	res	IEN	res

The initial value of this register upon power up is 00xx 0x0x. All reserved bits should be written zero and may be 0 or 1 when read.

XCLT1 - XCTL0 **External Control Bits**

"1" : TTL logic high is reflected to the respective XCTL1 & XCTL0 pins

"0" : TTL logic low is reflected to the respective XCTL1 & XCTL0 pins

DEN **Dither Enable**

This bit applies only to the 8-bit unsigned mode.

"1" : Dither is disabled

"0" : Dither is enabled . Triangular pdf dither is added before truncating the ADC 16-bit value to 8-bit unsigned data.

IEN **Interrupt Enable**

"1" : Interrupt pin is enabled. The interrupt pin IRQ will reflect the value of the INT bit of the Status register (R2). Interrupts invoke active high signals.

"0" : Interrupt pin is disabled

Error Status and Initialization (I11, Read Only)

D7	D6	D5	D4	D3	D2	D1	D0
COR	PUR	ACI	DRS	ORR1	ORR0	ORL1	ORL0

The initial value of this register upon power up is 0000 0000.

COR **Capture Overrun**

"1" : Capture overrun condition occurred. This bit indicates that the host has failed to read the capture data from CH6357 before the next sample arrived. The new sample will be ignored and the old sample will not be overwritten. This bit will reset once the Status register (R2) is read.

"0" : No error condition detected

PUR **Playback Under-run**

"1" : Playback underrun condition occurred. This bit indicates that the host has failed to supply playback data to CH6357 in time for it to be played. If DACZ=0, the last valid sample will be held and remain input to the DACs until the next sample arrives. If DACZ=1, the input to the DACs will be set to zero (mid-scale). This bit will reset once the Status register (R2) is read. For information on the DACZ register bit, please refer to the Alternate Feature Enable I register on page 2-49.

"0" : No error condition detected

The SER bit in the Status Register (R2) is a logical OR of the COR and PUR bits. This allows a polling host CPU to detect an error condition while checking other status bits.

ACI **Auto-Calibrate In Progress**

"1" : Auto-calibration is in progress

"0" : No auto-calibration is in progress

Error Status and Initialization (I11, Read Only) (continued)

DRS **DMA Request Status**

"1" : PDRQ (Playback DMA Request) **OR** CDRQ (Capture DMA Request) is currently active

"0" : PDRQ (Playback DMA Request) **AND** CDRQ (Capture DMA Request) are presently inactive

ORR1 - ORR0 **Overrange Right Detect**

These bits determine the over-range on the right ADC channel. They are updated on a sample-by-sample basis.

00	Less than -1.5 dB
01	Between -1.5 dB and 0 dB
10	Between 0 dB and +1.5 dB
11	Greater than +1.5 dB

ORL1 - ORL0 **Overrange Left Detect**

These bits determine the over-range on the left ADC channel. They are updated on a sample-by-sample basis.

00	Less than -1.5 dB
01	Between -1.5 dB and 0 dB
10	Between 0 dB and +1.5 dB
11	Greater than +1.5 dB

MODE and ID (I12)

D7	D6	D5	D4	D3	D2	D1	D0
1	MODE2	res	res	ID3	ID2	ID1	ID0

The initial value of this register upon power up is 10xx 1010. All reserved bits should be written zero and may be 0 or 1 when read.

MODE2 **Select Mode 2**

This bit enables access to indirect registers 16 – 31 and their associated features.

"1" : Selects MODE 2 : Features compatible to **CS4231**

"0" : Selects MODE 1 : Features compatible to **AD1848** & **CS4248**

ID3 - ID0 **CODEC Identification Number**

These four bits specify the ID and initial revisions of the codec. Further revisions are expanded in Indirect register I25 on page 2-56.

"1010" : ID compatibe to CS4231

Loopback Control (I13)

D7	D6	D5	D4	D3	D2	D1	D0
LBA5	LBA4	LBA3	LBA2	LBA1	LBA0	res	LBE

The initial value of this register upon power up is 0000 00x0. The reserved bit should be written zero and may be 0 or 1 when read.

LBA5 - LBA0 **Loopback Attenuation**

These bits selects the amount of attenuation applied to the loopback from ADC to DAC. The amount of attenuation can be controlled from -94.5 dB to 0 dB in 1.5 dB steps. For more information, please refer to **Table 13** on page 2-42 .

LBE **Loopback Enable**

"1" : Loopback is enabled. The ADC data is digitally mixed with the data sent to DAC.

"0" : Loopback is disabled

Playback Upper Base Count (I14)

D7	D6	D5	D4	D3	D2	D1	D0
PUB7	PUB6	PUB5	PUB4	PUB3	PUB2	PUB1	PUB0

The initial value of this register upon power up is 0000 0000.

PUB7 - PUB0 **Playback Upper Base**

This register represents the 8 most significant bits of the 16-bit playback base register. Reading from it returns the same value in which it was written. The current count registers cannot be read. When MODE 1 or SDC (Single DMA Channel) is selected, this register is used for both playback and capture base registers.

A write to the Playback Upper Base register will load the value in both base registers to the current count register. Therefore, in order to load the count value correctly, the lower count value must be first written into the Lower Base Count register and then followed by the count value's upper byte written into the Upper Base Count register.

Playback Lower Base Count (I15)

D7	D6	D5	D4	D3	D2	D1	D0
PLB7	PLB6	PLB5	PLB4	PLB3	PLB2	PLB1	PLB0

The initial value of this register upon power up is 0000 0000.

PLB7 - PLB0 **Playback Lower Base**

This register represents the 8 least significant bits of the 16-bit playback base register. Reading from it returns the same value in which it was written. When MODE 1 or SDC (Single DMA Channel) is selected, this register is used for both playback and capture base registers.

The following Indirect registers (I16 through I31) are available in MODE 2 ONLY

Alternate Feature Enable I (I16)

D7	D6	D5	D4	D3	D2	D1	D0
OLB	TE	CMCE	PMCE	SFSL1	SFSL0	SIE	DACZ

The initial value of this register upon power up is 0000 0000. All reserved bits should be written zero and may be 0 or 1 when read.

***Note** Changes to CMCE, and PMCE can only occur when CH6357 is in Chrontel programming mode. Changes to SIE and SFSL[1:0] can only occur when the CH6357 is in Chrontel programming mode and when the MCE bit set.*

OLB **Analog Output Level Bit**

This bit selects the analog output level.

"1" : Full scale of 2.8 Vpp (0 dB)
"0" : Full scale of 2 Vpp (-3 dB)

TE **Timer Enable**

"1" : Timer is enabled to run and interrupt the host at a specified frequency in the timer registers
"0" : Timer is disabled

CMCE **Capture Mode Change Enable**

"1" : Allows modification to the four most significant bits (D7-D4) of the Capture Data Format register I28 without asserting MCE.
"0" : Changes to bits (D7-D4) of the Capture Data Format register I28 without the assertion of MCE is not allowed.

PMCE **Playback Mode Change Enable**

"1" : Allows modification to the four most significant bits (D7-D4) of the Fs and Playback Data Format register I8 without asserting MCE.
"0" : Changes to bits (D7-D4) of the Playback Data Format register I8 without the assertion of MCE is not allowed.

SFSL1 - SFSL0 **Serial Format Select**

These bits select the format of the serial port when the serial interface is enabled.

SFSL1	SFSL0	Serial Data Format
0	0	Format 1: Right justified, 48 bit clock
0	1	Format 2: Right justified, 64 bit clock
1	0	Format 3: Reserved
1	1	Format 4: Reserved

Please refer to **Figures 13** and **14** on page 2-21 for timing information on these formats

SIE **Serial Interface Enable**

"1" : Enables the Serial Interface for digital audio data
"0" : Disables the Serial Interface

DACZ **DAC Zero**

This bit selects the action taken whenever an underrun error occurs.

"1" : The output to the DACs is set to the mid-scale
"0" : The last valid sample will be continuously outputted to the DACs

Alternate Feature Enable II (I17)

D7	D6	D5	D4	D3	D2	D1	D0
TEST	DGRST	TEST	TEST	res	res	XTALE	HPF

The initial value of this register upon power up is 0000 xx00. All reserved bits should be written zero and may be 0 or 1 when read.

Note *Changes to DGRST and XTALE register bits can only occur when the CH6357 is in Chrontel programming mode.*

TEST **Test bits**

These bits are for internal use only. Reading or writing to these bits is prohibited.

DGRST **Digital Reset**

"1" : Resets all direct and indirect registers to their default values.

"0" : normal operation

HPF **High Pass Filter**

"1" : Enables a DC-blocking high-pass filter in the digital filter of the ADCs. This filter eliminates the ADC offset.

"0" : Disables the DC-blocking high-pass filter in the digital filter of the ADCs.

XTALE **Crystal Enable**

"1" : Enables both crystal oscillators to be active.

"0" : Allows one crystal oscillator to be active at one time

Note that in order to minimize the start-up time when switching between crystal clock sources, the crystal enable bit could be set high.

Left Line Input Control (I18)

D7	D6	D5	D4	D3	D2	D1	D0
LLM	res	res	LLG4	LLG3	LLG2	LLG1	LLG0

The initial value of this register upon power up is 1xx0 1000. All reserved bits should be written zero and may be 0 or 1 when read.

LLM **Left Line Mute Control (LLINE)**

"1" : Left Line Input (LLINE) to the mixer is muted

"0" : Left Line Input (LLINE) to the mixer is passed through (not muted)

LLG4 - LLG0 **Left Line Mix Gain (LLINE)**

These five bits select the mix gain applied to the left LINE input signal. The gain can be controlled from -34.5 dB to 12 dB in 1.5 dB steps. For more details, please refer to **Table 12** on page 2-41.

Right Line Input Control (I19)

D7	D6	D5	D4	D3	D2	D1	D0
RLM	res	res	RLG4	RLG3	RLG2	RLG1	RLG0

The initial value of this register upon power up is 1xx0 1000. All reserved bits should be written zero and may be 0 or 1 when read.

RLM **Right Line Mute Control (RLINE)**

"1" : Right Line Input (RLINE) to the mixer is muted

"0" : Right Line Input (RLINE) to the mixer is passed through (not muted)

RLG4 - RLG0 **Right Line Mix Gain (RLINE)**

These five bits select the mix gain applied to the right Line input signal. The gain can be controlled from -34.5 dB to 12 dB in 1.5 dB steps. For more details, please refer to **Table 12** on page 2-41.

Timer Lower Byte (I20)

D7	D6	D5	D4	D3	D2	D1	D0
TL7	TL6	TL5	TL4	TL3	TL2	TL1	TL0

The initial value of this register upon power up is 0000 0000.

TL7 - TL0 **Lower Bits for Timer**

This register represents the low order byte of the 16-bit timer. The time base is determined by the crystal clock source selected. Additional detail is provided below, under the Timer Upper byte Register section.

A write to the Timer Lower Byte register will load the value in both timer registers to the current count register. Therefore, in order to load the count value correctly, the upper count value must be first written into the Timer Upper Byte register and then followed by the count value's lower byte written into theTimer Lower Byte register.

Timer Upper Byte (I21)

D7	D6	D5	D4	D3	D2	D1	D0
TU7	TU6	TU5	TU4	TU3	TU2	TU1	TU0

The initial value of this register upon power up is 0000 0000.

TU7 - TU0 **Upper Bits for Timer**

This register represents the high order byte of the 16-bit timer. Depending on which clock source is selected, the time base† or count period is as follows:

When C2SL = 0:XTAL1 = 24.576 MHz is divided by 245
Time base = 9.969 µsec

When C2SL = 1:XTAL2 = 16.9344 MHz is divided by 168
Time base = 9.92 µsec

† *Time base refers to the time it will take the internal current count register to perform a single decrement (count down).*

Left Serial Input Control (I22)

D7	D6	D5	D4	D3	D2	D1	D0
LSIM	res	res	LSIA4	LSIA3	LSIA2	LSIA1	LSIA0

The initial value of this register upon power up is 1000 0000. All reserved bits should be written zero and may be 0 or 1 when read.

Note *Changes to these register bits can only occur when CH6357 is in Chrontel programming mode.*

LSIM **Left Serial Input Mute**

"1" : Left Serial Digital Input is muted
"0" : Left Serial Digital Input is passed through (not muted)

LSIA4 - LSIA0 **Left Serial Input Attenuation Control**

These bits select the amount of attenuation applied to the left channel serial digital input. For more details, please refer to **Table 14** on page 2-54.

Alternate Feature Status (I24)

D7	D6	D5	D4	D3	D2	D1	D0
res	TI	CI	PI	CU	CO	PO	PU

The initial value of this register upon power up is x000 0000. The reserved bit should be written zero and may be 0 or 1 when read.

TI **Timer Interrupt**

"1" : An interrupt is pending from the timer current count registers

"0" : No interrupt

CI **Capture Interrupt**

"1" : An interrupt is pending from the record DMA current count registers

"0" : No capture interrupt

PI **Playback Interrupt**

"1" : An interrupt is pending from the playback DMA current count registers

"0" : No playback interrupt

The PI, CI, and TI bits are reset by clearing the respective interrupt bit or by performing a write of any value to the Status register (R2).

CU **Capture Underrun**

"1" : Capture underrun error has occurred. The host has read more data out of the FIFO than the FIFO contained. The last valid byte is read by the host

"0" : No underrun error

CO **Capture Overrun**

"1" : Capture overrun error has occurred. The FIFO is full and has no room to load the sample coming from the ADC. The new sample will be discarded.

"0" : No overrun error

PO **Playback Overrun**

"1" : Playback overrun error occurred. The host attempts to write data into a full FIFO. The FIFO could not be overwritten so the new data is discarded.

"0" : No overrun error

PU **Playback Underrun**

"1" : Playback underrun error has occurred. This indicates that a sample was missed and that the DAC has run out of data.

"0" : No underrun error

Version and ID (I25)

D7	D6	D5	D4	D3	D2	D1	D0
V2	V1	V0	res	res	CID2	CID1	CID0

The initial value of this register upon power up is 100x x000. All reserved bits should be written zero and may be 0 or 1 when read.

V2 - V0 **Version Number**

"100" : Revision C, D, and E of CS4231-compatible codec

CID2 - CID0 **Chip Identification Number**

"000" : CS4231-compatible codec

Mono Input and Output Control (I26)

D7	D6	D5	D4	D3	D2	D1	D0
MIM	MOM	res	res	MIA3	MIA2	MIA1	MIA0

The initial value of this register upon power up is 00xx 0011. All reserved bits should be written zero and may be 0 or 1 when read.

MIM **Mono Input Mute Control**

"1" : Enables the mute control on the mono input (MIN). The mono input provides mix for the "beeper" function in most computers.

"0" : Disables the mute control

MOM **Mono Output Mute Control**

"1" : Enables the mute control on the mono output (MOUT). The mute control is independent of the Line Output (LOUT) mute.

"0" : Disables the mute control

MIA3 - MIA0 **Mono Input Attenuation Control**

These four bits select the amount of attenuation applied to the mono input signal. The amount of attenuation can be controlled from -45 dB to 0 dB in 3 dB steps. For more details, please refer to **Table 15** below.

Table 15 • Mono Mixer Attenuation.

MIA3	MIA2	MIA1	MIA0	Level(dB)
0	0	0	0	0.0
0	0	0	1	-3.0
0	0	1	0	-6.0
0	0	1	1	-9.0
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.
1	1	0	0	-36.0
1	1	0	1	-39.0
1	1	1	0	-42.0
1	1	1	1	-45.0

Note: Output level relative to input level assuming OLB = 1
If OLB = 1, the output will reflect the gain setting
If OLB = 0, the output will be attenuated by 3 dB

Alternate Feature Enable III (I27)

D7	D6	D5	D4	D3	D2	D1	D0
SOM	SOSL	ATM	SIGS	MXGS2	MXGS1	MXGS0	CTMODE

The initial value of this register upon power up is 1000 0000.

Note *Except for the register bit CTMODE, changes to these register bits can only occur when CH6357 is in Chrontel programming mode.*

SOM **Serial Output Mute**

"1" : Serial Digital Output (SDOUT pin) is muted

"0" : Serial Digital Output (SDOUT pin) is passed through (not muted)

SOSL **Serial Output Source Select**

"1" : Capture data is output to SDOUT pin

"0" : Playback data is output to SDOUT pin

ATM **AT Bus Input Mute**

"1" : AT bus input to DAC is muted

"0" : AT bus input is passed through (not muted)

SIGS **Serial Input Mix Gain Scaling**

"1" : Input from the parallel bus and from the serial input are halved

"0" : No serial input mix gain scaling

MXGS2 - MXGS0 **Mixer Gain-Scaling**

These bits select the gain-scaling applied to the inputs of the analog mixer. Upon power-up, the mixer gain-scaling is set to one (i.e., G=1).

MXGS2	MXGS1	MXGS0	G = Mixer Gain Scaling
0	0	0	1
0	0	1	1/2
0	1	0	1/3
0	1	1	1/4
1	0	0	1/5
1	1	1	Automatic

where: $Automatic = \frac{1}{total\ \#\ of\ inputs\ applied\ to\ the\ mixer}$

Automatic mode allows CH6357 to detect the number of inputs to the analog mixer and apply the corresponding gain scaling necessary to avoid clipping.

In addition to the gain scaling applied to the inputs of the analog mixer, the definition of the analog output level bit (OLB) in index register I16 will result to an *overall analog mixer gain-scaling* defined as follows:

$$Overall\ Mixer\ Gain\text{-}Scaling = \begin{cases} G, & if\ OLB = 1 \\ G \div (1.4), & if\ OLB = 0 \end{cases}$$

Alternate Features Enable III (I27) (continued)

CTMODE ***CHRONTEL* Mode (Read Only)**

"1" : Indicates CH6357 is currently in Chrontel programming mode.

"0" : Indicates CH6357 is **NOT** in Chrontel programming mode.

Note *To enter or exit Chrontel mode, read the contents of index register I25 and write the content's bit-wise negation back to index register I25. For example, if 0X80H is read from I25, 0X7FH must be written back to I25 to exit or enter Chrontel mode.*

Capture Data Format (I28)

D7	D6	D5	D4	D3	D2	D1	D0
FMT1	FMT0	C/L*	S/M*	res	res	res	RCE

The initial value of this register upon power up is 0000 xxxx. All reserved bits should be written zero and may be 0 or 1 when read.

Note *The mode change enable (MCE) bit in index address register (R0) must be asserted high before contents of this register can be modified. FMT[1:0], C/L*, and S/M* can be independently modified if the capture mode change enable bit (CMCE) in index register I16 is asserted.*

FMT1 - FMT0 **Format Select**

These bits along with C/L* bit select the capture audio data format in **MODE 2 ONLY**. See the table below for bit setting and audio data formats.

The capture data format can vary from the Playback data format; however, the sample frequencies must be the same as set in the Indirect Register (I8).

C/L* **Companded or Linear Select**

This bit, along with FMT0 and FMT1, selects the audio data format. The table below shows the audio data formats available.

FMT1	FMT0	C/L*	Audio Data Format
0	0	0	Linear, 8-bit unsigned
0	0	1	μ-Law, 8-bit companded
0	1	0	Linear, 16-bit two's complement, Little Endian
0	1	1	A-Law, 8-bit companded
1	0	0	RESERVED
1	0	1	ADPCM, 4-bit, IMA compatible
1	1	0	Linear, 16-bit two's complement, Big Endian
1	1	1	RESERVED

S/M* **Stereo / Mono Select.**

This bit is for Capture audio data format.

"1" : Stereo data format is selected. Stereo format alternates samples to represent the left and right audio channels.

"0" : Mono data format is selected. Mono capture format captures audio data from the left channel.

Capture Data Format (I28) (continued)

RCE **Rate Conversion Enable**

"1" : Enables the CH6357's interpolator and decimator blocks, and shifts the ADCs and DACs sampling frequencies to 44.1 kHz. For additional information, please refer to **Digital Audio Serial Interface** on page 2-19.

"0" : Data rate conversion inactive

Note *Changes to RCE can only occur when CH6357 is in Chrontel programming mode.*

2

ID and FIFO Control Register (I29)

D7	D6	D5	D4	D3	D2	D1	D0
CTID2	CTID1	CTID0	CTIV1	CTIV0	BDBUD	FT1	FT0

The initial value of this register upon power up is 0000 0000. All reserved bits should be written zero and may be 0 or 1 when read.

Note *Changes to BDBUD and FT[1:0] register bits can only occur when CH6357 is in Chrontel programming mode.*

CTID2 - CTID0 **Chrontel Identification Number**

This number distinguishes between this chip and future chips that will support this register set.

"000" : Chrontel CH6357

CTIV1 - CTIV0 **Chrontel Version Number**

The version number is changed whenever enhancements to the CH6357 are made. This number would distinguish between different versions of the CH6357.

"00" : Revision A

BDBUD **Bus Data Burst Until Done**

"1" : Enables multiple sample transfers per DMA request

"0" : Default DMA transfer mode

FT1 - FT0 **FIFO Threshold for Capture and Playback Request Control**

These bits select the condition under which DMA requests are generated from the FIFOs.

FT1	FT0	Capture FIFO Threshold	Playback FIFO Threshold
0	0	FIFO is 1-sample full	FIFO is 1-sample empty
0	1	25% of FIFO is full	25% of FIFO empty
1	0	50% of FIFO is full	50% of FIFO empty
1	1	75% of FIFO is full	75% of FIFO empty

Capture Upper Base Count (I30)

D7	D6	D5	D4	D3	D2	D1	D0
CUB7	CUB6	CUB5	CUB4	CUB3	CUB2	CUB1	CUB0

The initial value of this register upon power up is 0000 0000.

CUB7 - CUB0 **Capture Upper Base**

This register represents the 8 most significant bits of the 16-bit capture base register. Reading from this register returns the same count value it was initialized (loaded) with.

A write to the Capture Upper Base register will load the value in both base registers to the current count register. Therefore, in order to load the count value correctly, the lower count value must be first written into the Lower Base Count register and then followed by the count value's upper byte written into the Upper Base Count register.

Capture Lower Base Count (I31)

D7	D6	D5	D4	D3	D2	D1	D0
CLB7	CLB6	CLB5	CLB4	CLB3	CLB2	CLB1	CLB0

The initial value of this register upon power up is 0000 0000.

CLB7 - CLB0 **Capture Lower Base**

This register represents the 8 least significant bits of the 16-bit capture base register. Reading from this register returns the same count value it was initialized (loaded) with.

Summary of Operation Modes

MODE 1	MODE 2
This is the default mode upon power up	Must set MODE 2 bit of MODE and ID register (I12) to enable this mode.
Allows access to the first 16 indirect registers	Allows access to all 32 indirect registers
Single DMA Channel Mode only	Single or Dual DMA Channel Mode available
No Simultaneous Playback and Capture	Simultaneous Playback and Capture available
Audio Data Formats: • 16-bit Signed "Little Endian" [1] • 8-bit Unsigned • 8-bit Companded, μ-Law • 8-bit Companded, A-Law	Audio Data Formats: • 16-bit Signed "Little Endian" [1] • 8-bit Unsigned • 8-bit Companded, μ-Law • 8-bit Companded, A-Law • 4-bit ADPCM • 16-bit Signed "Big Endian" [2]
Fs & Playback Data Format Register (I8) determines audio data format for both capture and playback	Fs & Playback Data Format Register (I8) determines audio data format for playback while Capture Data Format Register (I28) determines the audio data format for capture
Backward compatible with: • Analog Devices AD1848 • Crystal CS4248	Backward compatible with: • Crystal CS4231
Chrontel Enhanced Mode inactive	Chrontel Enhanced Mode: • Digital audio serial interface with: a. selectable data rate conversion b. programmable input attenuation and mute control • Programmable FIFO request control • Analog and digital mixer gain-scaling capabilities • Individual mode change enable bits for capture and playback data formats • Software resetable registers • Fast crystal clock source switching time via the XTALE register bit

Note: 1. "Little Endian" format refers to the byte ordering of a multiple word as having the least significant byte occupying the lowest memory address.
2. "Big Endian" format is similar to the Little Endian format except the upper byte is transferred first before the lower byte.

Table 16 • Analog Characteristics

(TA = 25 °C; VA1,VA2,VD1–VD4 = +5V; Input Levels: Logic 0 = 0V, Logic 1 = +5V; 1 kHz Input Sine wave; Conversion Rate = 48 kHz; Measurement Bandwidth is 10 Hz to 20 kHz, 16 bit linear coding)

Parameter		Symbol	Min	Typ	Max	Units
ANALOG INPUT CHARACTERISTICS - Minimum gain setting (0 dB); Unless Otherwise Specified						
ADC Resolution [1]			16	–	–	Bits
ADC Differential Nonlinearity [1]			–	–	± 0.5	LSB
Instantaneous Dynamic Range	Line Inputs Mic Inputs [2]	IDR	80 72	85 77	– –	dB dB
Total Harmonic Distortion	Line Inputs Mic Inputs [2]	THD	– –	0.003 0.01	0.02 0.025	% %
Signal-to-Intermodulation Distortion			–	90	–	dB
Inter-channel Isolation	Line to Line Inputs Line to Mic Inputs Line to AUX1 Line to AUX2		– – – –	80 80 90 90	– – – –	dB dB dB dB
Inter-channel Gain Mismatch	Line Inputs Mic Inputs		– –	– –	0.5 0.5	dB dB
Programmable Input Gain Span	Line Inputs		21.5	22.5	–	dB
Gain Step Size			1.3	1.5	1.7	dB
ADC Offset Error	0 dB gain		–	10	100	LSB
Gain Error			–	–	5	%
Full Scale Input Voltage	(MGE=1) MIC Inputs (MGE=0) MIC Inputs LINE, AUX1, AUX2, MIN Inputs		0.266 2.66 2.66	0.28 2.8 2.8	0.294 2.94 2.94	V_{pp} V_{pp} V_{pp}
Gain Drift			–	100	–	ppm/ °C
Input Resistance [1]			20	–	–	kΩ
Input Capacitance [1]			–	–	15	pF

Note: 1. This specification is guaranteed by characterization, not production testing.
2. MGE = 1 and a 10 mF capacitor on the VREF pin.

Analog Characteristics *(Continued)*

Parameter		Symbol	Min	Typ	Max	Units
ANALOG OUTPUT CHARACTERISTICS - Minimum Attenuation (0 dB); Unless Otherwise Specified						
DAC Resolution			16	–	–	Bits
DAC Differential Nonlinearity [1]			–	–	± 0.5	LSB
Dynamic Range	– Total All Outputs – Instantaneous	TDR IDR	– 80	95 85	– –	dB dB
Total Harmonic Distortion [4]		THD	–	0.01	0.02	%
Signal to Intermodulation Distortion			–	85	–	dB
Interchannel Isolation [4]	Line Out		–	95	–	dB
Interchannel Gain Mismatch	Line Out		–	0.1	0.5	dB
Voltage Reference Output			2.15	2.25	2.35	V
Voltage Reference Output Current [3]			–	100	–	µA
DAC Programmable Attenuation Span			93	94.5	–	dB
DAC Attenuation Step Size	0 dB to –81 dB –82.5 dB to –94.5 dB		1.3 1.0	1.5 1.5	1.7 2.0	dB dB
DAC Offset Voltage			–	1	10	mV
Full Scale OutputVoltage	OLB = 1 [4,5] OLB = 0 OUT, MOUT		1.9 2.66	2.0 2.8	2.1 2.94	V_{pp} V_{pp}
Gain Drift			–	100	–	ppm/ °C
Deviation from Linear Phase [1]			–	–	1	Degree
External Load Impedance			10	–	–	kΩ
Mute Attenuation (0 dB)			80	–	–	dB
Total Out-of-Band Energy [1]	0.6xFs to 3 MHz		–	–	-45	dB
Audible Out-of-Band Energy	(Fs=8kHz) 0.6xFs to 22 kHz		–	–	-60	dB
POWER SUPPLY						
Power Supply Current	Digital, Operating Analog, Operating Total Digital, Power Down Analog, Power Down		– – – – –	55 43 98 – –	65 60 120 1 1	mA mA mA mA mA
Power Supply Rejection [1]	1 kHz		40	–	–	dB

Note:
3. DC current only. If dynamic loading exists, then the voltage reference output must be buffered or the performance of ADCs and DACs will be degraded.
4. 10 kW, 100 pF load
5. All mixer and output gain tables assume the output level bit, OLB, in Indirect register 16 (I16) is set, wherein the input and output full scale values are equal. When OLB=0, the output value is 3 dB below the input value, given no gain or attenuation.

Table 17 • Auxiliary Input Mixers

(TA = 25 °C; VA1, VA2, VD1–VD4 = +5V; Input Levels: Logic 0 = 0V, Logic 1 = +5V; 1 kHz Input Sine wave)

Parameter		Symbol	Min	Typ	Max	Units
Mixer Gain RangeSpan [6]	LINE, AUX1, AUX2 MIN		45 42	46.5 45	– –	dB dB
Step Size	LINE, AUX1, AUX2 MIN		1.3 2.3	1.5 3.0	1.7 3.4	dB dB

Note: 6. All mixer gain values assume OLB=1. If OLB=0, the analog output will be 3 dB below listed settings.

Table 18 • Absolute Maximum Ratings

(AGND, DGND = 0 V, all voltages with respect to 0V)

Parameter		Symbol	Min	Max	Units
Power Supplies:	Digital Analog	VD1–VD4 VA1,VA2	–0.3 –0.3	6.0 6.0	V V
Input Current Per Pin	(Except Supply Pins)		–10	10	mA
Output Current Per Pin	(Except Supply Pins)		–50	50	mA
Analog Input Voltage			–0.3	VA + 0.3	V
Digital Input Voltage			–0.3	VD + 0.3	V
Ambient Temperature	(Power Applied)		–55	+125	°C
Storage Temperature			–65	+150	°C

Caution: Operation beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Table 19 • Recommended Operating Conditions

(AGND, DGND = 0V, all voltages with respect to 0V)

Parameter		Symbol	Min	Typ	Max	Units
Power Supplies:	Digital Analog	VD1–VD4 VA1,VA2	4.75 4.75	5.0 5.0	5.25 5.25	V V
Operating Ambient Temperature		TA	0	25	70	°C

Table 20 • Digital Filter Characteristics

Parameter		Symbol	Min	Typ	Max	Units
Passband			0	–	0.40xFs	Hz
Frequency Response			–0.5	–	+ 0.2	dB
Passband Ripple	(0 – 0.4xFs)		–	–	± 0.1	dB
Transition Band			0.4xFs	–	0.6xFs	Hz
Stop Band			0.6xFs	–	–	Hz
Stop Band Rejection			74	–	–	dB
Group Delay			–	–	30/Fs	s
Group Delay Variation vs. Frequency	ADCs DACs		– –	– –	0.0 0.1/Fs	µs µs

Table 21 • Digital Characteristics

(TA = 25 C; VA1,VA2, VD1–VD4 = 5V; AGND1, AGND2, DGND1–DGND4, DGND7, DGND8 = 0V.)

Parameter		Symbol	Min	Max	Units
High-level Input Voltage	Digital Inputs X1I, X2I, PDWN*	VIH	2.0 VD - 1.0	VD + 0.3 VD + 0.3	V V
Low-level Input Voltage		VIL	-0.3	0.8	V
High- level Output Voltage	D[7:0] Io = –16 mA All Others Io = –1 mA	VOH	2.4 2.4	VD VD	V V
Low- level Output Voltage	D[7:0] Io = 16 mA All Others Io = 4 mA	VOL	– –	0.4 0.4	V V
Input Leakage Current	(Digital Inputs)	–	–10	10	µA
Output Leakage Current	(High-Z Digital Outputs)	–	–10	10	µA

Table 22 • Timing Parameters

Parameter	Description	Min	Max	Units
tSTW	WR* or RD* strobe width	90	–	ns
tWDSU	Data valid to WR* rising edge (write cycle)	22	–	ns
tRDDV	RD* falling edge to data valid (read cycle)	–	60	ns
tCSSU	CS* setup to WR* or RD* falling edge	10	–	ns
tCSHD	CS* hold from WR* or RD* rising edge	0	–	ns
tADSU	ADDR<> setup to RD* or WR* falling edge	22	–	ns
tADHD	ADDR<> hold from WR* or RD* rising edge	10	–	ns
tSUDK1	DAK* inactive to WR* or RD* falling edge (DMA cycle completion immediately followed by a PIO cycle)	60	–	ns
tSUDK2	DAK* active to WR* or RD* rising edge (DMA cycle completion immediately followed by a PIO cycle)	0	–	ns
tDKSUa tDKSUb	DAK* setup to RD* falling edge (DMA cycles) DAK* setup to WR* falling edge	25 25	– –	ns ns
tDHD2	Data hold from WR* rising edge	15	–	ns
tDRHD	DRQ hold from WR* or RD* falling edge (assumes no more DMA cycles needed)	0	25	ns
tBWDN	Time between rising edge of WR* or RD* to next falling edge of WR* or RD*	80	–	ns
tDHD1	Data hold from RD* rising edge	0	20	ns
tDHKa tDHKb	DAK* hold from WR* rising edge DAK* hold from RD* rising edge	25 25	– –	ns ns
tDBDL	DBEN* or DBDIR* active from WR* or RD* falling edge	–	40	ns
tPDWN	PDWN* pulse width low	200	–	ns
Serial Port Timing				
fSBCK	SBCK frequency		64xFS	Hz
tSDINS	SDIN setup time		25	ns
tSDINH	SDIN hold time		25	ns
tSDOUTD	SDOUT output delay		50	ns
tSLRCKS	SLRCK setup time		25	ns
tSLRCKH	SLRCK hold time		25	ns

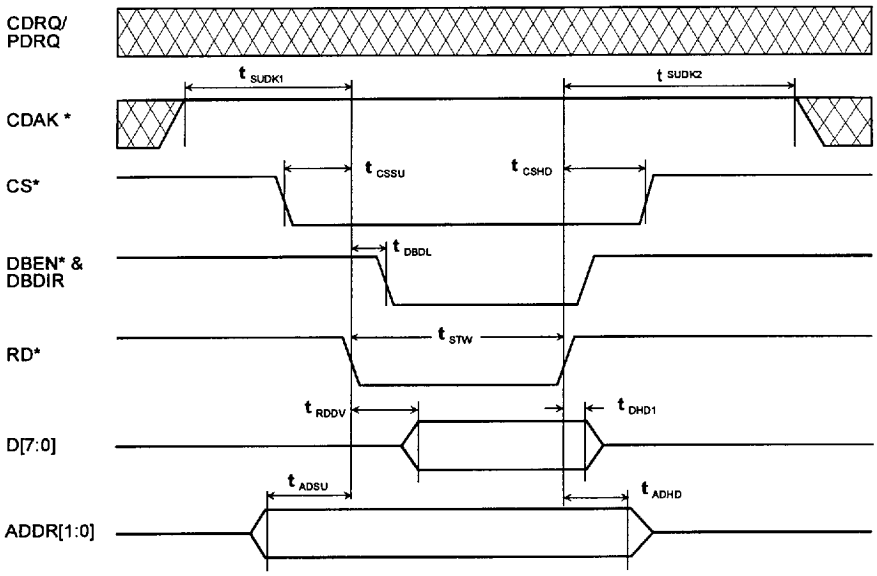

Figure 28: Programmed I/O Read Cycle

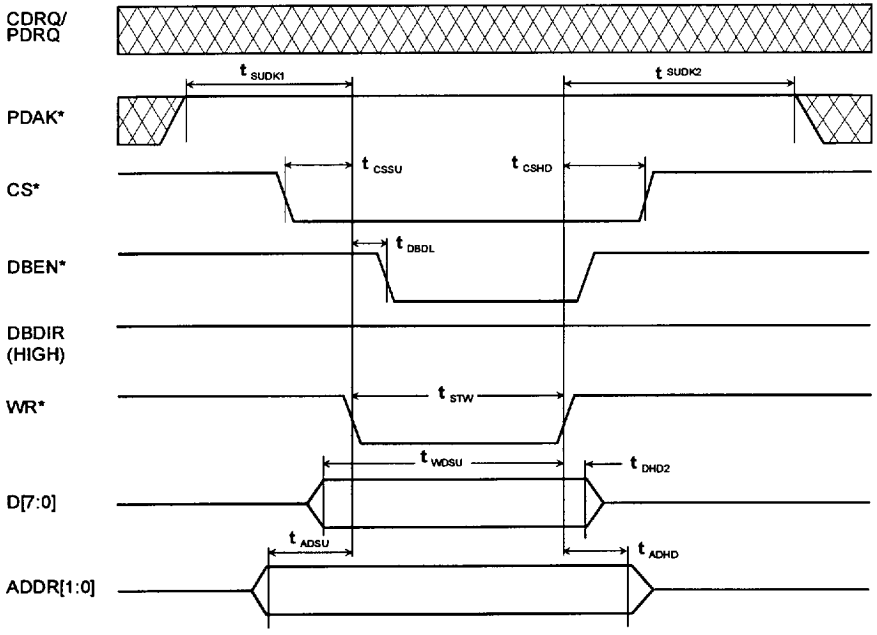

Figure 29: Programmed I/O Write Cycle

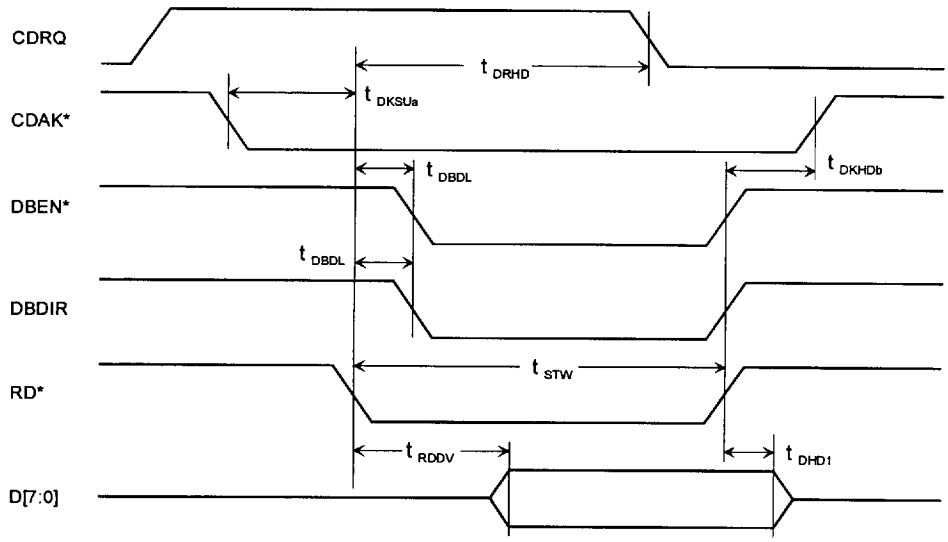

Figure 30: 8-Bit Mono DMA Read / Capture Cycle

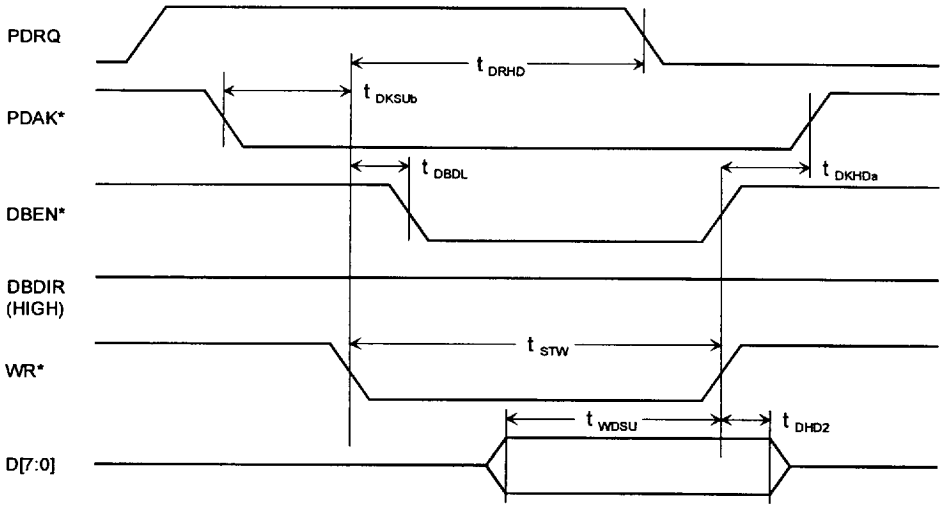

Figure 31: 8-Bit Mono DMA Write / Playback Cycle

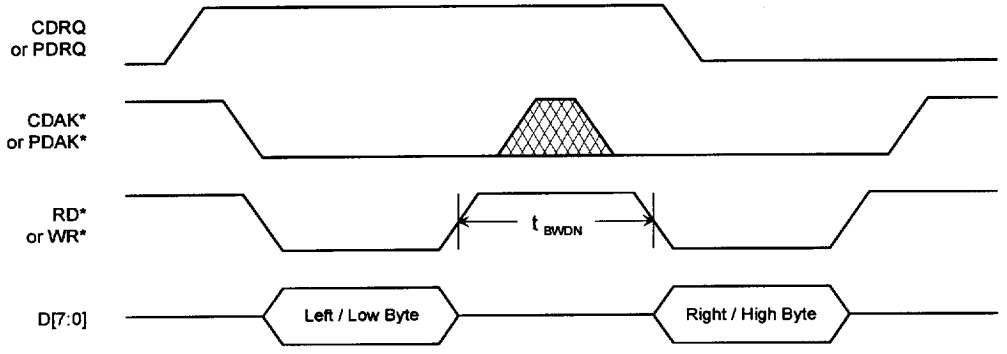

Figure 32: 8-Bit Stereo or 16-Bit Mono DMA Cycle

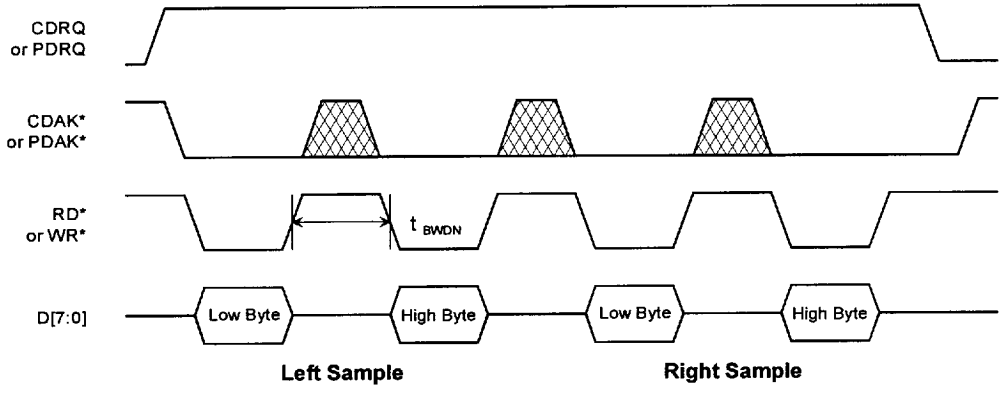

Figure 33: 16-Bit "Little Endian" Stereo DMA Cycle

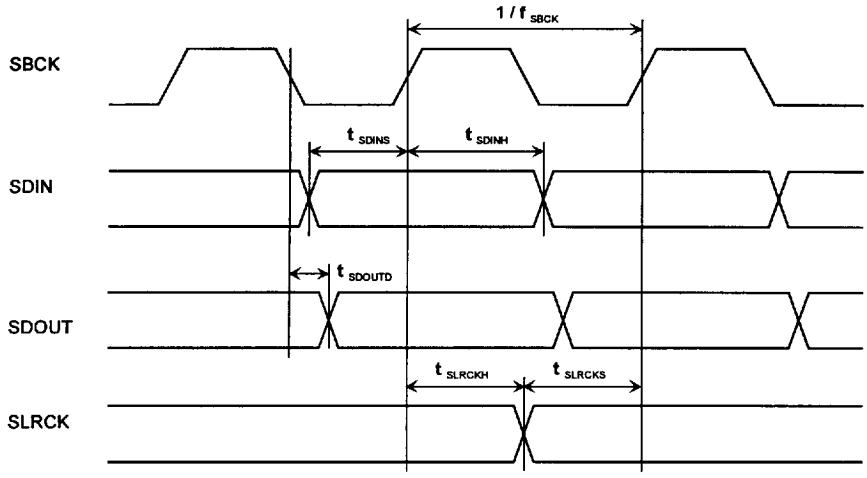

Figure 34: Serial Port Timing

ORDERING INFORMATION			
Part number	Package type	Number of pins	Voltage supply
CH6357-V	PLCC	68	5V and 3.3V
CH6357-T	TQFP	100	5V and 3.3V