Description

The μPD42275 is a dual-port graphics buffer equipped with a random access port and a serial read port. The serial read port is connected to an internal 2048-bit data register through a 256 x 8-bit serial read output circuit. The 128K x 8-bit random access port is used by the host CPU to read or write data addressed in any desired order.

A write-per-bit capability allows each of the eight data bits to be individually selected or masked for a write cycle. Block write cycles can also be used to write the eight data bits to four consecutive column addresses. Selection and masking of the eight data bits and four column addresses is provided. A flash write option with write-per-bit control enables data in the color register to be written to a selected row in the random access port.

The μPD42275 features fully asynchronous dual access, except when transferring graphics data from a selected row of the storage array to the data register. During a data transfer, the random access port requires a special cycle using a transfer clock; the serial port continues to operate normally. Following the clock transition of a data transfer, serial output data changes from an old line to a new line and the starting location on the new line is addressable in the data transfer cycle.

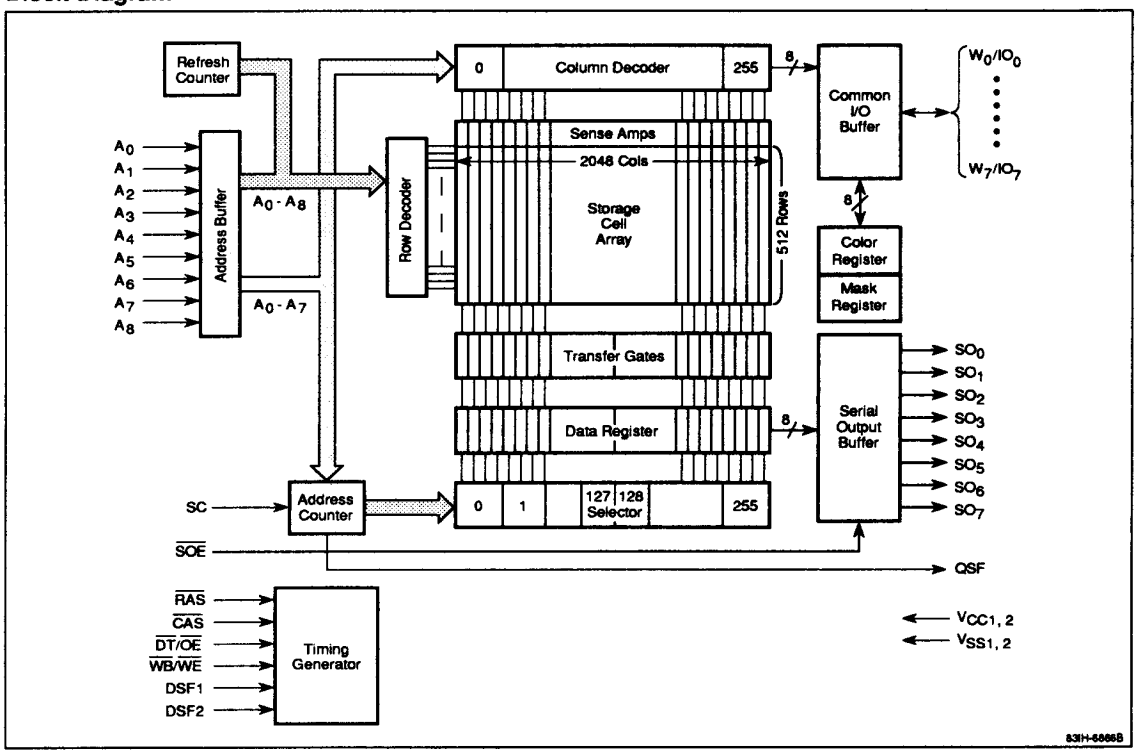
An advanced CMOS silicon-gate process using polycide technology and trench capacitors provides high storage cell density, high performance, and high reliability. Refreshing is accomplished by means of $\overline{RAS}$-only refresh cycles or by normal read or write cycles on the 512 address combinations of A_0 through A_8 during an 8-ms period. Automatic internal refreshing, by means of either hidden refreshing or the $\overline{CAS}$ before $\overline{RAS}$ timing and on-chip internal refresh circuitry, is also available. The transfer of a row of data from the storage array to the data register also refreshes that row automatically.

All inputs and outputs, including clocks, are TTL-compatible. All address and data-in signals are latched on-chip to simplify system design. Data-out is unlatched to allow greater system flexibility. The μPD42275 is available in a 400-mil, 40-pin plastic SOJ and is guaranteed for operation at 0 to +70°C.

Features

- Three functional blocks
  - 128K x 8-bit random access storage array
  - 2048-bit data register
  - 256 x 8-bit serial read output circuit
- Two data ports: random access and serial read
- Dual-port accessibility except during data transfer
- Addressable start of serial read operation
- Real-time data transfer
- On-chip substrate bias generator
- Random access port
  - Two main clocks: $\overline{RAS}$ and $\overline{CAS}$
  - Multiplexed address inputs
  - Direct connection of I/O and address lines allowed by $\overline{OE}$ to simplify system design
  - 512 refresh cycles every 8 ms
  - Read, early write, late write, read-write/read-modify-write, $\overline{RAS}$-only refresh, and fast-page cycles
  - Automatic internal refreshing by means of the $\overline{CAS}$ before $\overline{RAS}$ on-chip address counter
  - $\overline{CAS}$-controlled hidden refreshing
  - Persistent and nonpersistent write-per-bit option regarding eight I/O bits
  - Write bit selection multiplexed on IO_0 - IO_7
- Block write option with write-per-bit control and column mask function
- Flash write option with write-per-bit control
- Split serial data register to allow shifting from lower half while simultaneously loading upper half
- $\overline{RAS}$-activated data transfer
  - Same cycle time as for random access
  - Row data transferred to data register as specified by row address inputs
  - Starting location of following serial read cycle specified by column address inputs
  - Transfer of 2048 bits of data on one row to the data register, and the starting location of the serial read circuit, activated by a low-to-high transition of $\overline{DT}$
  - Data transfer during real-time operation or standby of serial port
- Fast serial read operation by means of SC pins
- Serial data output on SO_0 - SO_7
- Direct connection of multiple serial outputs for extension of data length
- Fully TTL-compatible inputs, outputs, and clocks
- Three-state outputs for random and serial access
- CMOS silicon-gate process with trench capacitors

Block Diagram



Pin Identification

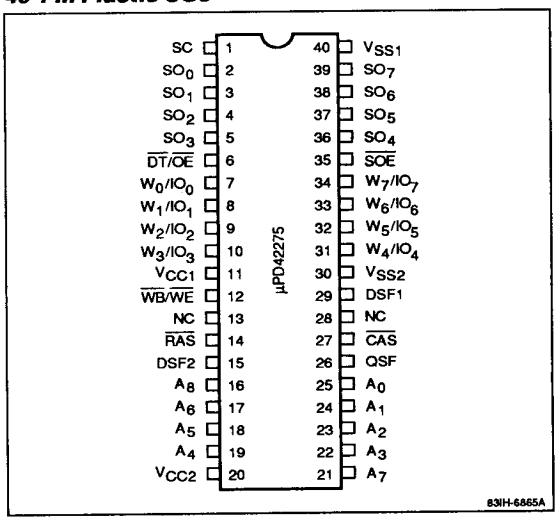
Symbol	Function
A_0 - A_8	Address inputs
W_0/IO_0 - W_7/IO_7	Write-per-bit selects/data inputs and outputs
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WB/WE}$	Write-per-bit/write enable
$\overline{DT/OE}$	Data transfer/output enable
DSF_1 and DSF_2	Special function enable
SO_0 - SO_7	Serial read outputs
SC	Serial control
$\overline{SOE}$	Serial output enable
QSF	Special function output
V_{SS1} and V_{SS2}	Ground
V_{CC1} and V_{CC2}	+5-volt ±10% power supply
NC	No connection

Ordering Information

Part Number	Row Access Time (max)	Serial Access Time (max)	Package
μPD42275LE-80	80 ns	25 ns	40-pin plastic SOJ
LE-10	100 ns	25 ns	
LE-12	120 ns	40 ns	

Pin Configuration

40-Pin Plastic SOJ



Pin Functions

A_0-A_8 (Address Inputs). These pins are multiplexed as row and column address inputs. Each of eight data bits in the random access port corresponds to 131,072 storage cells, which means that nine row addresses and eight column addresses are required to decode one cell location. Nine row addresses are first used to select one of the 512 possible rows for a read, write, data transfer, or refresh cycle. Eight column addresses are then used to select the one of 256 possible column decoders for a read or write cycle or the one of 256 possible starting locations for the next serial read cycle. (Column addresses are not required in $\overline{RAS}$-only refresh cycles.)

W_0/IO_0-W_7/IO_7 (Write-Per-Bit Inputs/Common Data Inputs and Outputs). Each of the eight data bits can be individually latched by these inputs at the falling edge of $\overline{RAS}$ in any write cycle, and then updated at the next falling edge of $\overline{RAS}$. In a read cycle, these pins serve as outputs for the selected storage cells. In a write cycle, data input on these pins is latched by the falling edge of $\overline{CAS}$ or $\overline{WE}$.

$\overline{RAS}$ (Row Address Strobe). This pin is functionally equivalent to a chip enable signal in that whenever it is activated, the 2048 storage cells of a selected row are sensed simultaneously and the sense amplifiers restore all data. The nine row address bits are latched by this signal and must be stable on or before its falling edge. $\overline{CAS}$, $\overline{DT/OE}$, $\overline{WB/WE}$, DSF_1 and DSF_2 are simultaneously latched to determine device operation.

$\overline{CAS}$ (Column Address Strobe). This pin serves as a chip selection signal to activate the column decoder and the input/output buffers. The eight column address bits are latched at the falling edge of $\overline{CAS}$.

QSF (Special Function Output). This pin indicates which side of the split register is active. QSF high shows that the upper half (addresses 128 through 255) is active, while QSF low indicates the lower half (addresses 0 through 127).

DSF_1 and DSF_2 (Special Function Control). At the leading edge of $\overline{RAS}$ and $\overline{CAS}$, the high or low level of these pins is latched to initiate one of the operations shown in the Truth Table. Holding both pins low causes the device to operate without any special functions.

$\overline{WB/WE}$ (Write-Per-Bit Control/Write Enable). At the falling edge of $\overline{RAS}$, the $\overline{WB/WE}$ and DSF_1 inputs must be low and $\overline{CAS}$ and $\overline{DT/OE}$ high to enable the write-per-bit option. When $\overline{CAS}$, $\overline{DT/OE}$, and DSF_1 are high at the falling edge of $\overline{RAS}$, the level of this signal indicates either a color register set cycle or flash write cycle. A high $\overline{WB/WE}$ can be used at the beginning of a standard write or read cycle.

$\overline{DT/OE}$ (Data Transfer/Output Enable). At the $\overline{RAS}$ falling edge, $\overline{CAS}$ and $\overline{WB/WE}$ high and $\overline{DT/OE}$ low initiate a data transfer. $\overline{DT/OE}$ high initiates conventional read or write cycles and controls the output buffer in the random access port. The level of DSF_1 determines whether this is a read or split read data transfer.

SO_0-SO_7 (Serial Data Outputs). Eight-bit data is read from these pins and remains valid until the next SC signal is activated.

SC (Serial Control). Repeatedly activating this signal causes serial read cycles (starting from the location specified in the data transfer cycle) to be executed within the 2048 bits in the data register. The rising edge of SC activates serial read operation, in which 8 of the 2048 data bits are transferred to eight serial data buses, respectively, and read out. Whenever SC is low, the serial port is in standby.

$\overline{SOE}$ (Serial Output Enable). This signal controls the serial data output buffer.

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OPERATION

The μPD42275 consists of a random access port and a serial read port. The random access port executes standard read and write cycles, as well as data transfer, block write and flash write cycles, all of which are based on conventional $\overline{RAS}/\overline{CAS}$ timing.

In a data transfer, data in each storage cell on the selected row is transferred simultaneously through a transfer gate to its corresponding register location. The serial read port shows the contents of the data register in serial order. The random access and serial read ports can operate asynchronously, except when the transfer gate is turned on during the data transfer period.

Addressing

The storage array is arranged in a 512-row by 2048-column matrix, whereby each of 8 data bits in the random access port corresponds to 131,072 storage cells and 17 address bits are required to decode one cell location. Nine row address bits are set up on pins A_0 through A_8 and latched onto the chip by $\overline{RAS}$. Eight column address bits then are set up on pins A_0 through A_7 and latched onto the chip by $\overline{CAS}$. All addresses must be stable, on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. Whenever $\overline{RAS}$ is activated, 2048 cells on the selected row are sensed simultaneously and the sense amplifiers automatically restore the data. $\overline{CAS}$ serves as a chip selection signal to activate the column decoder and the input and output buffers.

Through one of 256 column decoders, eight storage cells on the row are connected to eight data buses, respectively. In a data transfer cycle, 9 row address bits are used to select one of the 512 possible rows involved in the transfer of data to the data register. Eight column address bits are then used to select the one of 256 possible serial decoders that corresponds to the starting location of the next serial read cycle. In the serial read port, when SC is activated, 8 data bits in the 2048-bit data register are transferred to eight serial data buses and read out. Activating SC repeatedly causes serial read cycles (starting from the location specified in the data transfer cycle) to be executed within the 2048 bits in the data register.

Random Access Port

An operation in the random access port begins with a negative transition of $\overline{RAS}$. Both $\overline{RAS}$ and $\overline{CAS}$ have minimum pulse widths, as specified in the timing table, which must be maintained for proper device operation and data integrity. Once begun, a cycle must meet all specifications, including minimum cycle time. To reduce the number of pins, the following are multiplexed.

- $\overline{DT}/\overline{OE}$
- $\overline{WB}/\overline{WE}$
- W_i/IO_i (i = 0, 1, 2, 3, 4, 5, 6, 7)

The $\overline{OE}$, $\overline{WE}$, and IO_i functions represent standard operations, while $\overline{DT}$, $\overline{WB}$, and W_i are special inputs to be applied in the same way as row address inputs with setup and hold times referenced to the negative transition of $\overline{RAS}$.

The level of $\overline{DT}$ determines whether a cycle is a random access operation or a data transfer operation. $\overline{WB}$ affects only write cycles and determines whether or not the write-per-bit capability is used. W_i defines data bits to be written with the write-per-bit option. In the following discussions, these multiplexed pins are designated as $\overline{DT}(/\overline{OE})$, for example, depending on the function being described.

To use the μPD42275 for random access, $\overline{DT}(/\overline{OE})$ must be high as $\overline{RAS}$ falls. Holding $\overline{DT}(/\overline{OE})$ high disconnects the 2048-bit register from the corresponding 2048-digit lines of the storage array. Conversely, to execute a data transfer, $\overline{DT}(/\overline{OE})$ must be low as $\overline{RAS}$ falls to open the 2048 transfer gates and transfer data from one of the rows to the register.

Glossary of Special Functions

Masked Write Cycle with New Mask. When the write-per-bit function is enabled as shown in the following table, mask data on the W/IO_i pins is latched by $\overline{RAS}$ and loaded directly into the write mask register. A masked write cycle is then executed using $\overline{CAS}$ or $\overline{WB}/\overline{WE}$ to strobe the W/IO_i data into the on-chip data latch.

Write-Per-Bit Function

Mask Register Data	Action
1	Write
0	Do not write

Write Mask Register Set Cycle. In this cycle, data on W_i/IO_i is written to an 8-bit write mask register, where it is retained and used by subsequent masked write and masked block write cycles.

Masked Write Cycle with Old Mask. This write-per-bit cycle, commonly referred to as a persistent mask write cycle, uses the mask data previously set by the last write mask register set cycle.

Truth Table for Random Access Port

Cycle	Must Be Valid at Falling Edge of $\overline{RAS}$					Must be Valid at Falling Edge of $\overline{CAS}$	Mnemonic Code
	$\overline{CAS}$	$\overline{DT/OE}$	$\overline{WB/WE}$	DSF_1	DSF_2	DSF_1	
Read/write cycle	H	H	H	L	X	L	RW
Block write cycle	H	H	H	L	X	H	BW
Write mask register set cycle	H	H	H	H	X	L	LWR
Color register set cycle	H	H	H	H	X	H	LCR
Write cycle with new mask	H	H	L	L	X	L	RWNM
Block write cycle with new mask	H	H	L	L	X	H	BWNM
Write cycle with old mask	H	H	L	H	L	L	RWOM
Block write cycle with old mask	H	H	L	H	L	H	BWOM
Read data transfer cycle	H	L	H	L	X	X	RT
Split read data transfer cycle	H	L	H	H	X	X	SRT
$\overline{CAS}$ before $\overline{RAS}$ refresh cycle	L	X	H	X	X	X	CBR
Flash write cycle with new mask	H	H	L	H	H	X	FWT

Notes:

(1) X = don't care.

(2) Combinations not shown are used for refresh operation.

Block Write Addresses

Column Select By I/O Data	Result	Corresponding Column Address
$I/O_3 = 1$	Write	$A_1 = 1, A_0 = 1$
$I/O_3 = 0$	No write	
$I/O_2 = 1$	Write	$A_1 = 1, A_0 = 0$
$I/O_2 = 0$	No Write	
$I/O_1 = 1$	Write	$A_1 = 0, A_0 = 1$
$I/O_1 = 0$	No write	
$I/O_0 = 1$	Write	$A_1 = 0, A_0 = 0$
$I/O_0 = 0$	No write	

Notes:

(1) Data on I/O_7 - I/O_4 are don't care at the falling edge of $\overline{CAS}$.

Color Register Set Cycle. This cycle is executed in the same fashion as a conventional read or write cycle, with a read or write cycle available to the color register under the control of $\overline{WE}$. In read operation, color register data is read on the common W_i/IO_i pins. In write operation, common W_i/IO_i data can be written into the color register. $\overline{RAS}$-only refreshing is internally performed on the row selected by A_0 through A_8. This setup cycle precedes the first flash write or block write cycle supplying the 8 write data bits.

Block Write Cycle. In a block write cycle, A_1 and A_0 are ignored. I/O_0 - I/O_3 are used to select one or a combination of four column addresses for writing in an early write, late write, page early write, or page late write cycle. Block write data is previously stored in the color register using a set color register cycle. Column select data is latched by the W/IO_i pins at the falling edge of $\overline{CAS}$ or $\overline{WE}$. Block write cycles are useful for clearing windows and for accelerating polygon fill operations.

Masked Block Write Cycle with New Mask. This cycle allows for $W/I/O_0$ - $W/I/O_7$ masking during a block write cycle. The masking function is identical to a standard masked write cycle with new mask, except that four consecutive columns are written.

Masked Block Write Cycle with Old Mask. This cycle uses the masked data previously set by the last write mask register set cycle to write four consecutive columns.

Flash Write Cycle. A flash write cycle can clear or set each of the eight 256-bit data sets on the selected one of 512 possible rows according to data stored in the previously set color register. Bit mask inputs are latched as $\overline{RAS}$. This cycle is useful in graphics processing applications when the screen should be cleared or set to some uniform value as quickly as possible.

Read Data Transfer Cycle. In a full row read data transfer cycle, one of the possible 512 rows, as well as the starting location of the following serial read cycle, is defined by address inputs. The low-to-high transition of $DT/(\overline{OE})$ causes the 2048 bits of cell data to be transferred to the serial data register.

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Split Read Transfer Cycle. This cycle is a half-row data transfer in which one of the 512 rows, the starting location of the following serial read cycle, and either of the split registers are specified by the address inputs. On-chip control circuitry causes the previously specified half row to be transferred to the selected upper or lower split register.

Read Cycle. A read cycle is executed by activating $\overline{RAS}$, $\overline{CAS}$, and $\overline{OE}$ and by maintaining ($\overline{WB}$/)$\overline{WE}$ while $\overline{CAS}$ is active. The (W_i/)IO_i pin (i = 0 through 7) remains in high impedance until valid data appears at the output at access time. Device access time, t_{ACC}, will be the longest of the following four calculated intervals:

- t_{RAC}
- $\overline{RAS}$ to $\overline{CAS}$ delay (t_{RCD}) + t_{CAC}
- $\overline{RAS}$ to column address delay (t_{RAD}) + t_{AA}
- $\overline{RAS}$ to $\overline{OE}$ delay + t_{OEA}

Access times from $\overline{RAS}$ (t_{RAC}), from $\overline{CAS}$ (t_{CAC}), from the column addresses (t_{AA}), and from $\overline{OE}$ (t_{OEA}) are device parameters. The $\overline{RAS}$-to-$\overline{CAS}$, $\overline{RAS}$-to-column address, and $\overline{RAS}$-to-$\overline{OE}$ delays are system-dependent timing parameters. Output becomes valid after the access time has elapsed and it remains valid while both $\overline{CAS}$ and $\overline{OE}$ are low. Either $\overline{CAS}$ or $\overline{OE}$ high returns the output pins to high impedance.

Write Cycle. A write cycle is executed by bringing ($\overline{WB}$/)$\overline{WE}$ low during the $\overline{RAS}$/$\overline{CAS}$ cycle. The falling edge of $\overline{CAS}$ or ($\overline{WB}$/)$\overline{WE}$ strobes the data on (W_i/)IO_i into the on-chip data latch. To make use of the write-per-bit option, $\overline{WB}$(/$\overline{WE}$) must be low as $\overline{RAS}$ falls. In this case, write data bits can be specified by keeping W_i(/IO_i) high, with setup and hold times referenced to the negative transition of $\overline{RAS}$.

Write-Per-Bit Cycle. The falling edge of $\overline{RAS}$ latches the write-per-bit mask data input on W_0 through W_7. If DSF_1 is low at the falling edge of $\overline{RAS}$, mask data must be reloaded every write-per-bit mask cycle. If DSF_1 is high and DSF_2 is low at the falling edge of $\overline{RAS}$, mask data is not reloaded from W_0 through W_7 but is retained from the previous write mask set cycle. The latter is called a persistent write-per-bit cycle.

Early Write Cycle. An early write cycle is executed by bringing ($\overline{WB}$/)$\overline{WE}$ low before $\overline{CAS}$ falls. Data is strobed by $\overline{CAS}$, with setup and hold times referenced to this signal, and the output remains in high impedance for the entire cycle. As $\overline{RAS}$ falls, ($\overline{DT}$/)$\overline{OE}$ must meet the setup and hold times of a high $\overline{DT}$, but otherwise ($\overline{DT}$/)$\overline{OE}$ does not affect any circuit operation while $\overline{CAS}$ is active.

Read-Write/Read-Modify-Write Cycle. This cycle is executed by bringing ($\overline{WB}$/)$\overline{WE}$ low with the $\overline{RAS}$ and $\overline{CAS}$ signals low. (W_i/)IO_i shows read data at access time. Afterward, in preparation for the upcoming write cycle, (W_i/)IO_i returns to high impedance when ($\overline{DT}$/)$\overline{OE}$ goes high. The data to be written is strobed by ($\overline{WB}$/)$\overline{WE}$ with setup and hold times referenced to this signal.

Late Write Cycle. This cycle shows the timing flexibility of ($\overline{DT}$/)$\overline{OE}$, which can be activated just after ($\overline{WB}$/)$\overline{WE}$ falls, even when ($\overline{WB}$/)$\overline{WE}$ is brought low after $\overline{CAS}$.

Refresh Cycle. A cycle at each of the 512 row addresses (A_0 through A_8) will refresh all storage cells. Any cycle executed in the random access port (i.e., read, write, refresh, data transfer, color register set, flash write or block write) refreshes the 2048 bits selected by the $\overline{RAS}$ addresses or by the on-chip address counter.

$\overline{RAS}$-Only Refresh Cycle. A cycle having only $\overline{RAS}$ active refreshes all cells in one row of the storage array. A high $\overline{CAS}$ is maintained while $\overline{RAS}$ is active to keep (W_i/)IO_i in high impedance. This method is preferred for refreshing, especially when the host system consists of multiple rows of random access devices. The data outputs may be OR-tied with no bus contention when $\overline{RAS}$-only refresh cycles are executed.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle. This cycle executes internal refreshing using the on-chip control circuitry. Whenever $\overline{CAS}$ is low as $\overline{RAS}$ falls, this circuitry automatically refreshes the row addresses specified by the internal counter. In this cycle, the circuit operation based on $\overline{CAS}$ is maintained in a reset state. When internal refreshing is complete, the address counter automatically increments in preparation for the next $\overline{CAS}$ before $\overline{RAS}$ cycle.

Hidden Refresh Cycle. This cycle is executed after a read cycle, without disturbing the read data output. Once valid, the data output is controlled by $\overline{CAS}$ and $\overline{OE}$. After the read cycle, $\overline{CAS}$ is held low while $\overline{RAS}$ goes high for precharge. A $\overline{RAS}$-only cycle is then executed (except that $\overline{CAS}$ is held at a low level instead of a high level) and the data output remains valid. Since hidden refreshing is the same as $\overline{CAS}$ before $\overline{RAS}$ refreshing, the data output remains valid during either operation.

Fast-Page Cycle. This feature allows faster data access by keeping the same row address while successive column addresses are strobed onto the chip. Maintaining $\overline{RAS}$ low while successive $\overline{CAS}$ cycles are executed causes data to be transferred at a faster rate because

row addresses are maintained internally and do not have to be reapplied. In fast-page operation, read, write, and read-write/read-modify-write cycles may be executed. Additionally, the write-per-bit control specified in the entry write cycle is maintained throughout the next fast-page write cycle.

During a fast-page read cycle, the $(W_i)IO_i$ data pin (i = 0 through 7) remains in a state of high impedance until valid data appears at the output pin at access time. Device access time in this cycle will be the longest of the following intervals:

- t_{ACP}
- $t_{CP} + t_T + t_{CAC}$
- $\overline{CAS}$ high to column address delay + t_{AA}

Serial Read Port

The serial read port is used to serially read the previously loaded contents of the data register starting from a specified location. Other graphics buffers require very tight timing to synchronize this port with the random access port, but the μPD42275 has been designed with a split register to eliminate the need for synchronized timing between the two ports.

Split Register Data Transfer. A review of the split register architecture shows that the lower register (addresses 0 - 127) and upper register (addresses 128 - 255) are selected by the most significant bit of the column addresses (A_7). With the serial port split in half, data transfers can be executed to the inactive side (no SC clocks) while SC clocks are input to access data from the active side. This sequence allows for a longer time window to perform the transfer, i.e., 128 x t_{SCC}, or 3.84 μs. Column address bits A_0 through A_6 are latched on-chip to provide the tap address pointer for each split register.

QSF Special Function Output. This pin outputs a signal indicating which half of the data register is active and is synchronized with the SC clock.

Split Data Transfer Cycle

Portion of Split Register	QSF
0 through 127	Low
128 through 255	High

Notes:

(1) A full data transfer cycle must precede all split register operations.

(2) Column address A_7 must be specified for a split data transfer cycle.

Data in the data register is clocked serially by SC, starting from the first specified address of either register. After the last specified address has been transferred, QSF changes its level at the next rising edge of SC, and serial data transfer switches to the other (formerly inactive) register. Serial data output is maintained until the next SC clock.

SC clocks at the transition point, i.e., the end of one half and the beginning of the new half of the split registers, are restricted. Rising edges of the SC clock are not allowed for the last serial address (either 127 or 255) of the active register and for the first address (any address depending on current address pointer) of the next active register (figure 2).

$\overline{SOE}$ controls impedance of the serial output to allow multiplexing of more than one bank of μPD42275s on the same bus and has no effect on SC. When $\overline{SOE}$ is low, SO_i is disabled and in a state of high impedance.

Figure 1. Example of Split Register Transfer

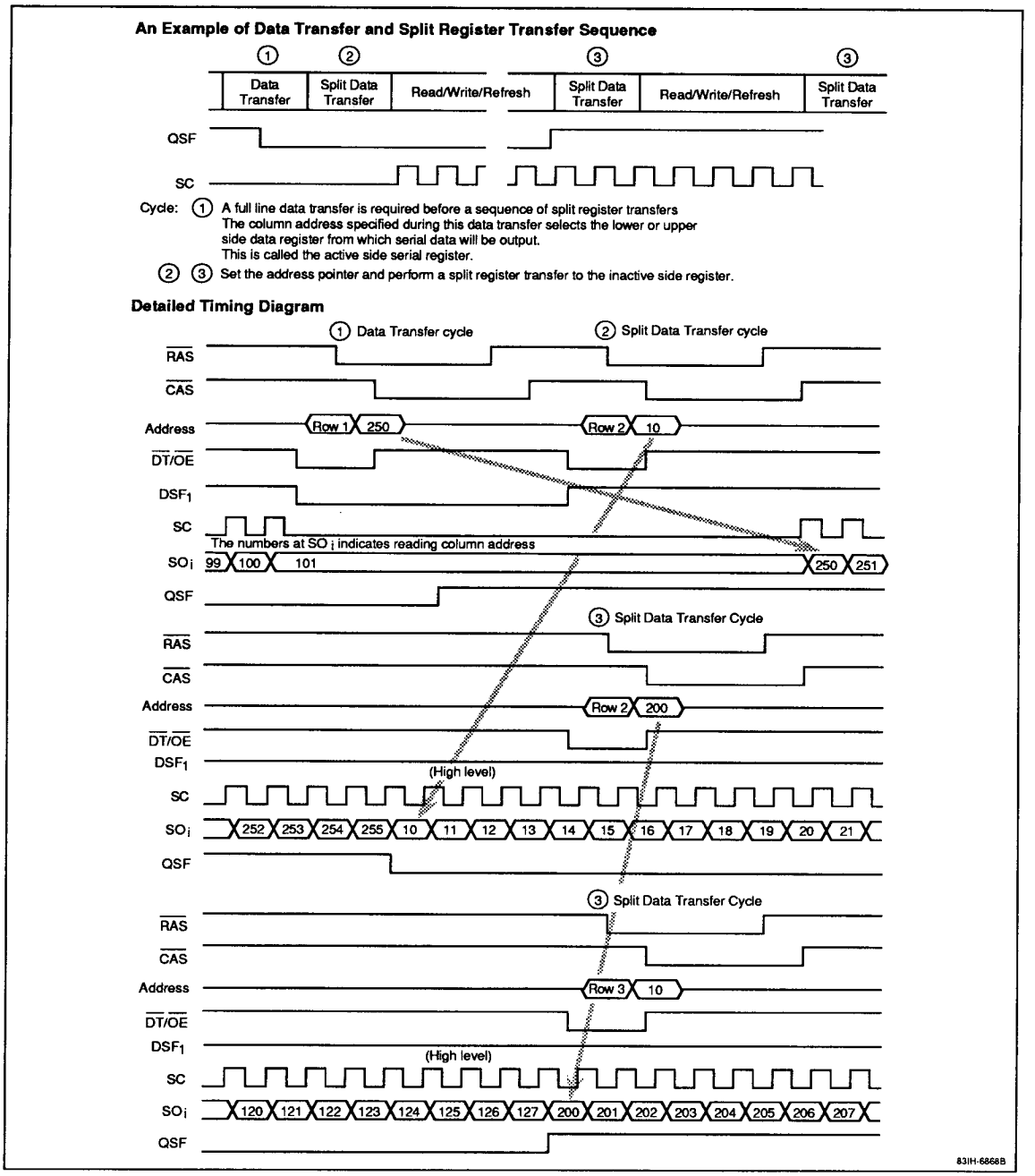
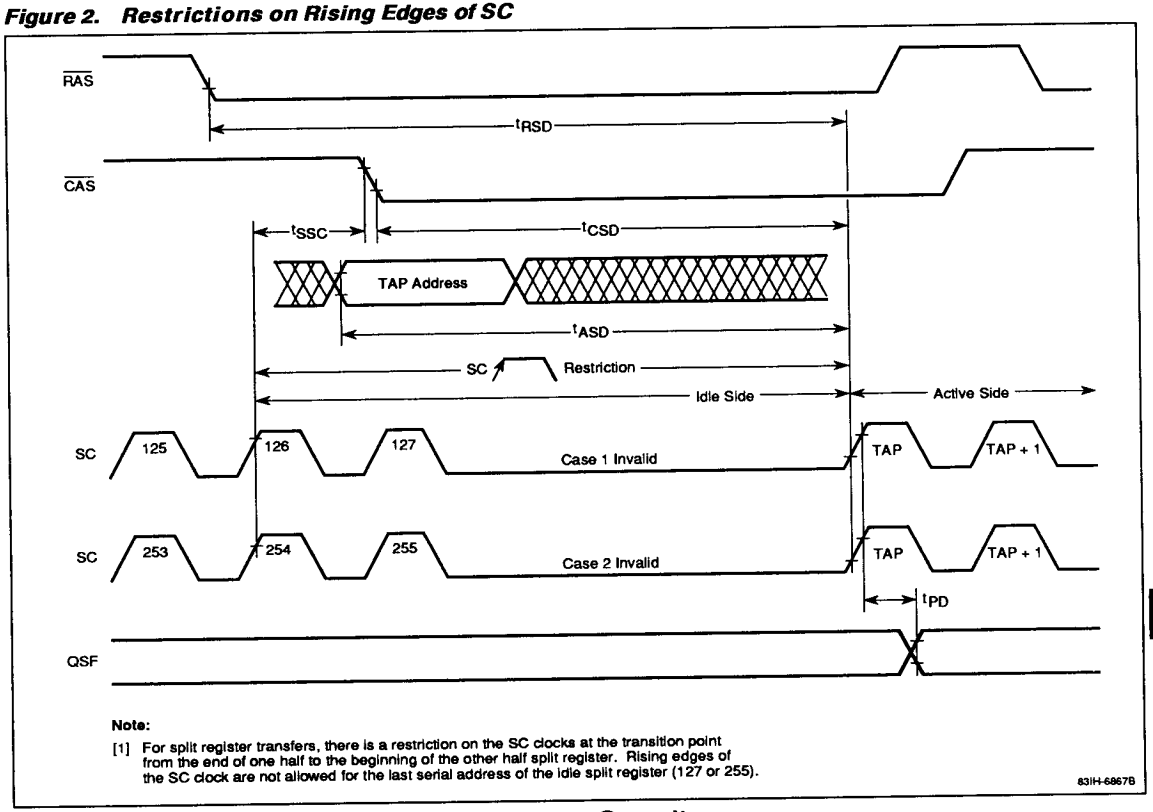


Figure 2. Restrictions on Rising Edges of SC



Note:

[1] For split register transfers, there is a restriction on the SC clocks at the transition point from the end of one half to the beginning of the other half split register. Rising edges of the SC clock are not allowed for the last serial address of the idle split register (127 or 255).

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Absolute Maximum Ratings

Voltage on any pin relative to GND, V_{R1}	−1.0 to +7.0 V
Voltage on V_{CC} relative to GND, V_{R2}	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	1.5 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, high	V_{IH}	2.4		5.5	V
Input voltage, low	V_{IL}	−1.0		0.8	V
Ambient temperature	T_A	0		70	°C

Capacitance

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%; f = 1 MHz; GND = 0 V

Parameter	Symbol	Max (pF)	Pins Under Test
Input capacitance	$C_{I(A)}$	5	A_0 - A_8
	$C_{I(\overline{DT}/\overline{OE})}$	8	$\overline{DT}/\overline{OE}$
	$C_{I(\overline{WB}/\overline{WE})}$	8	$\overline{WB}/\overline{WE}$
	$C_{I(DSF)}$	8	DSF_1 and DSF_2
	$C_{I(\overline{RAS})}$	8	$\overline{RAS}$
	$C_{I(\overline{CAS})}$	8	$\overline{CAS}$
	$C_{I(\overline{SOE})}$	8	$\overline{SOE}$
	$C_{I(SC)}$	8	SC
Input/output capacitance	$C_{IO(W/IO)}$	7	W_0/IO_0 - W_7/IO_7
Output capacitance	$C_{O(SO)}$	7	SO_0 - SO_7
	$C_{O(QSF)}$	7	QSF

Power Supply Current

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%; GND = 0 V

Port Operation							
Random Access	**Serial Read**	**Parameter**	**−80 (max)**	**−10 (max)**	**−12 (max)**	**Unit**	**Test Conditions**
Read/write cycle	Standby	I_{CC1}	95	85	70	mA	$\overline{RAS}$ and $\overline{CAS}$ cycling; DSF_1 and DSF_2 low as $\overline{RAS}$ falls; $t_{RC} = t_{RC}$ min; $\overline{SOE} = V_{IH}$; SC = V_{IH} or V_{IL}
Standby	Standby	I_{CC2}	10	10	10	mA	D_{OUT} = high impedance; address cycling; $t_{RC} = t_{RC}$ min; $\overline{CAS} = \overline{RAS} = V_{IH}$; $\overline{SOE} = V_{IH}$; SC = V_{IH} or V_{IL} (Note 4)
$\overline{RAS}$-only refresh cycle	Standby	I_{CC3}	85	80	65	mA	$\overline{RAS}$ cycling; $\overline{CAS} = V_{IH}$; DSF_1 and DSF_2 low as $\overline{RAS}$ falls; $t_{RC} = t_{RC}$ min; $\overline{SOE} = V_{IH}$; SC = V_{IH} or V_{IL} (Note 2)
Fast-page cycle	Standby	I_{CC4}	85	80	65	mA	$\overline{RAS} = V_{IL}$; $\overline{CAS}$ cycling; $t_{PC} = t_{PC}$ min; $\overline{SOE} = V_{IH}$; SC = V_{IH} or V_{IL} (Note 3)
$\overline{CAS}$ before $\overline{RAS}$ refresh cycle	Standby	I_{CC5}	85	75	60	mA	$\overline{CAS}$ low as $\overline{RAS}$ falls; $t_{RC} = t_{RC}$ min; $\overline{SOE} = V_{IH}$; SC = V_{IH} or V_{IL}
Data transfer cycle	Standby	I_{CC6}	115	100	85	mA	$\overline{DT}$ low as $\overline{RAS}$ falls; $t_{RC} = t_{RC}$ min; $\overline{SOE} = V_{IH}$; SC = V_{IH} or V_{IL}
Read/write cycle	Active	I_{CC7}	125	110	90	mA	$\overline{RAS}$ and $\overline{CAS}$ cycling; DSF_1 and DSF_2 low as $\overline{RAS}$ falls; $t_{RC} = t_{RC}$ min; $\overline{SOE} = V_{IL}$; SC cycling; $t_{SCC} = t_{SCC}$ min
Standby	Active	I_{CC8}	40	35	30	mA	D_{OUT} = high impedance; address cycling; $t_{RC} = t_{RC}$ min; $\overline{CAS} = \overline{RAS} = V_{IH}$; $\overline{SOE} = V_{IL}$; SC cycling; $t_{SCC} = t_{SCC}$ min (Note 4)
$\overline{RAS}$-only refresh cycle	Active	I_{CC9}	115	105	85	mA	$\overline{RAS}$ cycling; $\overline{CAS} = V_{IH}$; DSF_1 and DSF_2 low as $\overline{RAS}$ falls; $t_{RC} = t_{RC}$ min; $\overline{SOE} = V_{IL}$; SC cycling; $t_{SCC} = t_{SCC}$ min
Fast-page cycle	Active	I_{CC10}	105	90	75	mA	$\overline{RAS} = V_{IL}$; $\overline{CAS}$ cycling; $t_{PC} = t_{PC}$ min; $\overline{SOE} = V_{IL}$; SC cycling; $t_{SCC} = t_{SCC}$ min (Note 3)
$\overline{CAS}$ before $\overline{RAS}$ refresh cycle	Active	I_{CC11}	115	100	80	mA	$\overline{CAS}$ low as $\overline{RAS}$ falls; $t_{RC} = t_{RC}$ min; $\overline{SOE} = V_{IL}$; SC cycling; $t_{SCC} = t_{SCC}$ min
Data transfer cycle	Active	I_{CC12}	145	125	105	mA	$\overline{DT}$ low as $\overline{RAS}$ falls; $t_{RC} = t_{RC}$ min; $\overline{SOE} = V_{IL}$; SC cycling; $t_{SCC} = t_{SCC}$ min
Color register set cycle	Standby	I_{CC13}	80	70	55	mA	$t_{RC} = t_{RC}$ min; $\overline{SOE} = V_{IH}$; SC = V_{IH} or V_{IL}
Flash write cycle	Standby	I_{CC14}	80	70	55	mA	$t_{RC} = t_{RC}$ min; $\overline{SOE} = V_{IH}$; SC = V_{IH} or V_{IL}
Color register set cycle	Active	I_{CC15}	110	95	75	mA	$t_{RC} = t_{RC}$ min; $\overline{SOE} = V_{IL}$; SC cycling; $t_{SCC} = t_{SCC}$ min

Power Supply Current (cont)

Port Operation							
Random Access	**Serial Read**	**Parameter**	**-80 (max)**	**-10 (max)**	**-12 (max)**	**Unit**	**Test Conditions**
Flash write cycle	Active	I_{CC16}	110	95	75	mA	$t_{RC} = t_{RC}$ min; $\overline{SOE} = V_{IL}$; SC cycling; $t_{SCC} = t_{SCC}$ min
Block write cycle	Standby	I_{CC17}	95	85	75	mA	$t_{RC} = t_{RC}$ min; $\overline{SOE} = V_{IH}$; SC = V_{IH} or V_{IL}
Block write cycle	Active	I_{CC18}	125	110	95	mA	$t_{RC} = t_{RC}$ min; $\overline{SOE} = V_{IL}$; SC cycling; $t_{SCC} = t_{SCC}$ min

Notes:

(1) No load on IO_i or SO_i. Except for I_{CC2}, I_{CC3}, I_{CC6}, and I_{CC14}, real values depend on output loading in addition to cycle rates.

(2) $\overline{CAS}$ is not clocked, but is kept at a stable high level. The column addresses are also assumed to be kept stable, at either a high or low level.

(3) A change in column addresses must not occur more than once in a fast-page cycle.

(4) A change in row addresses must not occur more than once in a read or write cycle.

DC Characteristics

$T_A = 0$ to $+70°C$; $V_{CC} = +5.0\ V \pm 10\%$; GND = 0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{IL}	-10		10	μA	V_{IN} = 0 to 5.5 V; all other pins not under test = 0 V
Output leakage current	I_{OL}	-10		10	μA	D_{OUT} (IO_i, SO_i) disabled; V_{OUT} = 0 to 5.5 V
Random access port output voltage, high	$V_{OH(R)}$	2.4			V	$I_{OH(R)} = -1$ mA
Random access port output voltage, low	$V_{OL(R)}$			0.4	V	$I_{OL(R)} = 2.1$ mA
Serial read port output voltage, high	$V_{OH(S)}$	2.4			V	$I_{OH(S)} = -1$ mA
Serial read port output voltage, low	$V_{OL(S)}$			0.4	V	$I_{OL(S)} = 2.1$ mA

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AC Characteristics

$T_A = 0$ to $+70°C$; $V_{CC} = +5.0\ V \pm 10\%$; GND = 0 V

		μPD42275-80		μPD42275-10		μPD42275-12			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
Access time from column address	t_{AA}		45		50		65	ns	(Notes 3 and 4)
Access time from rising edge of $\overline{CAS}$	t_{ACP}		45		55		65	ns	(Notes 3 and 4)
$\overline{DT}$ low hold time after address	t_{ADD}	35		35		45		ns	(Note 15)
Column address setup time	t_{ASC}	0		0		0		ns	
Address to SC high delay	t_{ASD}	55		60		75		ns	(Notes 16 and 18)
Row address setup time	t_{ASR}	0		0		0		ns	
Column address to $\overline{WE}$ delay	t_{AWD}	70		85		100		ns	(Note 7)
Access time from falling edge of $\overline{CAS}$	t_{CAC1}		20		25		30	ns	(Notes 3 and 4
Access time from $\overline{CAS}$, mask register read cycle	t_{CAC2}		30		35		40	ns	(Note 14)
Column address hold time	t_{CAH}	15		15		25		ns	
$\overline{CAS}$ pulse width	t_{CAS}	25	10,000	30	10,000	35	10,000	ns	
$\overline{DT}$ low hold time after $\overline{CAS}$ low	t_{CDH}	25		30		35		ns	(Note 15)
$\overline{CAS}$ before $\overline{RAS}$ refresh hold time	t_{CHR}	12		12		15		ns	

AC Characteristics (cont)

Parameter	Symbol	μPD42275-80 Min	μPD42275-80 Max	μPD42275-10 Min	μPD42275-10 Max	μPD42275-12 Min	μPD42275-12 Max	Unit	Test Conditions
Fast-page $\overline{CAS}$ precharge time	t_{CP}	10		10		15		ns	
$\overline{CAS}$ precharge time (nonpage cycle)	t_{CPN}	10		10		15		ns	
$\overline{CAS}$ to QSF delay time	t_{CQD}		70		70		100	ns	(Notes 16 and 19)
$\overline{CAS}$ high to $\overline{RAS}$ low precharge time	t_{CRP}	10		10		10		ns	(Note 12)
$\overline{CAS}$ low to SC high delay	t_{CSD}	45		55		65		ns	(Notes 16 and 18)
$\overline{CAS}$ hold time	t_{CSH}	80		100		120		ns	
$\overline{CAS}$ before $\overline{RAS}$ refresh setup time	t_{CSR}	0		0		0		ns	
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	45		55		65		ns	(Note 7)
Write command to $\overline{CAS}$ lead time	t_{CWL}	30		30		35		ns	
Data-in hold time	t_{DH}	15		20		25		ns	(Note 8)
$\overline{DT}$ high hold time	t_{DHH}	12		12		15		ns	
$\overline{DT}$ high setup time	t_{DHS}	0		0		0		ns	
$\overline{DT}$ low setup time	t_{DLS}	0		0		0		ns	
Propagation delay time from $\overline{DT}/\overline{OE}$ to QSF	t_{DQD}		35		35		55	ns	(Note 20)
Propagation delay time from $\overline{RAS}$ to QSF	t_{DQR}		45		55		70	ns	(Note 20)
Data-in setup time	t_{DS}	0		0		0		ns	(Note 8)
$\overline{DT}$ high pulse width	t_{DTP}	25		30		35		ns	
$\overline{DT}$ high to $\overline{RAS}$ high delay	t_{DTR}	0		0		0		ns	(Note 15)
DSF_1 hold time from $\overline{CAS}$	t_{FCH1}	15		15		25		ns	
DSF_1 setup time from $\overline{CAS}$	t_{FCS1}	0		0		0		ns	
DSF_1 hold time from $\overline{RAS}$	t_{FRH1}	12		12		15		ns	
DSF_2 hold time from $\overline{RAS}$	t_{FRH2}	12		12		15		ns	
DSF_1 setup time from $\overline{RAS}$	t_{FRS1}	0		0		0		ns	
DSF_2 setup time from $\overline{RAS}$	t_{FRS2}	0		0		0		ns	
Access time from $\overline{OE}$	t_{OEA}		20		25		30	ns	(Notes 3 and 4)
$\overline{OE}$ high to data-in setup delay	t_{OED}	20		25		30		ns	
$\overline{OE}$ high hold time after $\overline{WE}$ low	t_{OEH}	20		20		30		ns	
$\overline{OE}$ to $\overline{RAS}$ inactive setup time	t_{OES}	10		10		10		ns	
Output disable time from $\overline{OE}$ high	t_{OEZ}	0	20	0	25	0	30	ns	(Note 5)
Output disable time from $\overline{CAS}$ high	t_{OFF}	0	20	0	20	0	30	ns	(Note 5)
Fast-page cycle time	t_{PC}	50		60		70		ns	(Note 11)
Propagation delay time from SC to QSF	t_{PD}		25		25		40	ns	
Fast-page read-write/read-modify-write cycle time	t_{PRWC}	105		125		145		ns	(Note 11)
Access time from $\overline{RAS}$	t_{RAC}		80		100		120	ns	(Notes 3 and 4)
$\overline{RAS}$ to column address delay time	t_{RAD}	17		17		20		ns	(Note 9)
Row address hold time	t_{RAH}	12		12		15		ns	

AC Characteristics (cont)

Parameter	Symbol	μPD42275-80 Min	μPD42275-80 Max	μPD42275-10 Min	μPD42275-10 Max	μPD42275-12 Min	μPD42275-12 Max	Unit	Test Conditions
Column address to $\overline{RAS}$ lead time	t_{RAL}	45		55		65		ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10,000	100	10,000	120	10,000	ns	
Fast-page $\overline{RAS}$ pulse width	t_{RASP}	80	100,000	100	100,000	120	100,000	ns	
Random read or write cycle time	t_{RC}	160		180		220		ns	(Note 11)
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD1}	22	60	25	75	25	90	ns	(Note 4)
$\overline{RAS}$ to $\overline{CAS}$ delay time, mask register read cycle	t_{RCD2}	22	50	25	65	25	80	ns	(Note 14)
Read command hold time after $\overline{CAS}$ high	t_{RCH}	0		0		0		ns	(Note 6)
Read command setup time	t_{RCS}	0		0		0		ns	
$\overline{DT}$ low hold time after $\overline{RAS}$ low, serial port active	t_{RDH}	65		80		95		ns	(Note 15)
$\overline{DT}$ low hold time after $\overline{RAS}$ low, serial port in standby, split data transfer	t_{RDHS}	12		12		15		ns	(Notes 16 and 18)
Refresh interval	t_{REF}		8		8		8	ms	Addresses A_0 through A_8
$\overline{RAS}$ precharge time	t_{RP}	70		70		90		ns	
$\overline{RAS}$ high to $\overline{CAS}$ low precharge time	t_{RPC}	0		0		0		ns	
$\overline{RAS}$ to QSF delay time	t_{RQD}		105		120		155	ns	(Notes 16 and 19)
Read command hold time after $\overline{RAS}$ high	t_{RRH}	0		0		0		ns	(Note 6)
$\overline{RAS}$ low to SC high delay	t_{RSD}	85		105		125		ns	(Note 18)
$\overline{RAS}$ hold time	t_{RSH}	20		25		30		ns	
Read-write/read-modify-write cycle time	t_{RWC}	220		245		295		ns	(Note 11)
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	105		130		155		ns	(Note 7)
Write command to $\overline{RAS}$ lead time	t_{RWL}	30		30		35		ns	
Serial output access time from SC	t_{SCA}		25		25		40	ns	(Note 3)
Serial clock cycle time	t_{SCC}	25		30		40		ns	(Note 11)
SC pulse width	t_{SCH}	7		10		15		ns	
SC precharge time	t_{SCL}	7		10		15		ns	
SC high to $\overline{DT}$ high delay	t_{SDD}	5		5		5		ns	(Note 15)
SC low hold time after $\overline{DT}$ high	t_{SDH}	10		15		20		ns	(Note 15)
SC low hold time after $\overline{RAS}$ high	t_{SDHR}	25		30		40		ns	(Note 16)
Serial output access time from $\overline{SOE}$	t_{SOA}		20		25		30	ns	(Note 3)
$\overline{SOE}$ pulse width	t_{SOE}	7		10		15		ns	
Serial output hold time after SC high	t_{SOH}	5		7		7		ns	
$\overline{SOE}$ low to serial output setup delay	t_{SOO}	5		5		5		ns	
$\overline{SOE}$ precharge time	t_{SOP}	7		10		15		ns	

AC Characteristics (cont)

Parameter	Symbol	μPD42275-80 Min	μPD42275-80 Max	μPD42275-10 Min	μPD42275-10 Max	μPD42275-12 Min	μPD42275-12 Max	Unit	Test Conditions
Serial output disable time from $\overline{SOE}$ high	t_{SOZ}	0	10	0	15	0	20	ns	(Note 5)
SC high to $\overline{CAS}$ low delay	t_{SSC}	10		10		10		ns	(Notes 16 and 18)
Rise and fall transition time	t_T	3	50	3	50	3	50	ns	(Notes 3 and 10)
Write-per-bit hold time	t_{WBH}	12		12		15		ns	
Write-per-bit setup time	t_{WBS}	0		0		0		ns	
Write command hold time	t_{WCH}	15		20		25		ns	
Write command setup time	t_{WCS}	0		0		0		ns	(Note 7)
Write bit selection hold time	t_{WH}	12		12		15		ns	
Write command pulse width	t_{WP}	15		20		25		ns	(Note 13)
Write bit selection setup time	t_{WS}	0		0		0		ns	

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles, before proper device operation is achieved.

(3) See figures 3 and 4 for reference voltages and figures 5 and 6 for output loads.

(4) Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. The t_{RCD} (max) limit is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.

(5) An output disable time defines the time at which the output achieves the open-circuit condition and is not referenced to output voltage levels.

(6) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(7) t_{WCS}, t_{CWD}, and t_{RWD} are restrictive operating parameters in read-write and read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data output will remain open-circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the condition of the data output (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

(8) These parameters are referenced to the falling edge of $\overline{CAS}$ in early write cycles and to the falling edge of (WB/)$\overline{WE}$ in delayed write or read-modify-write cycles.

(9) Assumes that t_{RAD} (min) = t_{RAH} (min) + typical t_T of 5 ns.

(10) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Additionally, transition times are measured between V_{IH} and V_{IL}.

(11) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(12) The t_{CRP} requirement is applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceded by any cycle.

(13) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write operation, both t_{WCS} and t_{WCH} must be met.

(14) Only for mask register read operation during register read cycles.

(15) For real-time data transfer operation (data transfer with $\overline{SC}$ active).

(16) For read data transfers with serial port in standby.

(17) Ac measurements assume t_T = 5 ns.

(18) For split data transfer cycles.

(19) If $t_{CDH} \leq t_{CDH}$ (min) or $t_{RDHS} \leq t_{RDH}$ (min), then the delay time for the switching of QSF is determined by t_{RQD} or t_{CQD}, whichever occurs later.

(20) If $t_{CDH} \geq t_{CDH}$ (min) and $t_{RDHS} \geq t_{RDH}$ (min), then the switching delay time of QSF is determined by t_{DQD} or t_{DQR}, whichever occurs first.

Figure 3. Input Timing

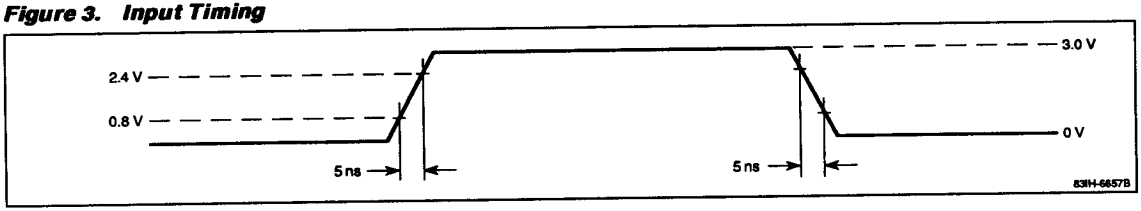

Figure 4. Output Timing

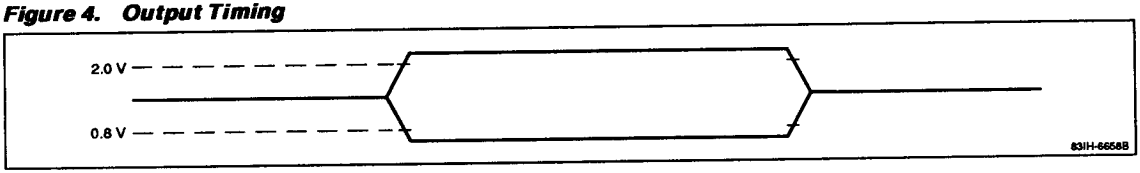

Figure 5. Output Load in Random Access Port

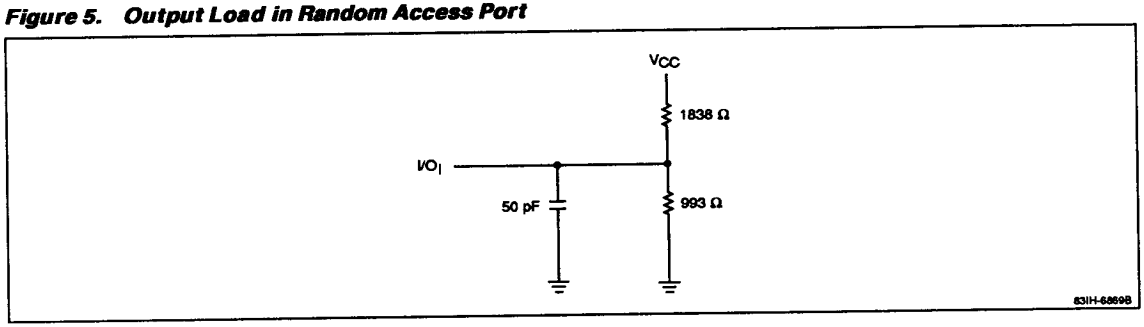

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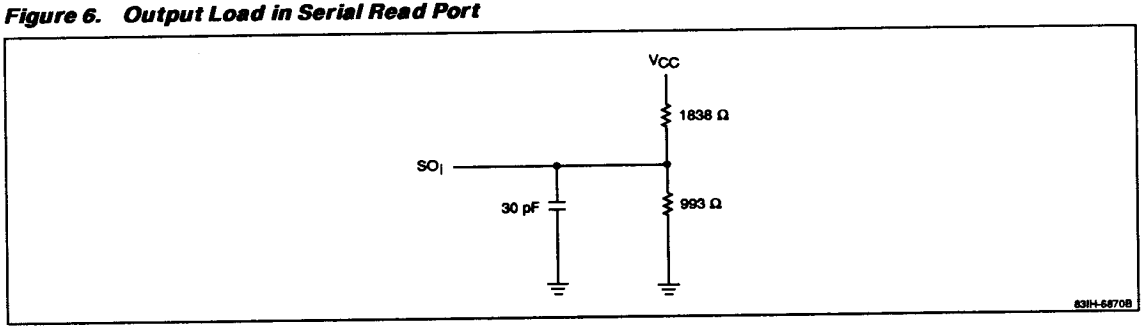
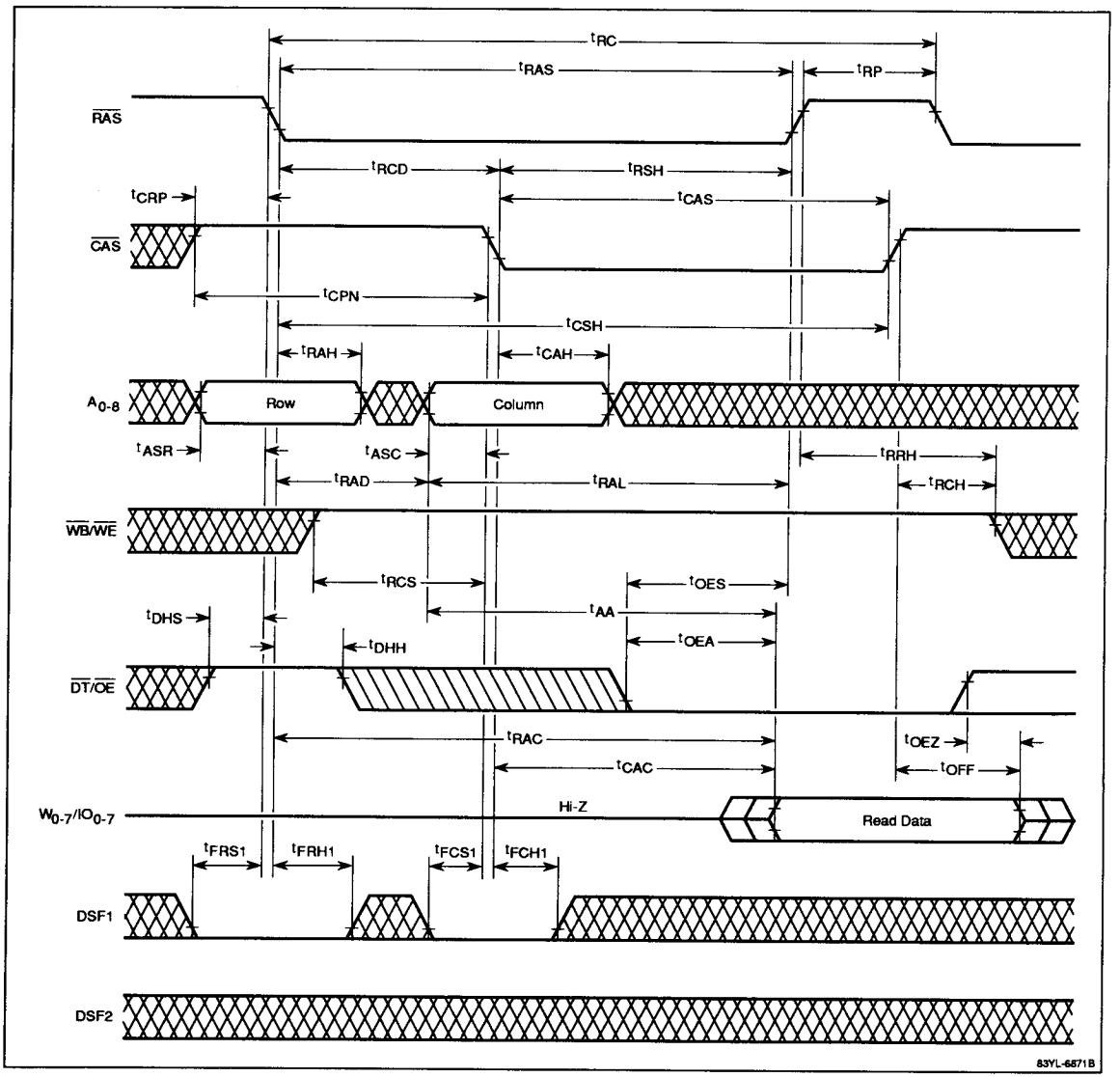
Figure 6. Output Load in Serial Read Port



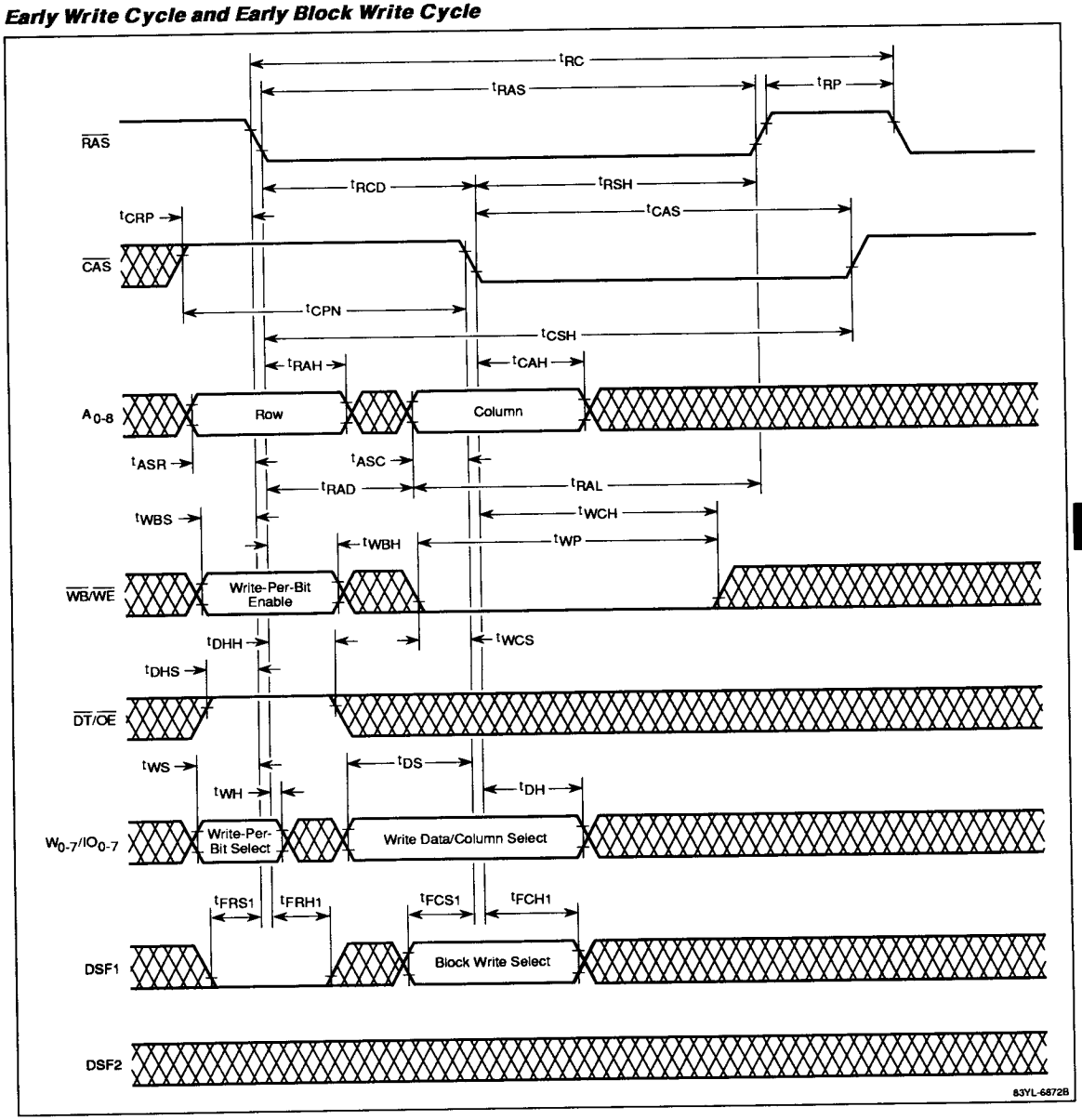
Timing Waveforms

Read Cycle



Timing Waveforms (cont)

Early Write Cycle and Early Block Write Cycle



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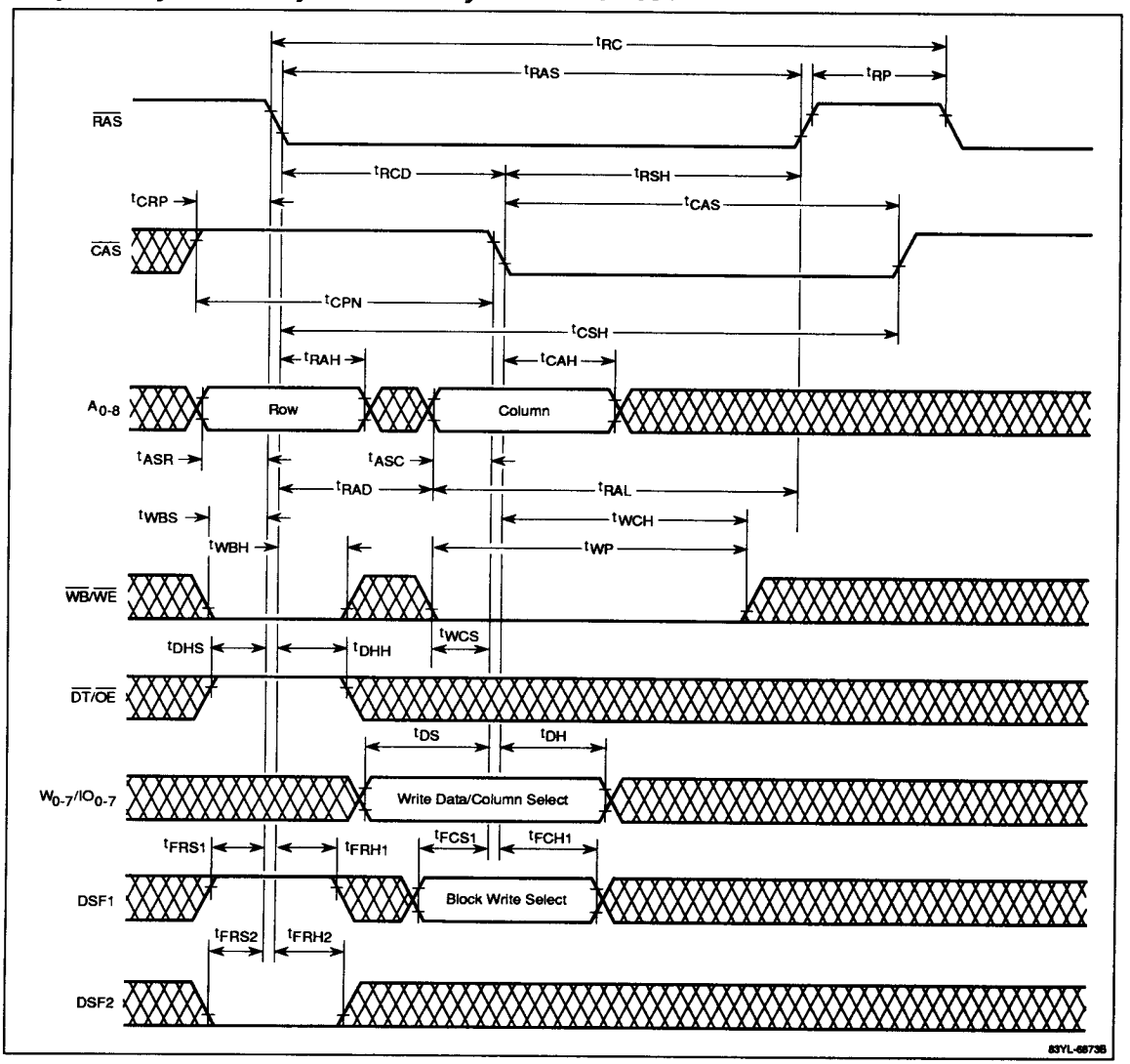
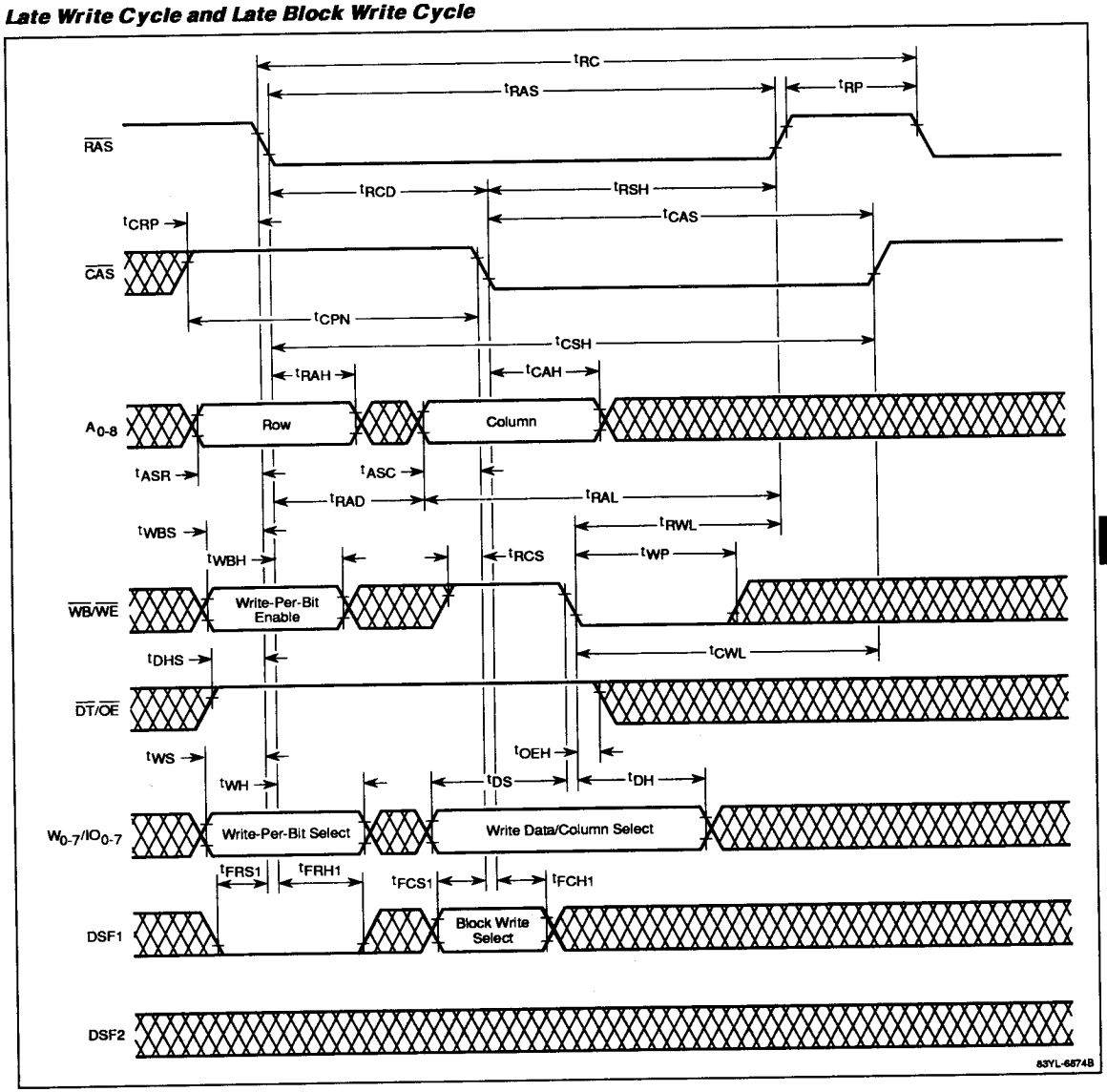
Timing Waveforms (cont)

Early Write Cycle and Early Block Write Cycle With Old Mask



Timing Waveforms (cont)

Late Write Cycle and Late Block Write Cycle



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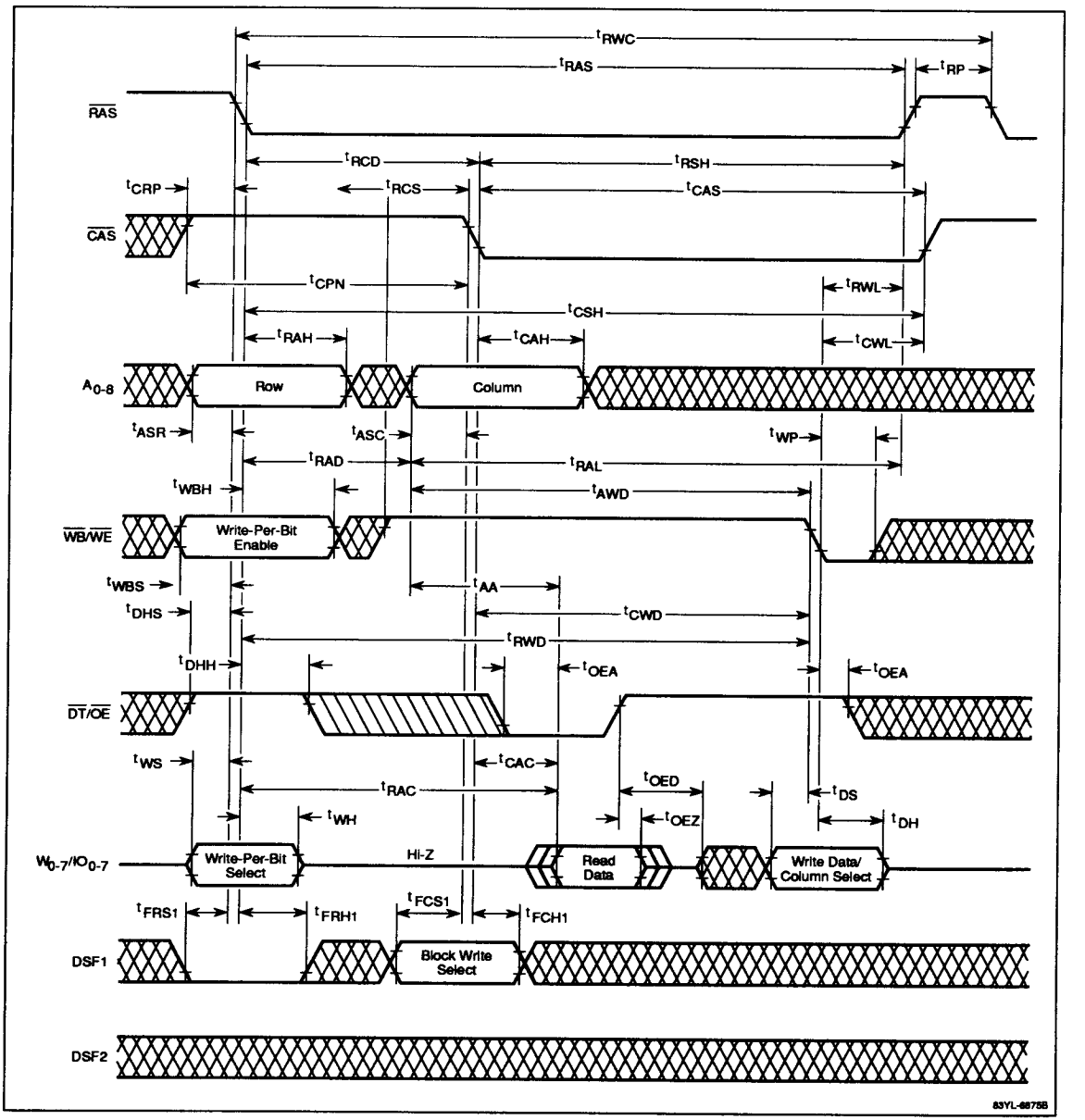
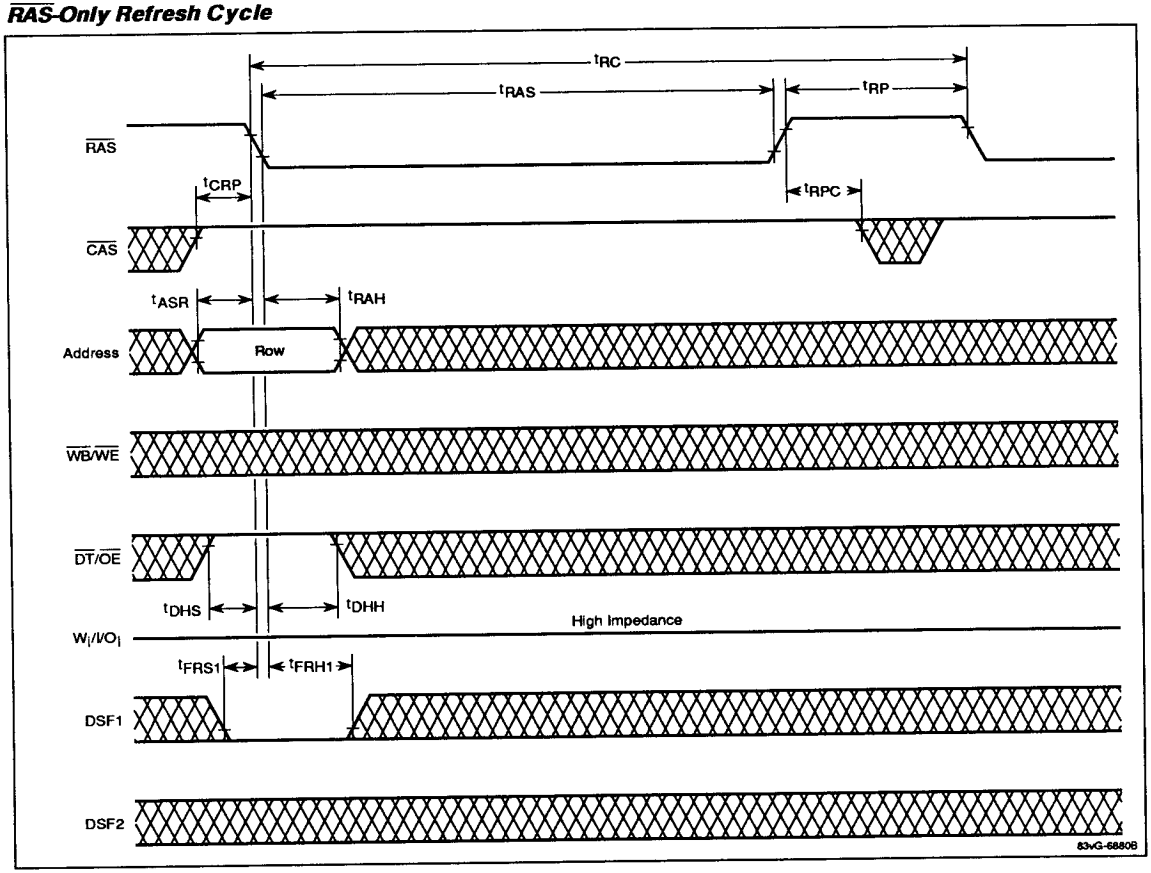
Timing Waveforms (cont)

Read-Write/Read-Modify-Write Cycle



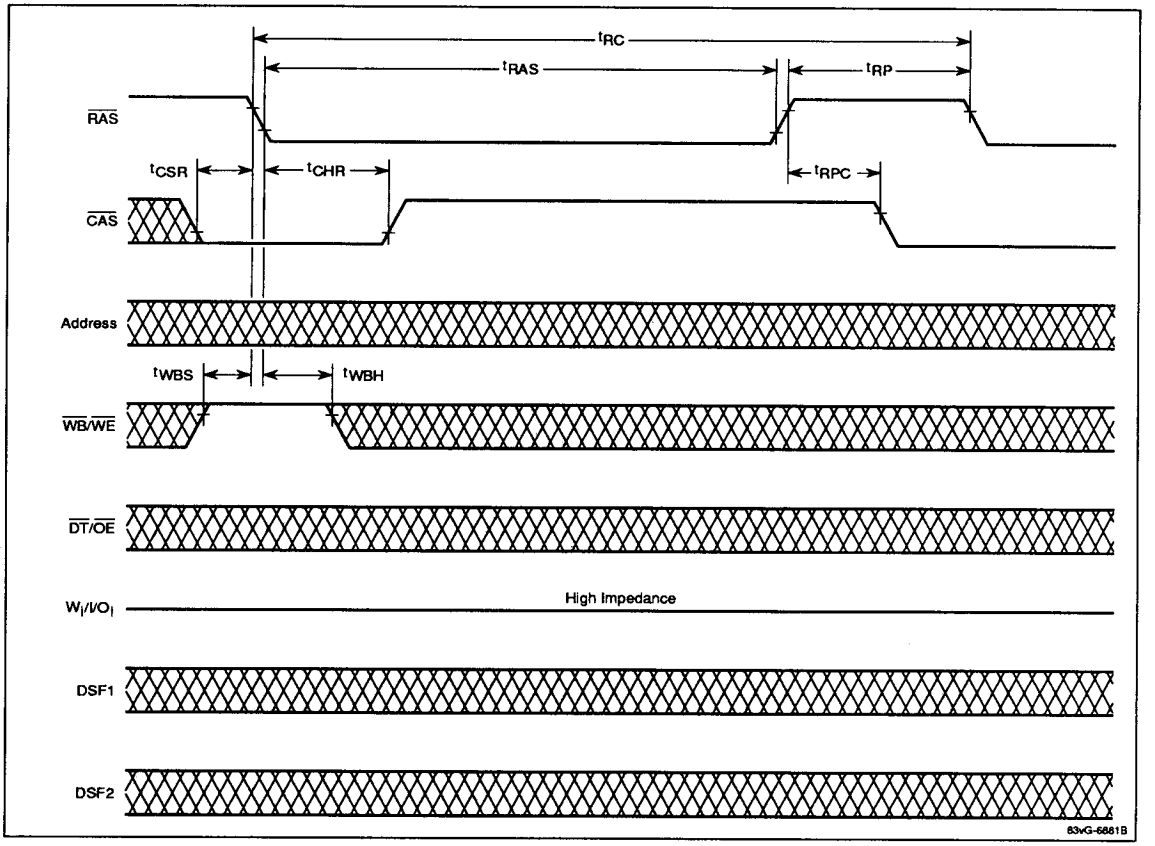
Timing Waveforms (cont)

RAS-Only Refresh Cycle



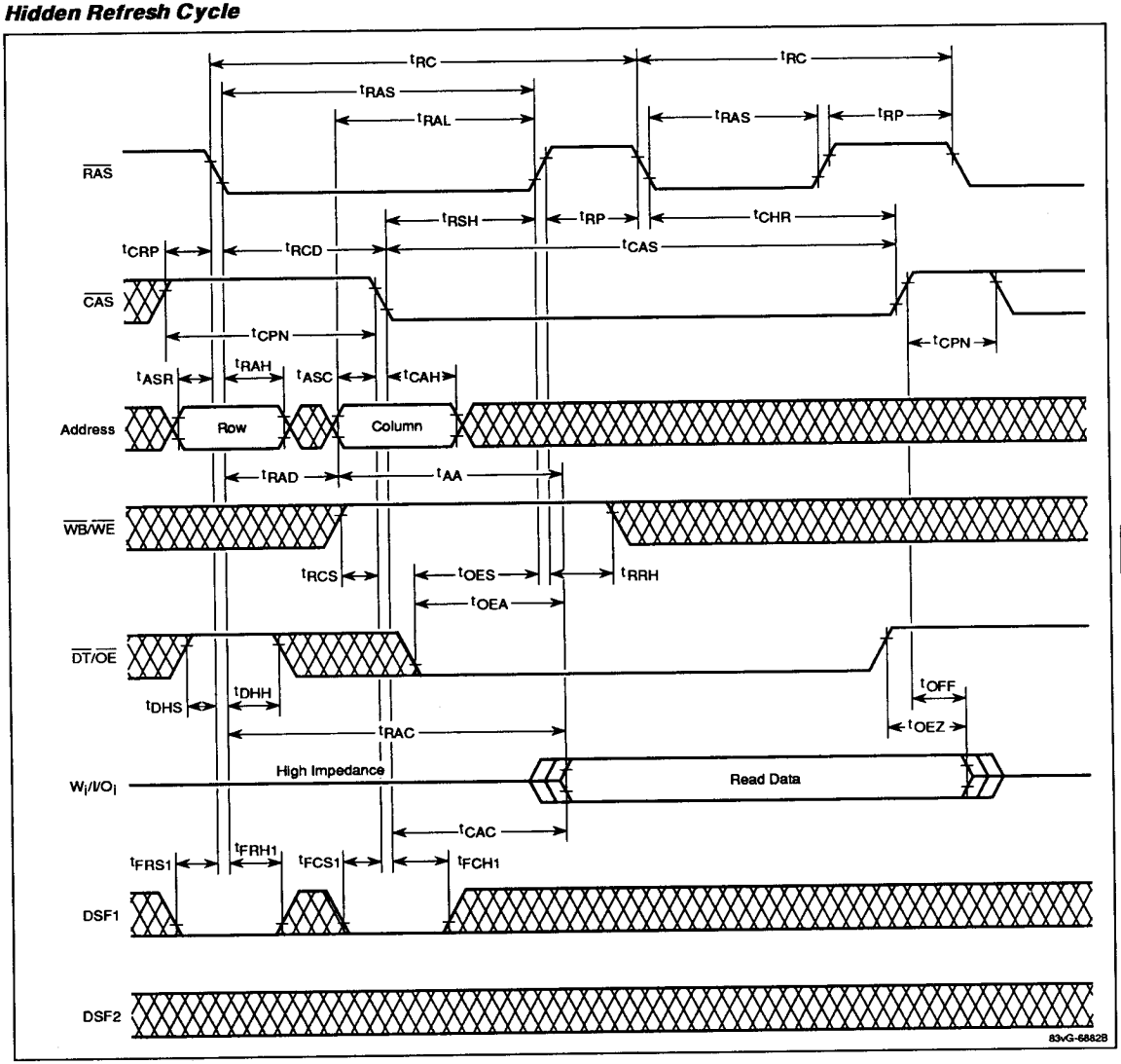
Timing Waveforms (cont)

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Timing Waveforms (cont)

Hidden Refresh Cycle



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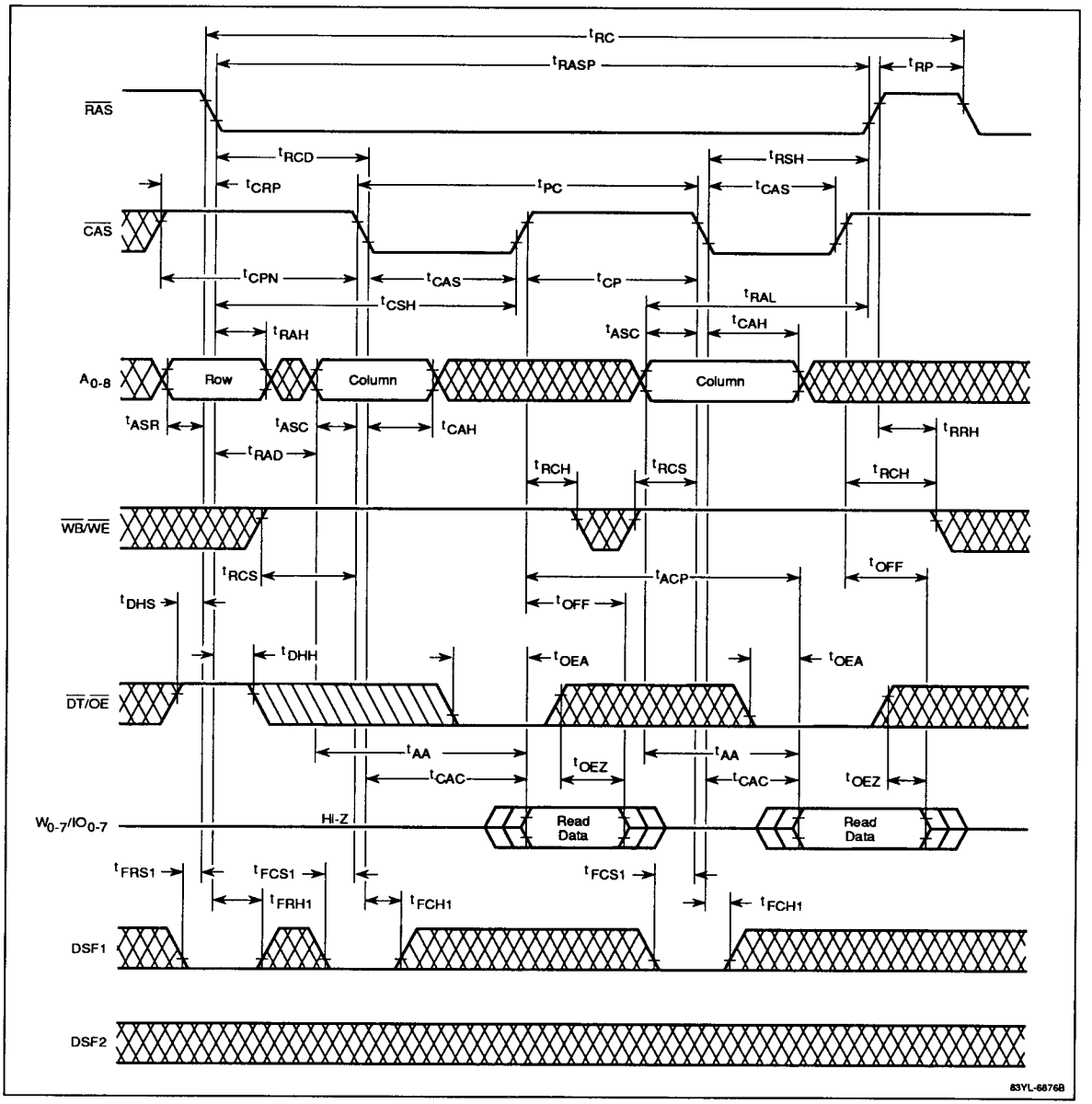
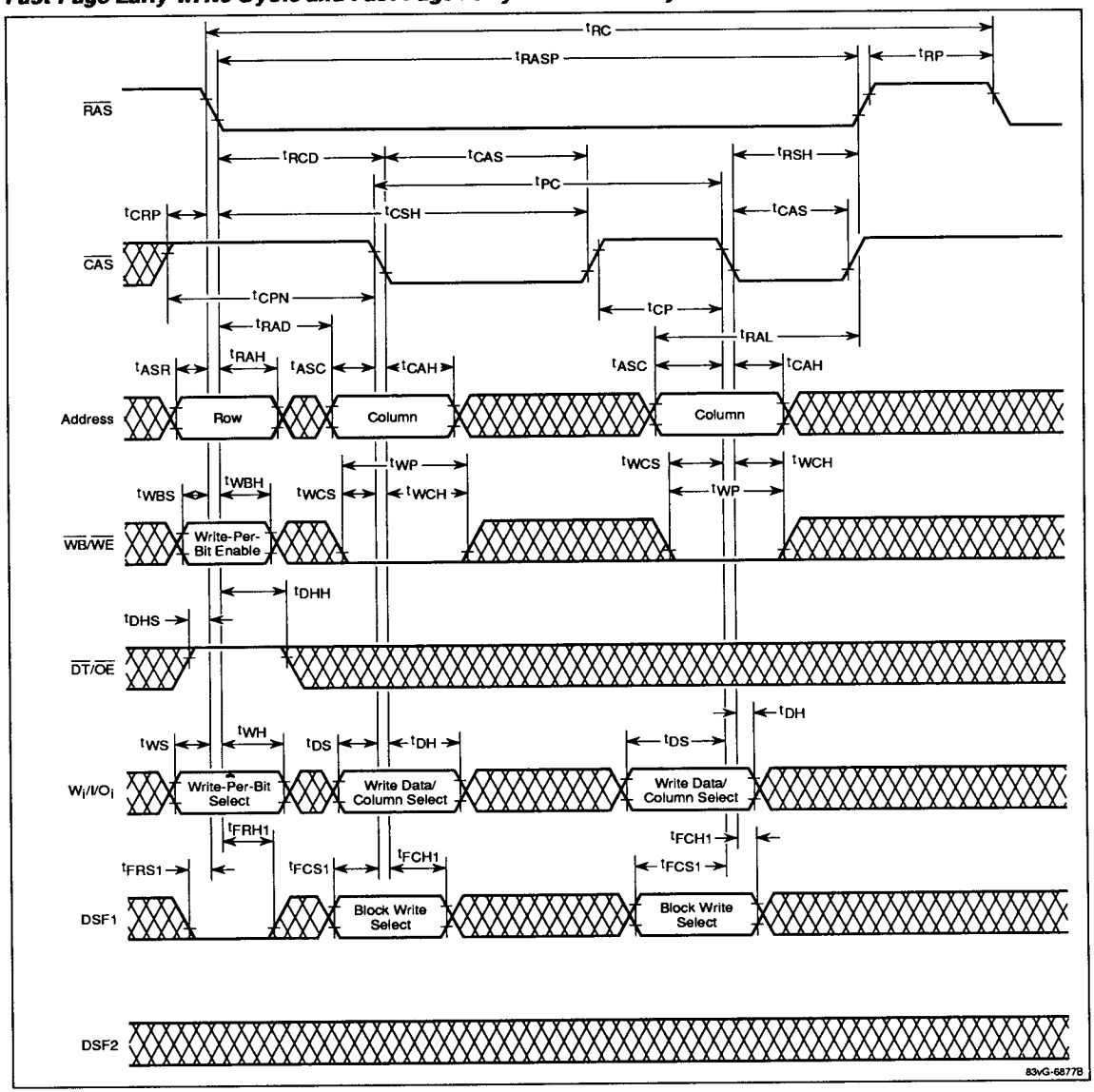
Timing Waveforms (cont)

Fast-Page Read Cycle



Timing Waveforms (cont)

Fast-Page Early Write Cycle and Fast-Page Early Block Write Cycle



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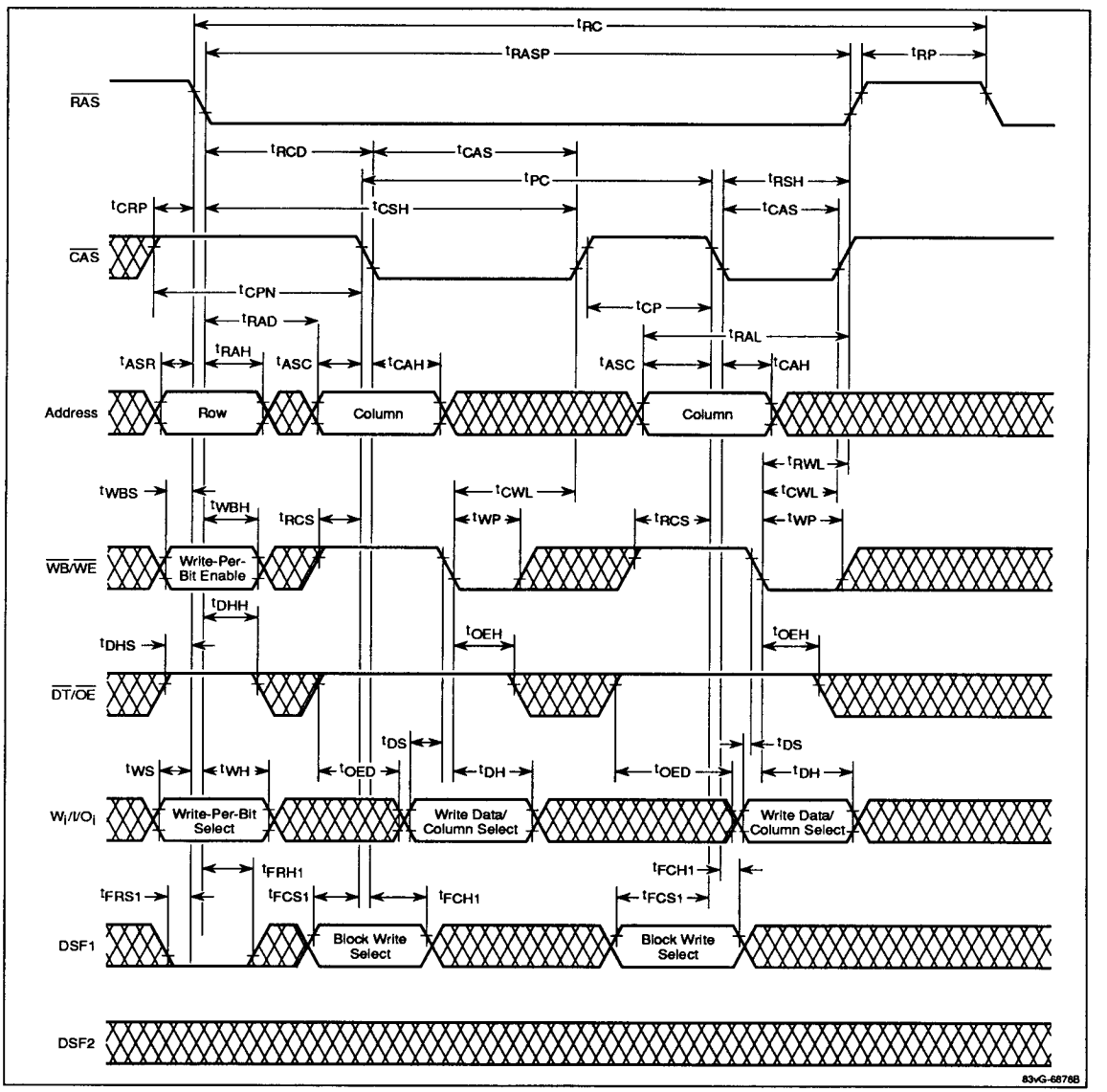
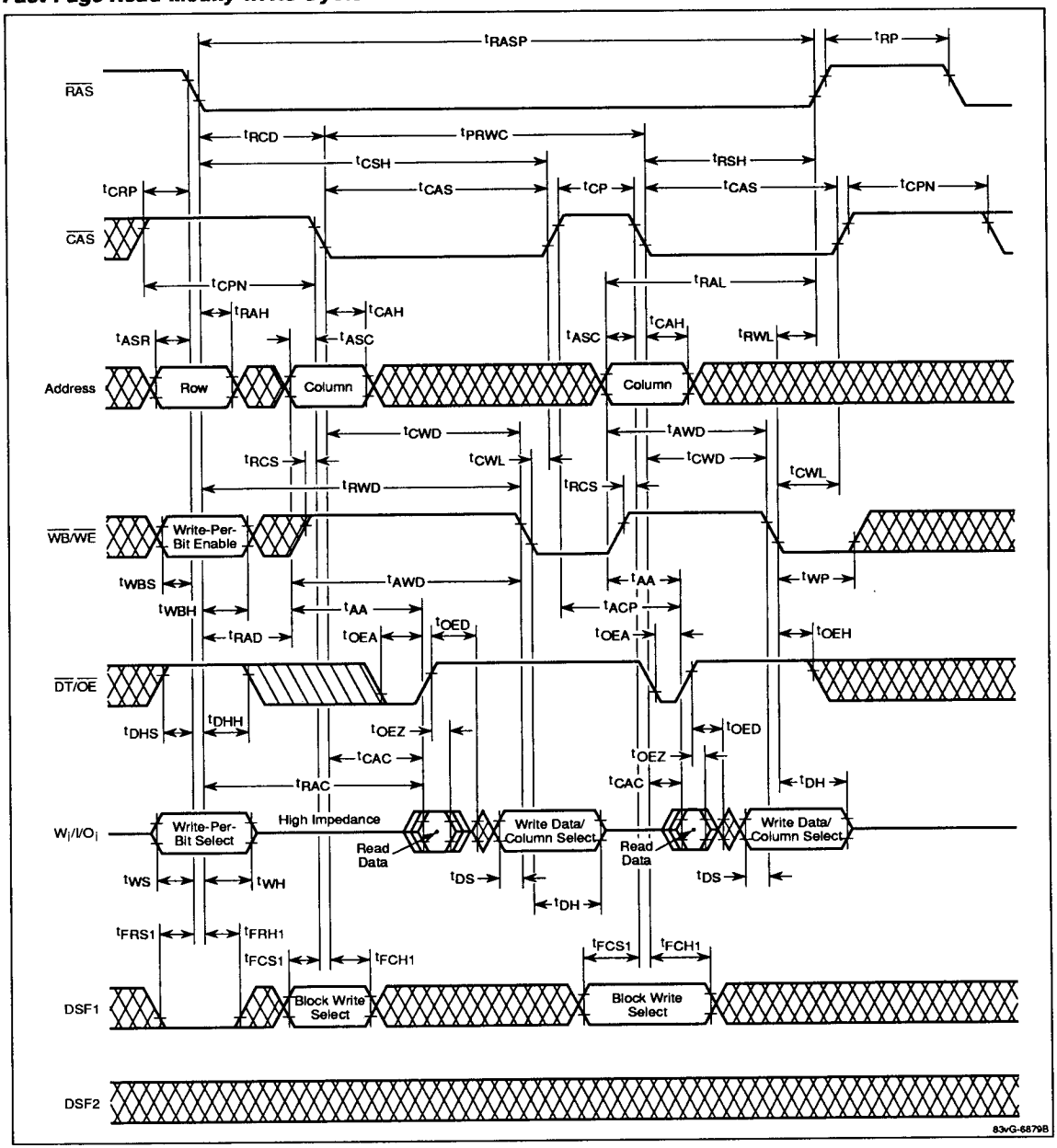
Timing Waveforms (cont)

Fast-Page Late Write Cycle and Fast-Page Late Block Write Cycle



Timing Waveforms (cont)

Fast-Page Read-Modify-Write Cycle



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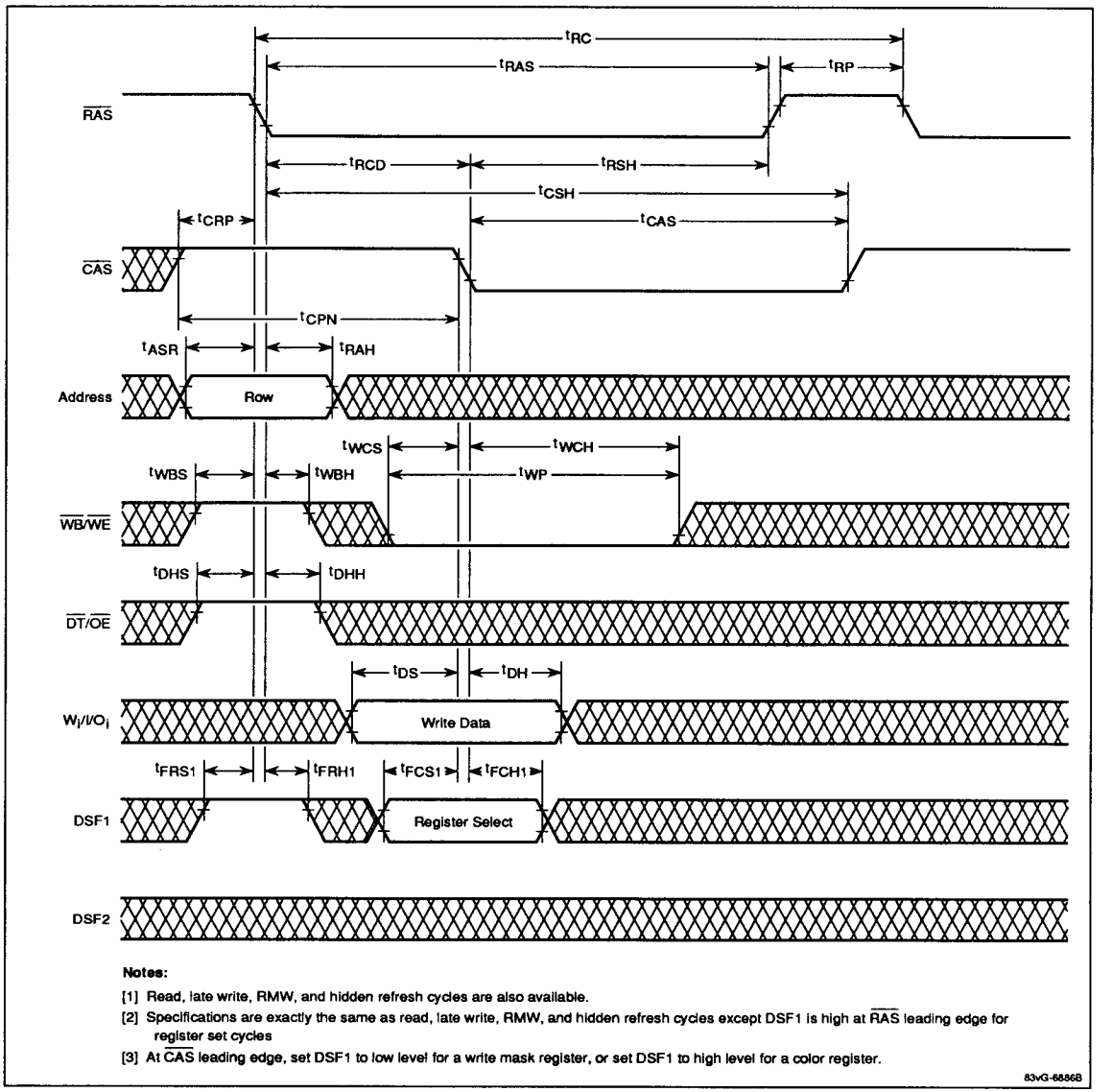
Timing Waveforms (cont)

Color Register Set Cycle



Notes:

[1] Read, late write, RMW, and hidden refresh cycles are also available.

[2] Specifications are exactly the same as read, late write, RMW, and hidden refresh cycles except DSF1 is high at $\overline{RAS}$ leading edge for register set cycles

[3] At $\overline{CAS}$ leading edge, set DSF1 to low level for a write mask register, or set DSF1 to high level for a color register.

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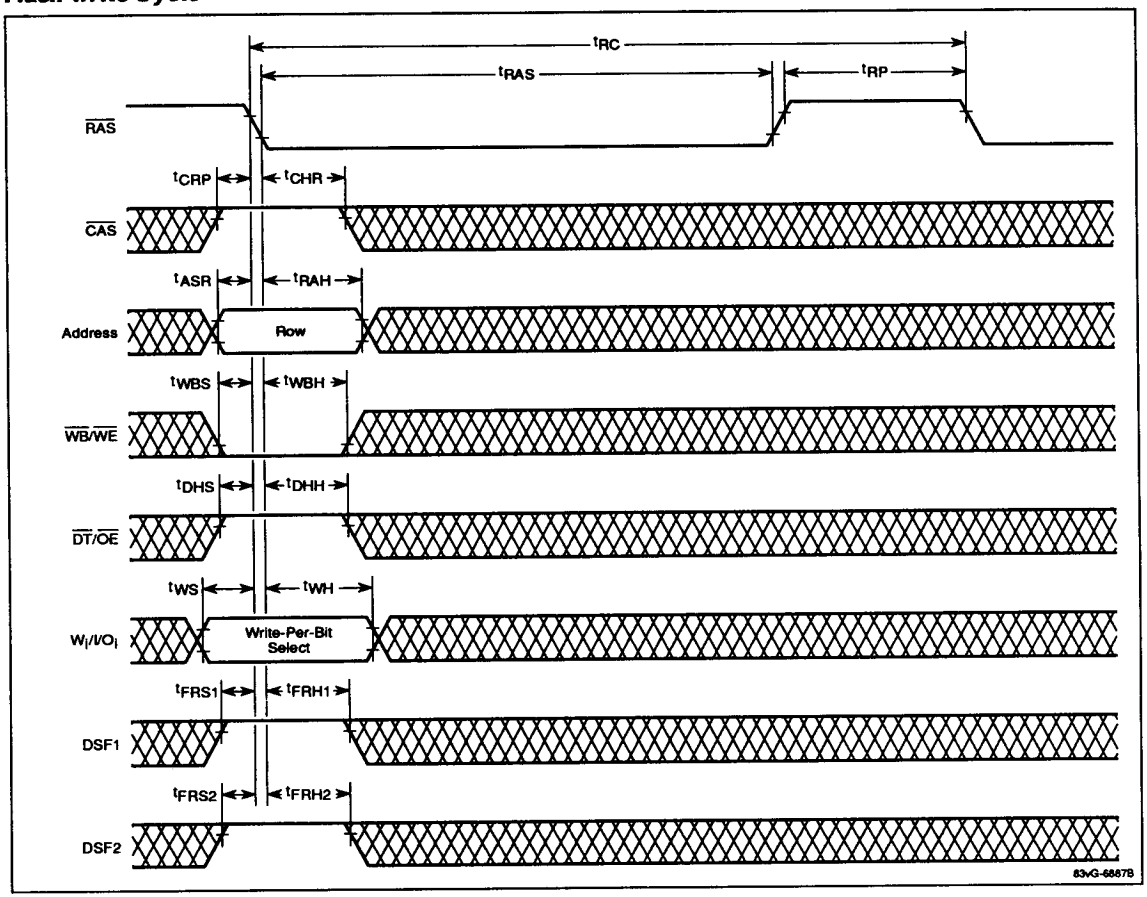
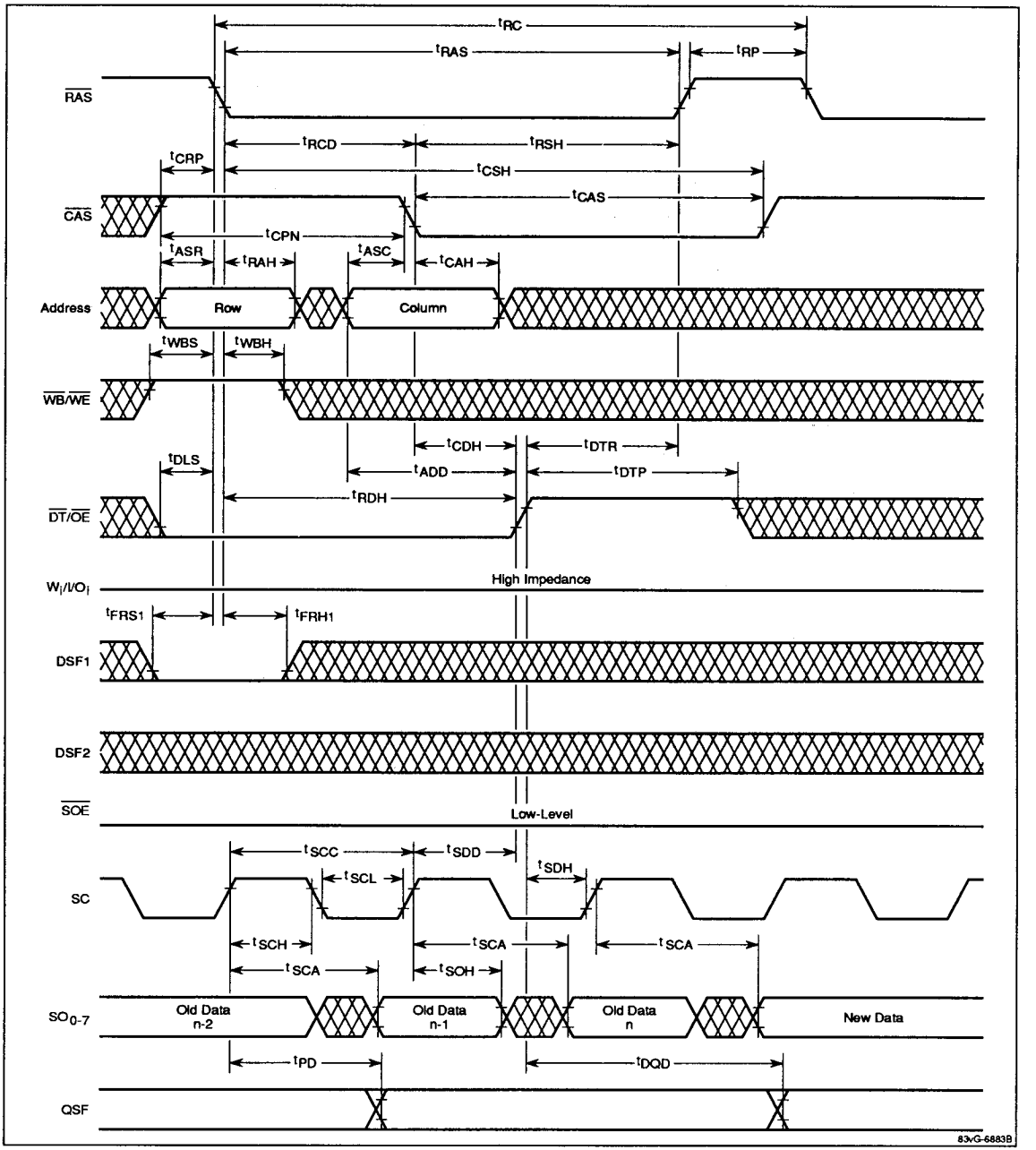
Timing Waveforms (cont)

Flash Write Cycle



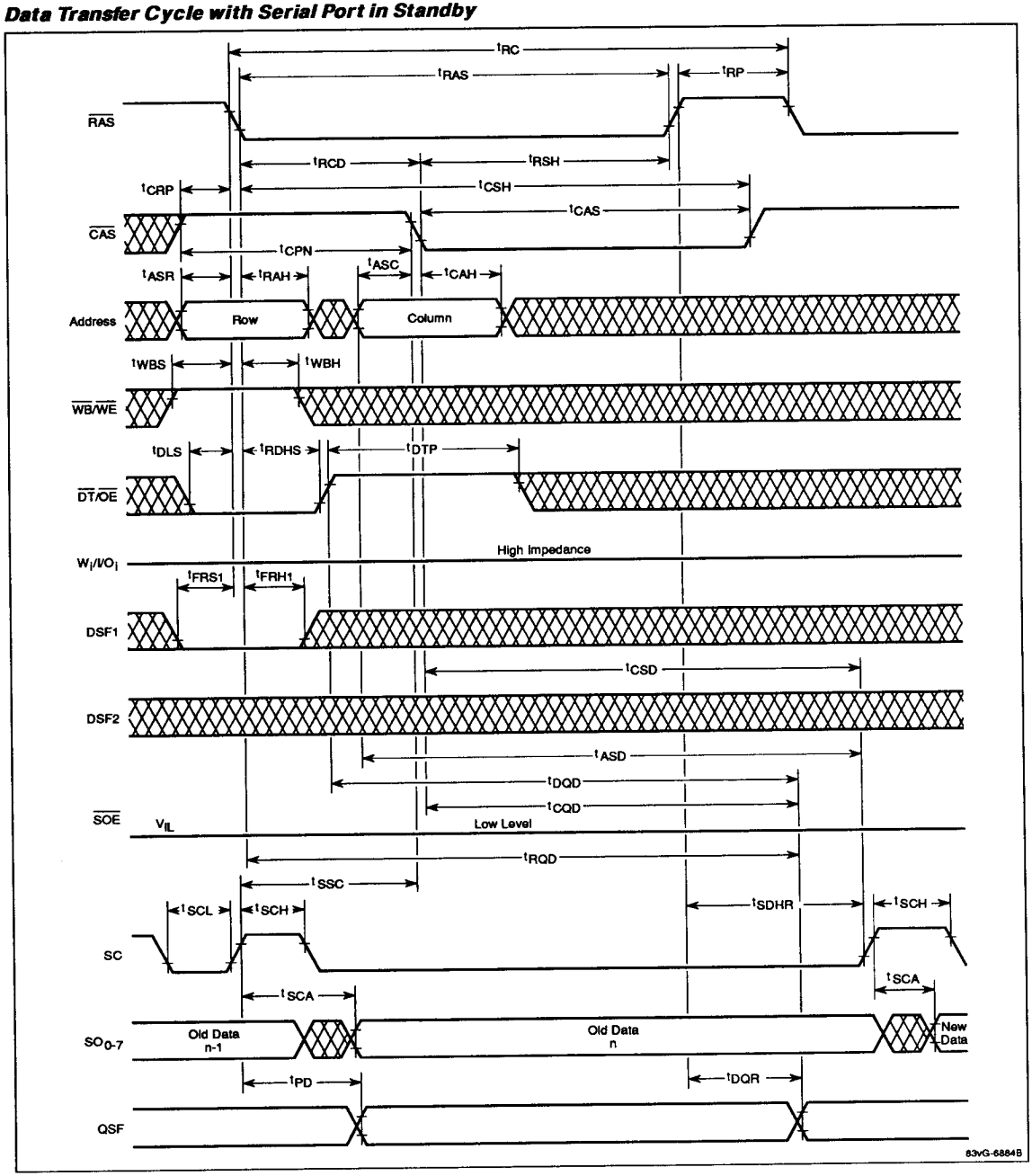
Timing Waveforms (cont)

Data Transfer Cycle with Serial Port Active



Timing Waveforms (cont)

Data Transfer Cycle with Serial Port in Standby



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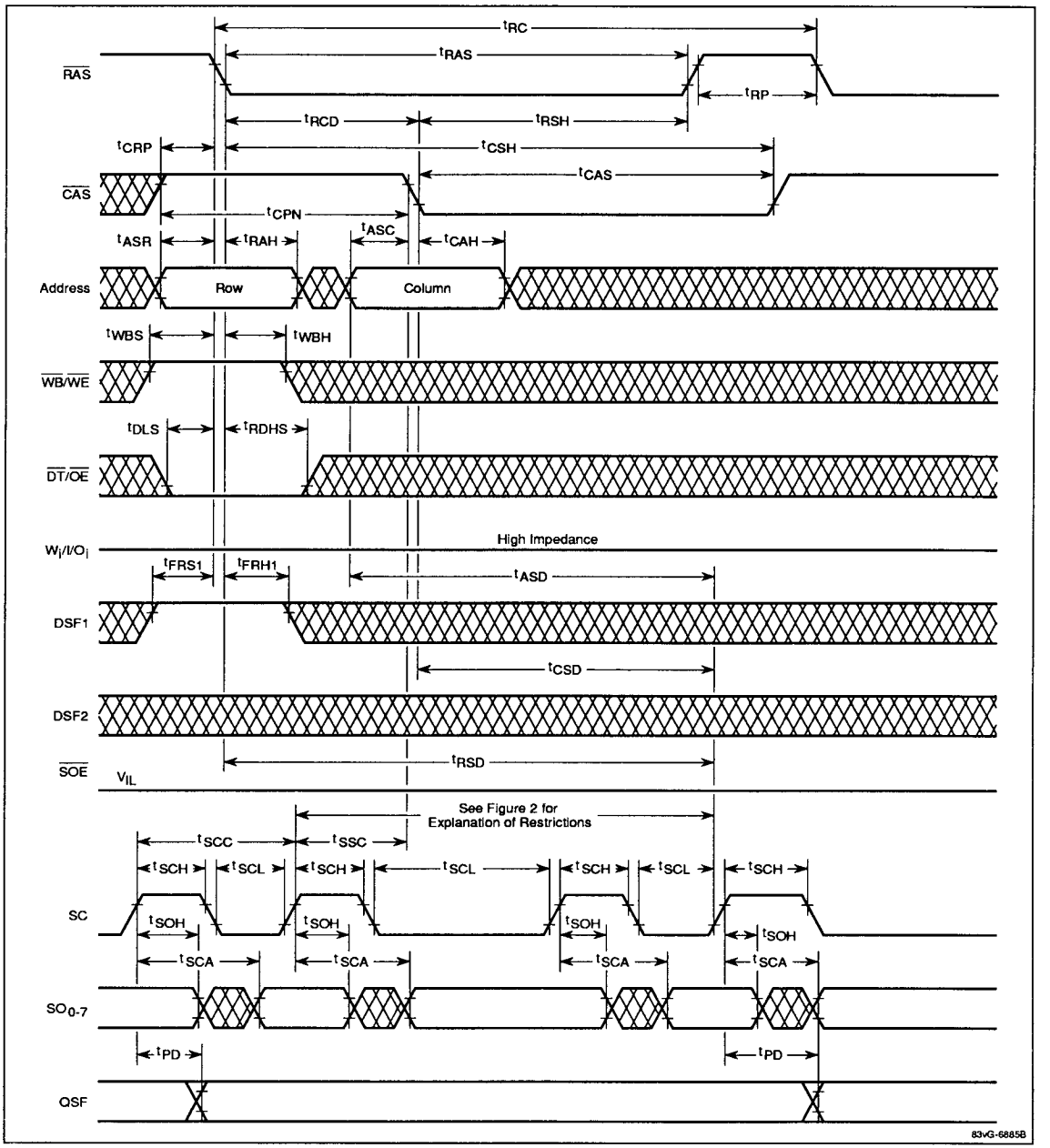
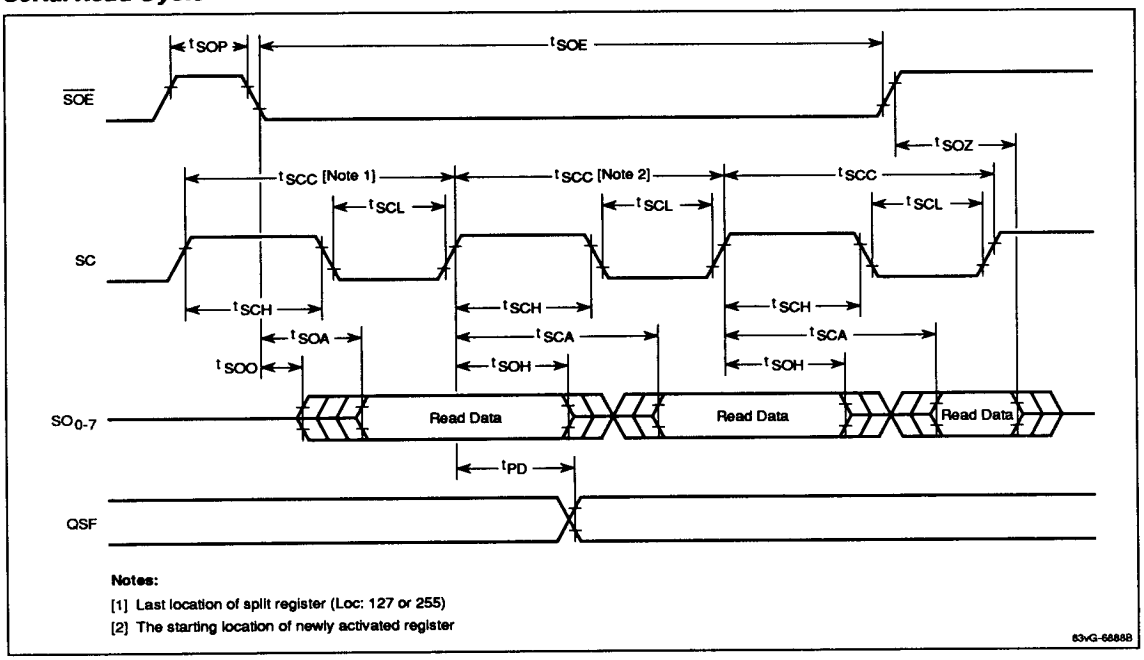
Timing Waveforms (cont)

Split Read Data Transfer Cycle



Timing Waveforms (cont)

Serial Read Cycle



Notes:

[1] Last location of split register (Loc: 127 or 255)

[2] The starting location of newly activated register

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