μPD4216101, 4217101
16,777,216 x 1-Bit
Dynamic CMOS RAM

Advance Information

Description

The μPD4216101 and the μPD4217101 are nibble-mode dynamic RAMs organized as 16,777,216 words by 1 bit and designed to operate from a single +5-volt power supply. Advanced polycide technology minimizes silicon area and provides high storage cell capacity, high performance, and high reliability. A single-transistor dynamic storage cell and advanced CMOS circuitry throughout ensure minimum power dissipation, while an on-chip circuit internally generates the negative-voltage substrate bias—automatically and transparently.

The three-state output is controlled by $\overline{CAS}$ independent of $\overline{RAS}$. After a valid read or read-modify-write cycle, data is held on the output by holding $\overline{CAS}$ low. The data output is returned to high impedance by returning $\overline{CAS}$ high. Nibble-mode read and write cycles can be executed by cycling $\overline{CAS}$.

Refreshing may be accomplished by a $\overline{CAS}$ before $\overline{RAS}$ cycle that internally generates the refresh address. Refreshing can also be accomplished by $\overline{RAS}$-only refresh cycles or by normal read or write cycles.

Two versions of the 16,777,216 by 1-bit nibble-mode dynamic RAM are available. The μPD4216101 version uses 4096 address combinations of A_0 - A_{11} to refresh the memory during a 64-ms refresh period. The μPD4217101 version uses 2048 address combinations of A_0 - A_{10} to refresh the memory during a 32-ms refresh period.

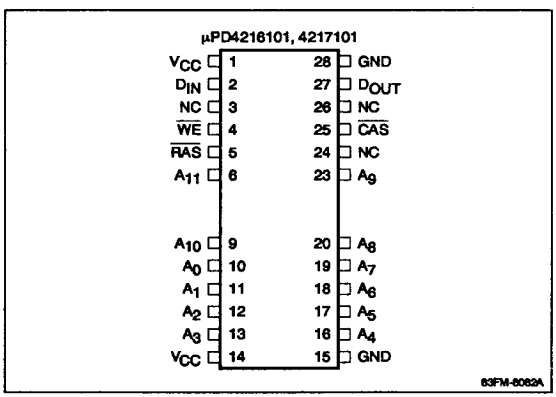
Both versions use row and column address combinations of A_0 - A_{11} for accessing the memory during read, write, and read-modify-write cycles.

Features

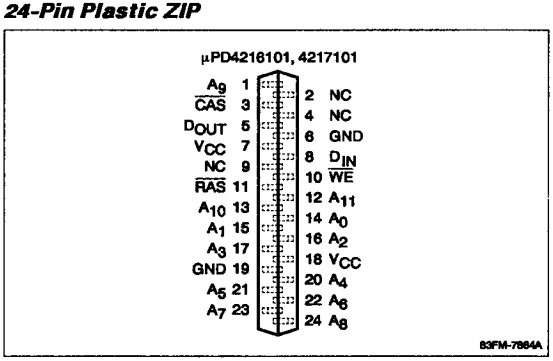
- 16,777,216 by 1-bit organization
- Single +5-volt power supply
- Nibble-mode option
- Low power dissipation
- $\overline{CAS}$ before $\overline{RAS}$ refresh cycles
- Multiplexed address inputs
- On-chip substrate bias generator
- TTL-compatible inputs and outputs
- Nonlatched, three-state outputs
- Low input capacitance
- 4K refresh cycles every 64 ms (4216101); 2K refresh cycles every 32 ms (4217101)
- 28/24-pin SOJ (400 mil), 24-pin ZIP (475 mil), and 28/24-pin TSOP plastic packaging

Pin Configurations

28/24-Pin Plastic SOJ



24-Pin Plastic ZIP



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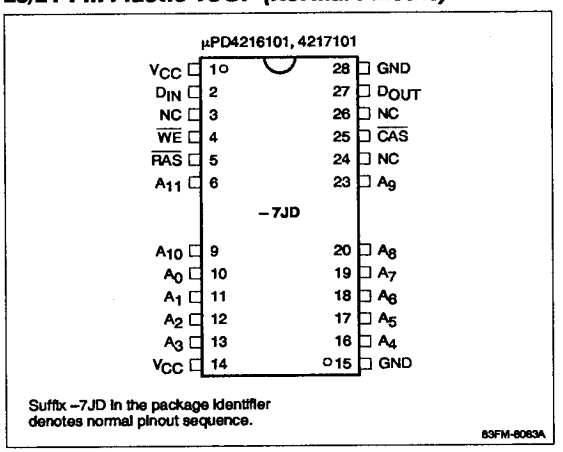
Contact your NEC sales representative for complete data sheet and product availability.

Pin Configurations (cont)

28/24-Pin Plastic TSOP (Normal Pinouts)



Suffix –7JD in the package identifier denotes normal pinout sequence.

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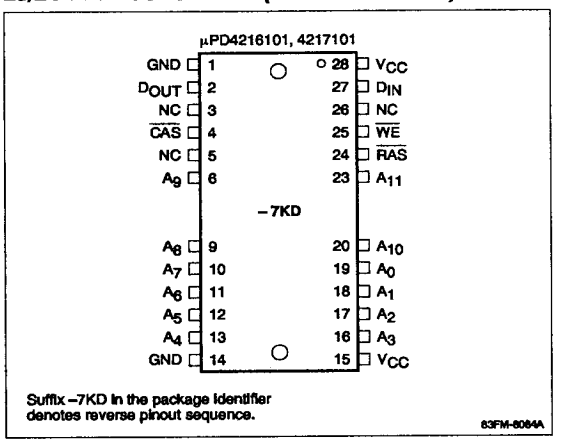
28/24-Pin Plastic TSOP (Reverse Pinouts)



Suffix –7KD in the package identifier denotes reverse pinout sequence.

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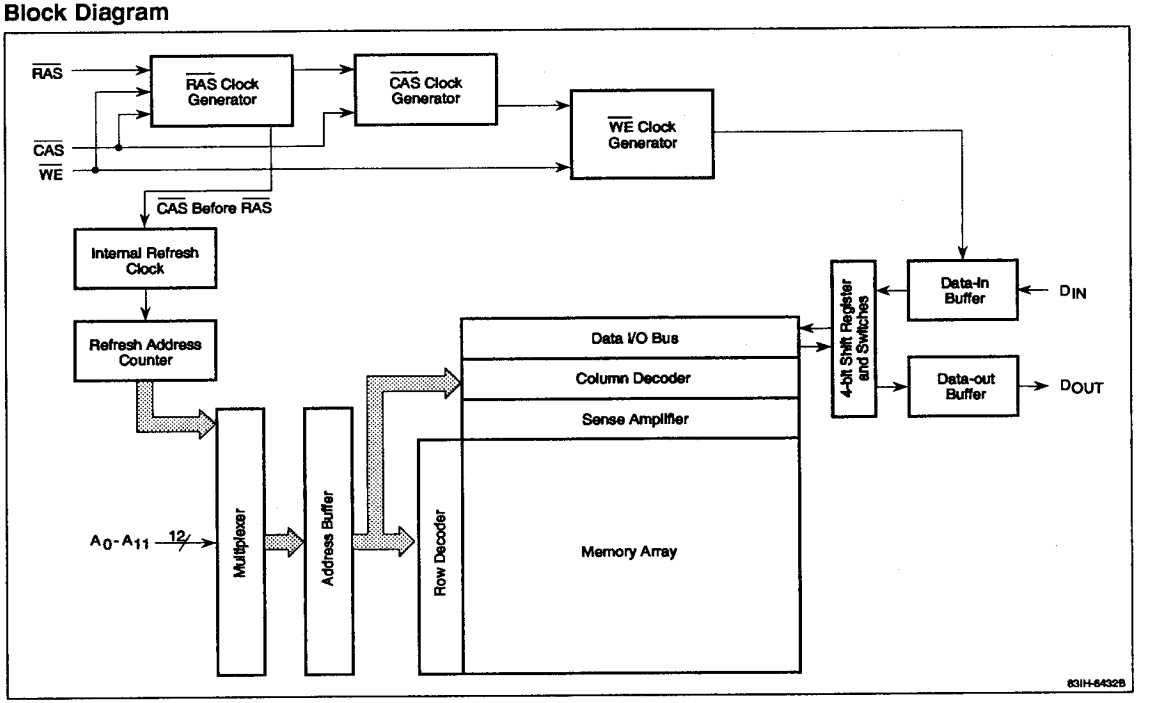
Block Diagram



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Ordering Information, μPD4216101 (4K refresh cycles)

Part Number	$\overline{RAS}$ Access Time (max)	R/W Cycle Time (max)	Nibble-Mode Cycle (max)	Package
μPD4216101LE-60	60 ns	110 ns	40 ns	28/24-pin plastic SOJ (400 mil)
LE-70	70 ns	130 ns	40 ns	
LE-80	80 ns	150 ns	40 ns	
LE-10	100 ns	180 ns	45 ns	
μPD4216101V-60	60 ns	110 ns	40 ns	24-pin plastic ZIP
V-70	70 ns	130 ns	40 ns	
V-80	80 ns	150 ns	40 ns	
V-10	100 ns	180 ns	45 ns	
μPD4216101G5-60	60 ns	110 ns	40 ns	28/24-pin plastic TSOP (normal pinouts)
G5-70	70 ns	130 ns	40 ns	
G5-80	80 ns	150 ns	40 ns	
G5-10	100 ns	180 ns	45 ns	
μPD4216101G5M-60	60 ns	110 ns	40 ns	28/24-pin plastic TSOP (reverse pinouts)
G5M-70	70 ns	130 ns	40 ns	
G5M-80	80 ns	150 ns	40 ns	
G5M-10	100 ns	180 ns	45 ns	

Ordering Information, μPD4217101 (2K refresh cycles)

Part Number	$\overline{RAS}$ Access Time (max)	R/W Cycle Time (max)	Nibble-Mode Cycle (max)	Package
μPD4217101LE-60	60 ns	110 ns	40 ns	28/24-pin plastic SOJ (400 mil)
LE-70	70 ns	130 ns	40 ns	
LE-80	80 ns	150 ns	40 ns	
LE-10	100 ns	180 ns	45 ns	
μPD4217101V-60	60 ns	110 ns	40 ns	24-pin plastic ZIP
V-70	70 ns	130 ns	40 ns	
V-80	80 ns	150 ns	40 ns	
V-10	100 ns	180 ns	45 ns	
μPD4217101G5-60	60 ns	110 ns	40 ns	28/24-pin plastic TSOP (normal pinouts)
G5-70	70 ns	130 ns	40 ns	
G5-80	80 ns	150 ns	40 ns	
G5-10	100 ns	180 ns	45 ns	
μPD4217101G5M-60	60 ns	110 ns	40 ns	28/24-pin plastic TSOP (reverse pinouts)
G5M-70	70 ns	130 ns	40 ns	
G5M-80	80 ns	150 ns	40 ns	
G5M-10	100 ns	180 ns	45 ns	