



# HY57V283220(L)T(P)/ HY5V22(L)F(P) 4 Banks x 1M x 32Bit Synchronous DRAM

## Revision History

Revision No.	History	Remark
0.1	Defined Preliminary Specification	
0.2	1) Modified FBGA Ball Configuration Typo. 2) Changed Functional Block Diagram from A10 to A11. 3) Changed VDD min from 3.0V to 3.135V. 4) Changed Cap. Value from C11, 3, 5 to 4pf & C12, 3.8 to 4pf. 5) Insert tAC2 Value. 6) Insdrtr tRAS & CLK Value.	
0.3	Defined IDD Spec.	
0.4	Delited Preliminary.	
0.5	Changed IDD Spec.	
0.6	133MHz Speed Added	
0.7	Changed FBGA Package Size from 11x13 to 8x13.	
0.8	1) Changed VDD min from 3.135V to 3.0V. 2) Changed VIL min from VSSQ-0.3V to -0.3V.	
0.9	Modified of size erra. (Page15) (Equation : $13.00 \pm 10$ -> $13.00 \pm 0.10$ )	



# HY57V283220(L)T(P)/ HY5V22(L)F(P) 4 Banks x 1M x 32Bit Synchronous DRAM

## DESCRIPTION

The Hynix HY57V283220(L)T(P) / HY5V22(L)F(P) is a 134,217,728-bit CMOS Synchronous DRAM, ideally suited for the memory applications which require wide data I/O and high bandwidth. HY57V283220(L)T(P) / HY5V22(L)F(P) is organized as 4banks of 1,048,576x32.

HY57V283220(L)T(P) / HY5V22(L)F(P) is offering fully synchronous operation referenced to a positive edge of the clock. All inputs and outputs are synchronized with the rising edge of the clock input. The data paths are internally pipelined to achieve very high bandwidth. All input and output voltage levels are compatible with LVTTTL.

Programmable options include the length of pipeline (Read latency of 2 or 3), the number of consecutive read or write cycles initiated by a single control command (Burst length of 1,2,4,8 or full page), and the burst count sequence(sequential or interleave). A burst of read or write cycles in progress can be terminated by a burst terminate command or can be interrupted and replaced by a new burst read or write command on any cycle. (This pipelined design is not restricted by a `2N` rule.)

## FEATURES

- JEDEC standard 3.3V power supply
- All device pins are compatible with LVTTTL interface
- 86TSOP-II, 90Ball FBGA with 0.8mm of pin pitch
- All inputs and outputs referenced to positive edge of system clock
- Data mask function by DQM0,1,2 and 3
- Internal four banks operation
- Auto refresh and self refresh
- 4096 refresh cycles / 64ms
- Programmable Burst Length and Burst Type
  - 1, 2, 4, 8 or full page for Sequential Burst
  - 1, 2, 4 or 8 for Interleave Burst
- Programmable  $\overline{\text{CAS}}$  Latency ; 2, 3 Clocks
- Burst Read Single Write operation

## ORDERING INFORMATION

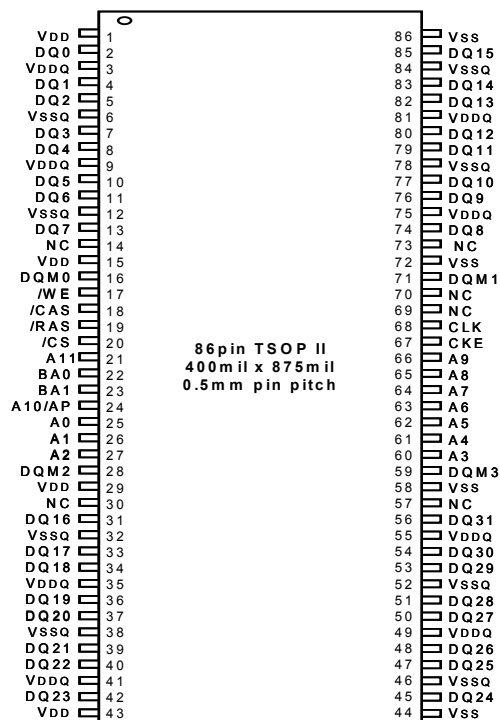
Part No.	Clock Frequency	Organization	Interface	Package
HY57V283220(L)T(P)-5 HY5V22(L)F(P)-5	200MHz	4Banks x 1Mbits x32	LVTTTL	86TSOP-II 90Ball FBGA
HY57V283220(L)T(P)-55 HY5V22(L)F(P)-55	183MHz			
HY57V283220(L)T(P)-6 HY5V22(L)F(P)-6	166MHz			
HY57V283220(L)T(P)-7 HY5V22(L)F(P)-7	143MHz			
HY57V283220(L)T(P)-H HY5V22(L)F(P)-H	133MHz			
HY57V283220(L)T(P)-8 HY5V22(L)F(P)-8	125MHz			
HY57V283220(L)T(P)-P HY5V22(L)F(P)-P	100MHz			
HY57V283220(L)T(P)-S HY5V22(L)F(P)-S	100MHz			

**Note)** Hynix supports lead free part for each speed grade with same specification.

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Rev. 0.9 / July 2004

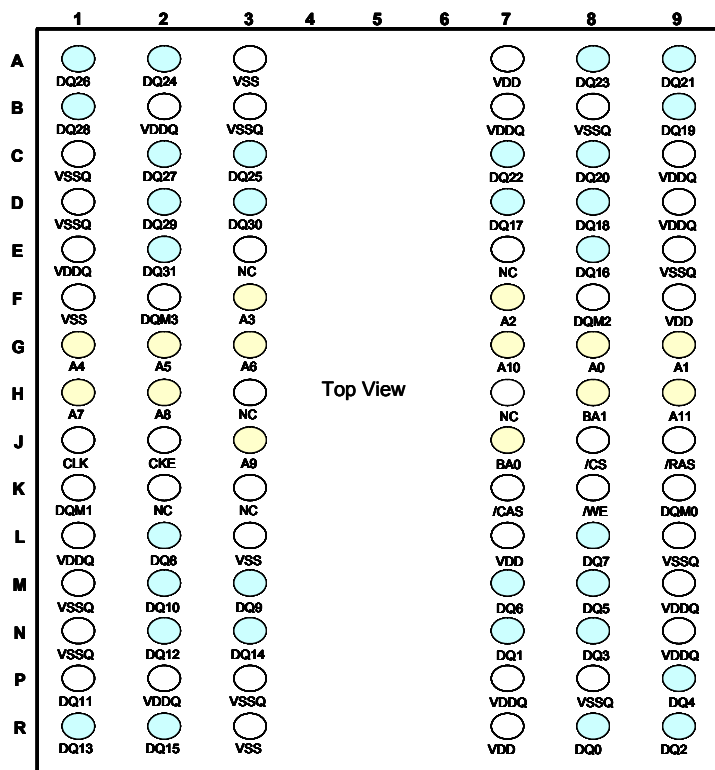
## PIN CONFIGURATION ( HY57V283220(L)T(P) Series)



## PIN DESCRIPTION

PIN	PIN NAME	DESCRIPTION
CLK	Clock	The system clock input. All other inputs are registered to the SDRAM on the rising edge of CLK.
CKE	Clock Enable	Controls internal clock signal and when deactivated, the SDRAM will be one of the states among power down, suspend or self refresh
$\overline{CS}$	Chip Select	Enables or disables all inputs except CLK, CKE and DQM
BA0, BA1	Bank Address	Selects bank to be activated during $\overline{RAS}$ activity Selects bank to be read/written during $\overline{CAS}$ activity
A0 ~ A11	Address	Row Address : RA0 ~ RA11, Column Address : CA0 ~ CA7 Auto-precharge flag : A10
$\overline{RAS}$ , $\overline{CAS}$ , $\overline{WE}$	Row Address Strobe, Column Address Strobe, Write Enable	$\overline{RAS}$ , $\overline{CAS}$ and $\overline{WE}$ define the operation Refer function truth table for details
DQM0~3	Data Input/Output Mask	Controls output buffers in read mode and masks input data in write mode
DQ0 ~ DQ31	Data Input/Output	Multiplexed data input / output pin
VDD/VSS	Power Supply/Ground	Power supply for internal circuits and input buffers
VDDQ/VSSQ	Data Output Power/Ground	Power supply for output buffers
NC	No Connection	No connection

## Ball CONFIGURATION ( HY5V22(L)F(P) Series)

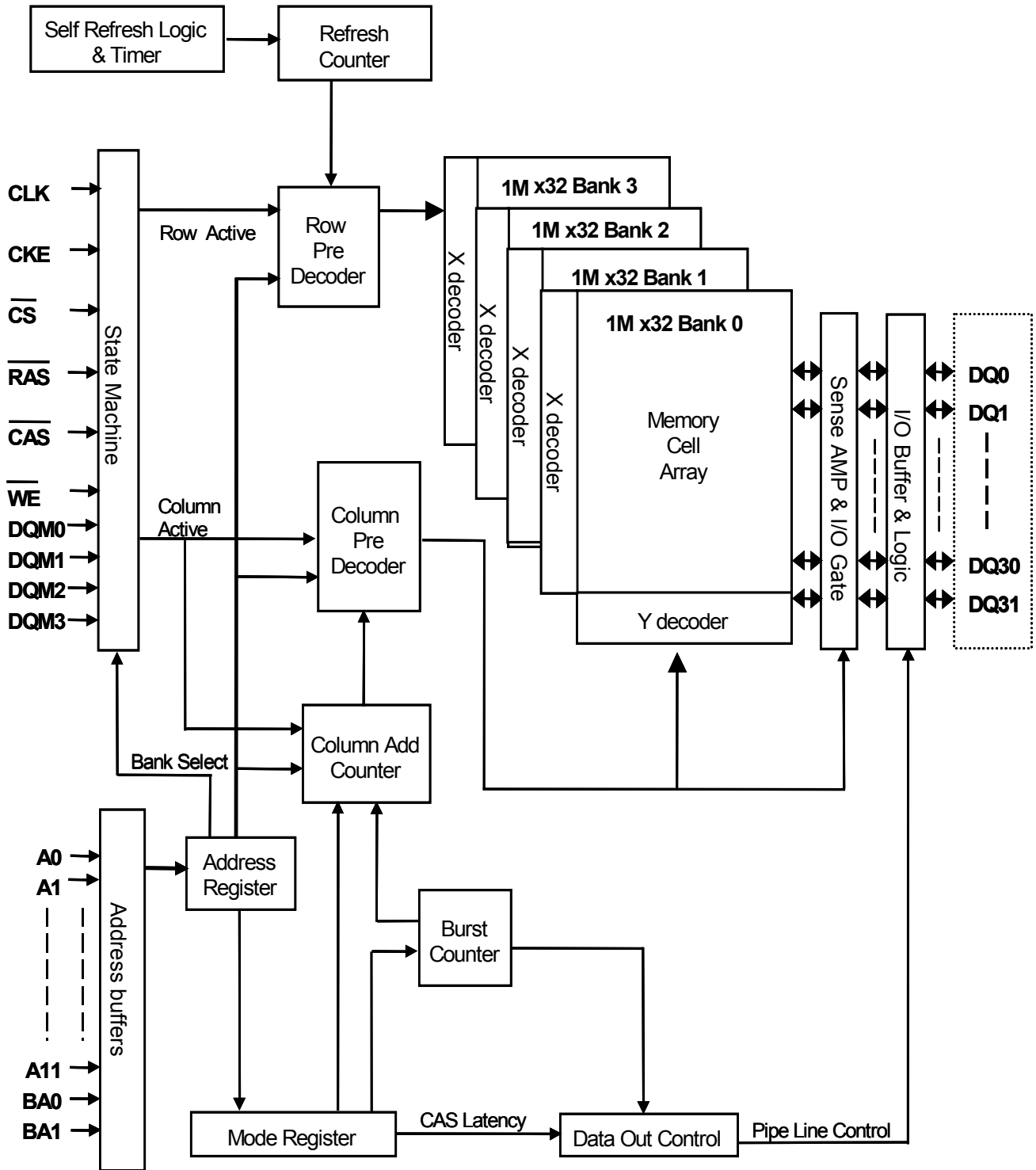


## Ball DESCRIPTION

PIN	PIN NAME	DESCRIPTION
CLK	Clock	The system clock input. All other inputs are registered to the SDRAM on the rising edge of CLK.
CKE	Clock Enable	Controls internal clock signal and when deactivated, the SDRAM will be one of the states among power down, suspend or self refresh
$\overline{CS}$	Chip Select	Enables or disables all inputs except CLK, CKE and DQM
BA0, BA1	Bank Address	Selects bank to be activated during $\overline{RAS}$ activity Selects bank to be read/written during $\overline{CAS}$ activity
A0 ~ A11	Address	Row Address : RA0 ~ RA11, Column Address : CA0 ~ CA7 Auto-precharge flag : A10
$\overline{RAS}$ , $\overline{CAS}$ , $\overline{WE}$	Row Address Strobe, Column Address Strobe, Write Enable	$\overline{RAS}$ , $\overline{CAS}$ and $\overline{WE}$ define the operation Refer function truth table for details
DQM0~3	Data Input/Output Mask	Controls output buffers in read mode and masks input data in write mode
DQ0 ~ DQ31	Data Input/Output	Multiplexed data input / output pin
VDD/VSS	Power Supply/Ground	Power supply for internal circuits and input buffers
VDDQ/VSSQ	Data Output Power/Ground	Power supply for output buffers
NC	No Connection	No connection

## FUNCTIONAL BLOCK DIAGRAM

### 1Mbit x 4banks x 32 I/O Synchronous DRAM



## ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Ambient Temperature	TA	0 ~ 70	°C
Storage Temperature	TSTG	-55 ~ 125	°C
Voltage on Any Pin relative to VSS	VIN, VOUT	-1.0 ~ 4.6	V
Voltage on VDD relative to VSS	VDD, VDDQ	-1.0 ~ 4.6	V
Short Circuit Output Current	IOS	50	mA
Power Dissipation	PD	1	W
Soldering Temperature & Time	TSOLDER	260 · 10	°C · Sec

**Note :** Operation at above absolute maximum rating can adversely affect device reliability

## DC OPERATING CONDITION (TA=0 to 70°C)

Parameter	Symbol	Min	Typ.	Max	Unit	Note
Power Supply Voltage	VDD, VDDQ	3.0	3.3	3.6	V	1
Input high voltage	VIH	2.0	3.0	VDDQ + 0.3	V	1,2
Input low voltage	VIL	- 0.3	0	0.8	V	1,3

**Note :**

1. All voltages are referenced to VSS = 0V
2. VIH (max) is acceptable 5.6V AC pulse width with ≤3ns of duration with no input clamp diodes
3. VIL (min) is acceptable -2.0V AC pulse width with ≤3ns of duration with no input clamp diodes

## AC OPERATING CONDITION (TA=0 to 70°C, 3.0V ≤VDD ≤3.6V, VSS=0V - Note1)

Parameter	Symbol	Value	Unit	Note
AC input high / low level voltage	VIH / VIL	2.4/0.4	V	
Input timing measurement reference level voltage	Vtrip	1.4	V	
Input rise / fall time	tR / tF	1	ns	
Output timing measurement reference level	Voutref	1.4	V	
Output load capacitance for access time measurement	CL	30	pF	1

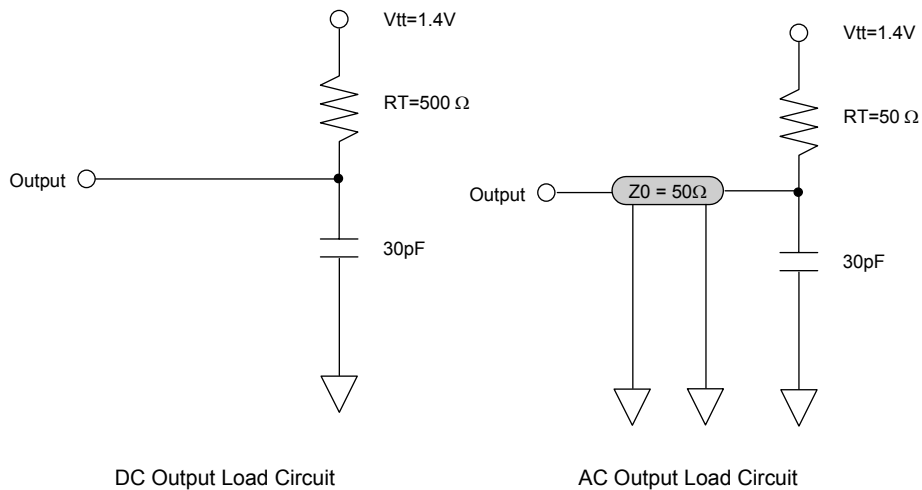
**Note :**

1. Output load to measure access times is equivalent to two TTL gates and one capacitor (30pF)  
For details, refer to AC/DC output load circuit

## CAPACITANCE ( HY57V283220T Series) (TA=25°C, f=1MHz, VDD=3.3V)

Parameter	Pin	Symbol	Min	Max	Unit
Input capacitance	CLK	CI1	2.5	4.0	pF
	A0 ~ A11, BA0, BA1, CKE, $\overline{CS}$ , $\overline{RAS}$ , $\overline{CAS}$ , $\overline{WE}$ , DQM0~3	CI2	2.5	4.0	pF
Data input / output capacitance	DQ0 ~ DQ31	CI/O	4.0	6.5	pF

## OUTPUT LOAD CIRCUIT



## DC CHARACTERISTICS I (DC operating conditions unless otherwise noted)

Parameter	Symbol	Min.	Max	Unit	Note
Input leakage current	ILI	-1	1	uA	1
Output leakage current	ILO	-1	1	uA	2
Output high voltage	VOH	2.4	-	V	IOH = -2mA
Output low voltage	VOL	-	0.4	V	IOL = +2mA

**Note :**

- 1.VIN = 0 to 3.6V, All other pins are not under test = 0V
- 2.DOUT is disabled, VOUT=0 to 3.6V

## DC CHARACTERISTICS II (DC operating conditions unless otherwise noted)

Parameter	Symbol	Test Condition	Speed								Unit	Note	
			-5	-55	-6	-7	-H	-8	-P	S			
Operating Current	IDD1	Burst length=1, One bank active $t_{RC} \geq t_{RC}(\min)$ , $I_{OL}=0\text{mA}$	120	120	110	100	100	100	90	90	mA	1	
Precharge Standby Current in power down mode	IDD2P	$CKE \leq V_{IL}(\max)$ , $t_{CK} = 10\text{ns}$	2								mA		
	IDD2PS	$CKE \leq V_{IL}(\max)$ , $t_{CK} = \infty$	1										
Precharge Standby Current in non power down mode	IDD2N	$CKE \geq V_{IH}(\min)$ , $\overline{CS} \geq V_{IH}(\min)$ , $t_{CK} = 10\text{ns}$ Input signals are changed one time during 2clks. All other pins $\geq V_{DD}-0.2\text{V}$ or $\leq 0.2\text{V}$	14								mA		
	IDD2NS	$CKE \geq V_{IH}(\min)$ , $t_{CK} = \infty$ Input signals are stable.	9										
Active Standby Current in power down mode	IDD3P	$CKE \leq V_{IL}(\max)$ , $t_{CK} = 10\text{ns}$	7								mA		
	IDD3PS	$CKE \leq V_{IL}(\max)$ , $t_{CK} = \infty$	6										
Active Standby Current in non power down mode	IDD3N	$CKE \geq V_{IH}(\min)$ , $\overline{CS} \geq V_{IH}(\min)$ , $t_{CK} = 10\text{ns}$ Input signals are changed one time during 2clks. All other pins $\geq V_{DD}-0.2\text{V}$ or $\leq 0.2\text{V}$	17								mA		
	IDD3NS	$CKE \geq V_{IH}(\min)$ , $t_{CK} = \infty$ Input signals are stable.	13										
Burst Mode Operating Current	IDD4	$t_{tCK} \geq t_{CK}(\min)$ , $I_{OL}=0\text{mA}$ All banks active	CL=3	230	220	200	180	180	150	130	130	mA	1
			CL=2	-	-	-	-	-	-	130	130		
Auto Refresh Current	IDD5	$t_{RC} \geq t_{RC}(\min)$ , All banks active	170	160	150	140	140	140	140	140	mA	2	
Self Refresh Current	IDD6	$CKE \leq 0.2\text{V}$	2								mA	3	
			0.8									4	

**Note :**

- 1.IDD1 and IDD4 depend on output loading and cycle rates. Specified values are measured with the output open
- 2.Min. of tRRC (Refresh RAS cycle time) is shown at AC CHARACTERISTICS II
- 3.HY57V283220T(P)(HY5V22F(P))-5/55/6/7/H/8/P/S
- 4.HY57V283220LT(P)(HY5V22LF(P))-5/55/6/7/H/8/P/S



## AC CHARACTERISTICS I (AC operating conditions unless otherwise noted)

Parameter		Symbol	-5		-55		-6		-7		-H		-8		-P		-S		Unit	Note
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
System clock cycle time	$\overline{\text{CAS}}$ Latency = 3	tCK3	5	1000	5.5	1000	6	1000	7	1000	7.5	1000	8	1000	10	1000	10	1000	ns	
	$\overline{\text{CAS}}$ Latency = 2	tCK2	10		10		10		10		10		-10		10		12		ns	
Clock high pulse width		tCHW	2	-	2.25	-	2.5	-	3	-	3	-	3	-	3	-	3	-	ns	1
Clock low pulse width		tCLW	2	-	2.25	-	2.5	-	3	-	3	-	3	-	3	-	3	-	ns	1
Access time from clock	$\overline{\text{CAS}}$ Latency = 3	tAC3	-	4.5	-	5	-	5.5	-	5.5	-	5.5	-	6	-	6	-	6	ns	2
	$\overline{\text{CAS}}$ Latency = 2	tAC2	-	6	-	6	-	6	-	6	-	6	-	6	-	6	-	6	ns	
Data-out hold time		tOH	1.5	-	2	-	2	-	2	-	2	-	2	-	2	-	2	-	ns	3
Data-Input setup time		tDS	1.5	-	1.5	-	1.5	-	1.75	-	1.75	-	2	-	2	-	2	-	ns	1
Data-Input hold time		tDH	1	-	1	-	1	-	1	-	1	-	1	-	1	-	1	-	ns	1
Address setup time		tAS	1.5	-	1.5	-	1.5	-	1.75	-	1.75	-	2	-	2	-	2	-	ns	1
Address hold time		tAH	1	-	1	-	1	-	1	-	1	-	1	-	1	-	1	-	ns	1
CKE setup time		tCKS	1.5	-	1.5	-	1.5	-	1.75	-	1.75	-	2	-	2	-	2	-	ns	1
CKE hold time		tCKH	1	-	1	-	1	-	1	-	1	-	1	-	1	-	1	-	ns	1
Command setup time		tCS	1.5	-	1.5	-	1.5	-	1.75	-	1.75	-	2	-	2	-	2	-	ns	1
Command hold time		tCH	1	-	1	-	1	-	1	-	1	-	1	-	1	-	1	-	ns	1
CLK to data output in low Z-time		tOLZ	1	-	1	-	1	-	1	-	1	-	1	-	1	-	1	-	ns	
CLK to data output in high Z-time	$\overline{\text{CAS}}$ Latency = 3	tOHZ3	-	4.5	-	5	-	5.5	-	5.5	-	5.5	-	6	-	6	-	6	ns	
	$\overline{\text{CAS}}$ Latency = 2	tOHZ2	-	6	-	6	-	6	-	6	-	6	-	6	-	6	-	6	ns	

**Note :**

1. Assume tR / tF (input rise and fall time ) is 1ns
2. Access times to be measured with input signals of 1v/ns edge rate, 0.8v to 2.0v
3. Data-out hold time to be measured under 30pF load condition, without Vt termination

## AC CHARACTERISTICS II (AC operating conditions unless otherwise noted)

Parameter		Symbol	-5		-55		-6		-7		-H		-8		-P		-S		Unit	Note
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
RAS cycle time	Operation	tRC	55	-	55	-	60	-	63	-	63	-	64	-	70	-	70	-	ns	
	Auto Refresh	tRRC	55	-	55	-	60	-	63	-	63	-	64	-	70	-	70	-	ns	
RAS to CAS delay		tRCD	15	-	16.5	-	18	-	20	-	20	-	20	-	20	-	20	-	ns	
RAS active time		tRAS	38.7	100 K	38.7	100 K	42	100 K	42	100 K	42	100 K	48	100 K	50	100 K	50	100 K	ns	
RAS precharge time		tRP	15	-	16.5	-	18	-	20	-	20	-	20	-	20	-	20	-	ns	
RAS to RAS bank active delay		tRRD	2	-	2	-	2	-	2	-	2	-	2	-	20	-	20	-	CLK	
CAS to CAS delay		tCCD	1	-	1	-	1	-	1	-	1	-	1	-	1	-	1	-	CLK	
Write command to data-in delay		tWTL	0	-	0	-	0	-	0	-	0	-	0	-	0	-	0	-	CLK	
Data-in to precharge command		tDPL	1	-	1	-	1	-	1	-	1	-	1	-	1	-	1	-	CLK	
Data-in to active command		tDAL	4	-	4	-	4	-	4	-	4	-	4	-	4	-	4	-	CLK	
DQM to data-out Hi-Z		tDQZ	2	-	2	-	2	-	2	-	2	-	2	-	2	-	2	-	CLK	
DQM to data-in mask		tDQM	0	-	0	-	0	-	0	-	0	-	0	-	0	-	0	-	CLK	
MRS to new command		tMRD	2	-	2	-	2	-	2	-	2	-	2	-	2	-	2	-	CLK	
Precharge to data output Hi-Z	CAS Latency = 3	tPROZ3	3	-	3	-	3	-	3	-	3	-	3	-	3	-	3	-	CLK	
	CAS Latency = 2	tPROZ2	2	-	2	-	2	-	2	-	2	-	2	-	2	-	2	-	CLK	
Power down exit time		tPDE	1	-	1	-	1	-	1	-	1	-	1	-	1	-	1	-	CLK	
Self refresh exit time		tSRE	1	-	1	-	1	-	1	-	1	-	1	-	1	-	1	-	CLK	1
Refresh Time		tREF	-	64	-	64	-	64	-	64	-	64	-	64	-	64	-	64	ms	

**Note :**

1. A new command can be given tRRC after self refresh exit

**DEVICE OPERATING OPTION TABLE**
**HY5xxxxxxxxxx(P)-5**

	<b>CAS Latency</b>	<b>tRCD</b>	<b>tRAS</b>	<b>tRC</b>	<b>tRP</b>	<b>tAC</b>	<b>tOH</b>
<b>200MHz(5ns)</b>	3CLKs	3CLKs	8CLKs	11CLKs	3CLKs	4.5ns	1.5ns
<b>183MHz(5.5ns)</b>	3CLKs	3CLKs	8CLKs	10CLKs	3CLKs	5ns	2ns
<b>166MHz(6ns)</b>	3CLKs	3CLKs	7CLKs	10CLKs	3CLKs	5.5ns	2ns

**HY5xxxxxxxxxx(P)-55**

	<b>CAS Latency</b>	<b>tRCD</b>	<b>tRAS</b>	<b>tRC</b>	<b>tRP</b>	<b>tAC</b>	<b>tOH</b>
<b>183MHz(5.5ns)</b>	3CLKs	3CLKs	7CLKs	10CLKs	3CLKs	5ns	2ns
<b>166MHz(6ns)</b>	3CLKs	3CLKs	7CLKs	10CLKs	3CLKs	5.5ns	2ns
<b>143MHz(7ns)</b>	3CLKs	3CLKs	6CLKs	9CLKs	3CLKs	5.5ns	2ns

**HY5xxxxxxxxxx(P)-6**

	<b>CAS Latency</b>	<b>tRCD</b>	<b>tRAS</b>	<b>tRC</b>	<b>tRP</b>	<b>tAC</b>	<b>tOH</b>
<b>166MHz(6ns)</b>	3CLKs	3CLKs	7CLKs	10CLKs	3CLKs	5.5ns	2ns
<b>143MHz(7ns)</b>	3CLKs	3CLKs	6CLKs	9CLKs	3CLKs	5.5ns	2ns
<b>125MHz(8ns)</b>	3CLKs	3CLKs	6CLKs	9CLKs	3CLKs	6ns	2.5ns

**HY5xxxxxxxxxx(P)-7**

	<b>CAS Latency</b>	<b>tRCD</b>	<b>tRAS</b>	<b>tRC</b>	<b>tRP</b>	<b>tAC</b>	<b>tOH</b>
<b>143MHz(7ns)</b>	3CLKs	3CLKs	6CLKs	9CLKs	3CLKs	5.5ns	2ns
<b>125MHz(8ns)</b>	3CLKs	3CLKs	6CLKs	9CLKs	3CLKs	6ns	2ns
<b>100MHz(10ns)</b>	2CLKs	2CLKs	5CLKs	7CLKs	2CLKs	6ns	2ns

**HY5xxxxxxxxxx(P)-H**

	<b>CAS Latency</b>	<b>tRCD</b>	<b>tRAS</b>	<b>tRC</b>	<b>tRP</b>	<b>tAC</b>	<b>tOH</b>
<b>133MHz(7.5ns)</b>	3CLKs	3CLKs	6CLKs	9CLKs	3CLKs	5.5ns	2ns
<b>125MHz(8ns)</b>	3CLKs	3CLKs	6CLKs	9CLKs	3CLKs	6ns	2ns
<b>100MHz(10ns)</b>	2CLKs	2CLKs	5CLKs	7CLKs	2CLKs	6ns	2ns

**HY5xxxxxxxxxx(P)-8**

	<b>CAS Latency</b>	<b>tRCD</b>	<b>tRAS</b>	<b>tRC</b>	<b>tRP</b>	<b>tAC</b>	<b>tOH</b>
<b>125MHz(8ns)</b>	3CLKs	3CLKs	6CLKs	9CLKs	3CLKs	6ns	2ns
<b>100MHz(10ns)</b>	2CLKs	2CLKs	5CLKs	7CLKs	2CLKs	6ns	2ns
<b>83MHz(12ns)</b>	2CLKs	2CLKs	4CLKs	6CLKs	2CLKs	6ns	2.5ns

## HY5xxxxxxxxxx(P)-P

	<b>CAS Latency</b>	<b>tRCD</b>	<b>tRAS</b>	<b>tRC</b>	<b>tRP</b>	<b>tAC</b>	<b>tOH</b>
<b>100MHz(10ns)</b>	2CLKs	2CLKs	5CLKs	7CLKs	2CLKs	6ns	2ns
<b>83MHz(12ns)</b>	2CLKs	2CLKs	5CLKs	7CLKs	2CLKs	6ns	2.5ns
<b>66MHz(15ns)</b>	2CLKs	2CLKs	4CLKs	6CLKs	2CLKs	6ns	2.5ns

## HY5xxxxxxxxxx(P)-S

	<b>CAS Latency</b>	<b>tRCD</b>	<b>tRAS</b>	<b>tRC</b>	<b>tRP</b>	<b>tAC</b>	<b>tOH</b>
<b>100MHz(10ns)</b>	3CLKs	2CLKs	5CLKs	7CLKs	2CLKs	6ns	2ns
<b>83MHz(12ns)</b>	2CLKs	2CLKs	5CLKs	7CLKs	2CLKs	6ns	2.5ns
<b>66MHz(15ns)</b>	2CLKs	2CLKs	4CLKs	6CLKs	2CLKs	6ns	2.5ns

**COMMAND TRUTH TABLE**

Command	CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	ADDR	A10/ AP	BA	Note	
Mode Register Set	H	X	L	L	L	L	X	OP code				
No Operation	H	X	H	X	X	X	X	X				
			L	H	H	H						
Bank Active	H	X	L	L	H	H	X	RA		V		
Read	H	X	L	H	L	H	X	CA	L	V		
Read with Autoprecharge									H			
Write	H	X	L	H	L	L	X	CA	L	V		
Write with Autoprecharge									H			
Precharge All Banks	H	X	L	L	H	L	X	X	H	X		
Precharge selected Bank									L	V		
Burst Stop	H	X	L	H	H	L	X	X				
DQM	H	X					V	X				
Auto Refresh	H	H	L	L	L	H	X	X				
Burst-Read-Single-WRITE	H	X	L	L	L	L	X	A9 Pin High (Other Pins OP code)			3	
Self Refresh <sup>1</sup>	Entry	H	L	L	L	L	H	X	X			
	Exit	L	H	H	X	X	X	X				
Precharge power down	Entry	H	L	H	X	X	X	X	X			
				L	H	H	H					
	Exit	L	H	H	X	X	X	X				
				L	H	H	H					
Clock Suspend	Entry	H	L	H	X	X	X	X	X			
				L	V	V	V					
	Exit	L	H	X				X				

**Note :**

1. Exiting Self Refresh occurs by asynchronously bringing CKE from low to high
2. X = Don't care, H = Logic High, L = Logic Low. BA = Bank Address, RA = Row Address, CA = Column Address, Opcode = Operand Code, NOP = No Operation
3. The burst read single write mode is entered by programming the write burst mode bit (A9) in the mode register to a logic 1.

## PACKAGE INFORMATION (HY57V283220T(P) Series)

400mil 86pin Thin Small Outline Package

