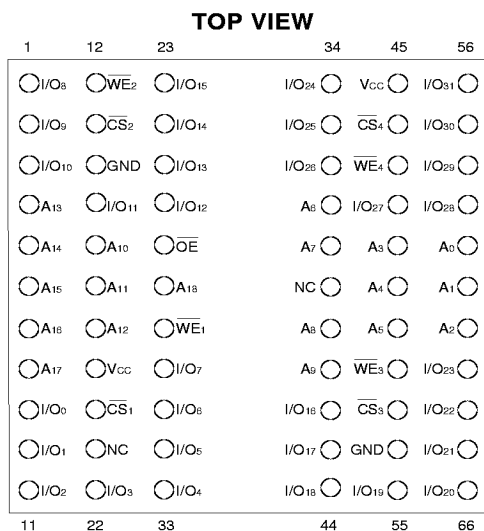


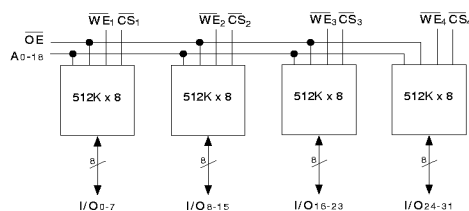
**512Kx32 SRAM MODULE** PRELIMINARY***FEATURES**

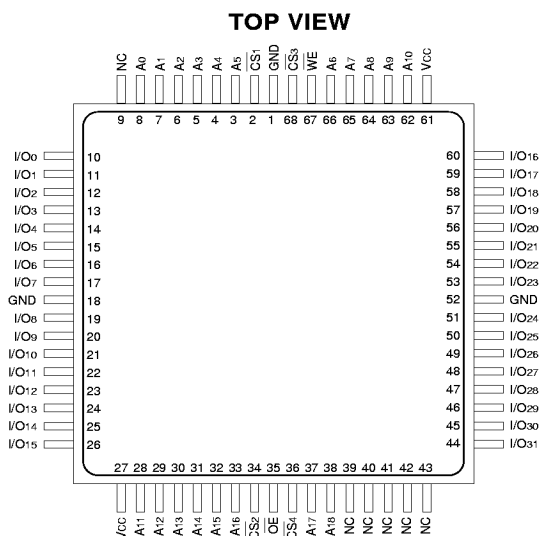
- Access Times of 17, 20, 25, 35, 45, 55nS
- Packaging
 - 66 pin, PGA Type, 1.385 inch square, Hermetic Ceramic HIP (Package 402), SMD Number 5962-94611
 - 68 lead, 40mm Hermetic Low Capacitance CQFP, 5.1mm (0.200") (Package 501) SMD Number 5962-95624
 - 68 lead, 40mm Hermetic Low Profile CQFP, 3.5mm (0.140") (Package 502), SMD Number 5962-94611, Package to be developed.
 - 68 lead, Hermetic CQFP (G2), 22mm (0.880 inch) square (Package 500). Designed to fit JEDEC 68 lead 0.990" CQFJ footprint (Fig. 3) SMD Number 5962-94611
- Organized as 512Kx32, User Configurable as 1Mx16 or 2Mx8
- Commercial, Industrial and Military Temperature Ranges
- TTL Compatible Inputs and Outputs
- 5 Volt Power Supply
- Low Power CMOS
- Built in Decoupling Caps and Multiple Ground Pins for Low Noise Operation
- Weight
 - WS512K32-XG2X- 8 grams typical
 - WS512K32-XH2X - 13 grams typical
 - WS512K32-XG4X - 20 grams typical

* This data sheet describes a product under development, not fully characterized, and is subject to change without notice.

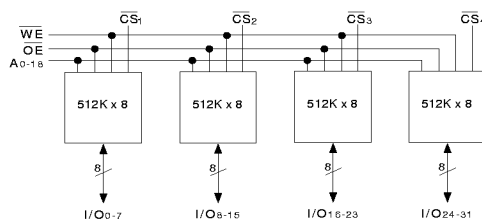
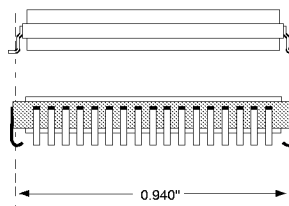
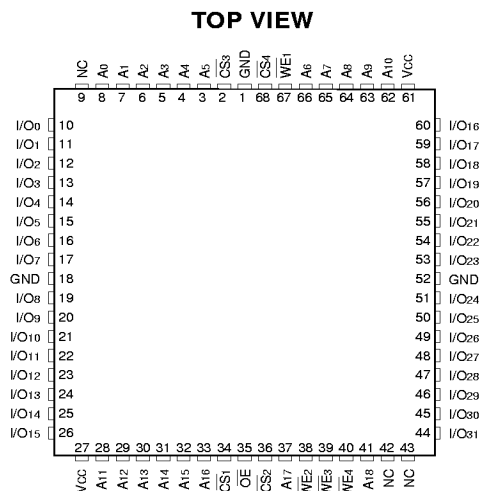
FIG. 1 PIN CONFIGURATION FOR WS512K32N-XH2X, SMD 5962-94611 (XXHXX)**PIN DESCRIPTION**

I/O ₀₋₃₁	Data Inputs/Outputs
A ₀₋₁₈	Address Inputs
$\overline{\text{WE}}_{1-4}$	Write Enables
$\overline{\text{CS}}_{1-4}$	Chip Selects
$\overline{\text{OE}}$	Output Enable
V _{CC}	Power Supply
GND	Ground
NC	Not Connected

BLOCK DIAGRAM

**FIG. 2 PIN CONFIGURATION FOR WS512K32F-XG4X, SMD 5962-95624 (XXHNX)
AND WS512K32-XG4TX, SMD 5962-94611 (XXHNX)****PIN DESCRIPTION**

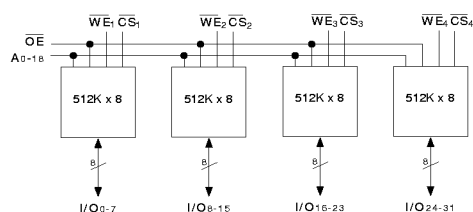
I/O0-31	Data Inputs/Outputs
A0-18	Address Inputs
WE	Write Enables
CS1-4	Chip Selects
OE	Output Enable
Vcc	Power Supply
GND	Ground
NC	Not Connected

BLOCK DIAGRAM**FIG. 3 PIN CONFIGURATION FOR WS512K32-XG2X, SMD 5962-94611 (XXHMX)**

The White 68 lead G2 CQFP fills the same fit and function as the JEDEC 68 lead CQFJ or 68 PLCC. But the G2 has the TCE and lead inspection advantage of the CQFP form.

PIN DESCRIPTION

I/O0-31	Data Inputs/Outputs
A0-18	Address Inputs
WE1-4	Write Enables
CS1-4	Chip Selects
OE	Output Enable
Vcc	Power Supply
GND	Ground
NC	Not Connected

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T _A	-55	+125	°C
Storage Temperature	T _{STG}	-65	+150	°C
Signal Voltage Relative to GND	V _G	-0.5	V _{CC} +0.5	V
Junction Temperature	T _J		150	°C
Supply Voltage	V _{CC}	-0.5	7.0	V

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V _{CC}	4.5	5.5	V
Input High Voltage	V _{IH}	2.2	V _{CC} + 0.3	V
Input Low Voltage	V _{IL}	-0.5	+0.8	V
Operating Temp (Mil)	T _A	-55	+125	°C

TRUTH TABLE

CS	OE	WE	Mode	Data I/O	Power
H	X	X	Standby	High Z	Standby
L	L	H	Read	Data Out	Active
L	H	H	Out Disable	High Z	Active
L	X	L	Write	Data In	Active

CAPACITANCE

(T_A = +25°C)

Parameter	Symbol	Conditions	Max	Unit
OE capacitance	C _{OE}	V _{IN} = 0 V, f = 1.0 MHz	50	pF
WE1-4 capacitance HIP (PGA)	C _{WE}	V _{IN} = 0 V, f = 1.0 MHz	20	pF
CQFP G4			50	
CQFP G2			20	
CS1-4 capacitance	C _{CS}	V _{IN} = 0 V, f = 1.0 MHz	20	pF
Data I/O capacitance	C _{I/O}	V _{I/O} = 0 V, f = 1.0 MHz	20	pF
Address input capacitance	C _{AD}	V _{IN} = 0 V, f = 1.0 MHz	50	pF

This parameter is guaranteed by design but not tested.

LOW CAPACITANCE CQFP

(T_A = +25°C)

Parameter	Symbol	Conditions	Max	Unit
OE capacitance	C _{OE}	V _{IN} = 0 V, f = 1.0 MHz	32	pF
CQFP G4 capacitance	C _{WE}	V _{IN} = 0 V, f = 1.0 MHz	32	pF
CS1-4 capacitance	C _{CS}	V _{IN} = 0 V, f = 1.0 MHz	15	pF
Data I/O capacitance	C _{I/O}	V _{I/O} = 0 V, f = 1.0 MHz	15	pF
Address input capacitance	C _{AD}	V _{IN} = 0 V, f = 1.0 MHz	32	pF

This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	Conditions	Units	
			Min	Max
Input Leakage Current	I _{LI}	V _{CC} = 5.5, V _{IN} = GND to V _{CC}		10
Output Leakage Current	I _{LO}	CS = V _{IH} , OE = V _{IH} , V _{OUT} = GND to V _{CC}		10
Operating Supply Current x 32 Mode	I _{CC} x 32	CS = V _{IL} , OE = V _{IH} , f = 5MHz, V _{CC} = 5.5		520
Standby Current	I _{SB}	CS = V _{IH} , OE = V _{IH} , f = 5MHz, V _{CC} = 5.5		60
Output Low Voltage	V _{OL}	I _{OL} = 8mA for 17 - 35nS, I _{OL} = 2.1mA for 45 - 55nS, V _{CC} = 4.5		0.4
Output High Voltage	V _{OH}	I _{OH} = -4.0mA for 17 - 35nS, I _{OH} = -1.0mA for 45 - 55nS, V _{CC} = 4.5	2.4	

NOTE: DC test conditions: V_{IH} = V_{CC} - 0.3V, V_{IL} = 0.3V

DATA RETENTION CHARACTERISTICS

(T_A = -55°C to +125°C)

Parameter	Symbol	Conditions	Units		
			Min	Typ	Max
Data Retention Supply Voltage	V _{DR}	CS ≥ V _{CC} - 0.2V	2.0		5.5
Data Retention Current	I _{CCDR1}	V _{CC} = 3V		3.2	12*

* Also available in Low Power version, please call factory for information.



AC CHARACTERISTICS

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	-17		-20		-25		-35		-45		-55		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t _{RC}	17		20		25		35		45		55		nS
Address Access Time	t _{AA}		17		20		25		35		45		55	nS
Output Hold from Address Change	t _{OH}	0		0		0		0		0		0		nS
Chip Select Access Time	t _{ACS}		17		20		25		35		45		55	nS
Output Enable to Output Valid	t _{OE}		9		10		12		25		25		25	nS
Chip Select to Output in Low Z	t _{CLZ}	2		2		2		4		4		4		nS
Output Enable to Output in Low Z	t _{OLZ}	0		0		0		0		0		0		nS
Chip Disable to Output in High Z	t _{CHZ}		12		12		12		15		20		20	nS
Output Disable to Output in High Z	t _{OHZ}		12		12		12		15		20		20	nS

1. This parameter is guaranteed by design but not tested.

AC CHARACTERISTICS

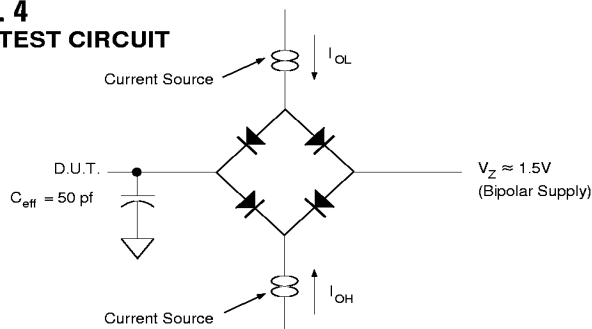
(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	-17		-20		-25		-35		-45		-55		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t _{WC}	17		20		25		35		45		55		nS
Chip Select to End of Write	t _{CW}	15		15		17		25		35		50		nS
Address Valid to End of Write	t _{AW}	15		15		17		25		35		50		nS
Data Valid to End of Write	t _{DW}	11		12		13		20		25		25		nS
Write Pulse Width	t _{WP}	15		15		17		25		35		40		nS
Address Setup Time	t _{AS}	2		2		2		2		2		2		nS
Address Hold Time	t _{AH}	0		0		0		0		5		5		nS
Output Active from End of Write	t _{OW}	2		3		4		4		5		5		nS
Write Enable to Output in High Z	t _{WHZ}		9		11		13		15		20		20	nS
Data Hold Time	t _{DH}	0		0		0		0		0		0		nS

1. This parameter is guaranteed by design but not tested.

2. The Address Setup Time of minimum 2nS is for the G2 and H2 packages. t_{AS} minimum for G4 and G4T packages is 0nS.

FIG. 4
AC TEST CIRCUIT



AC TEST CONDITIONS

Parameter	Typ	Unit
Input Pulse Levels	V _{IL} = 0, V _{IH} = 3.0	V
Input Rise and Fall	5	nS
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

NOTES:

V_Z is programmable from -2V to +7V.
I_{OL} & I_{OH} programmable from 0 to 16mA.
Tester Impedance Z₀ = 75 Ω.
V_Z is typically the midpoint of V_{OH} and V_{OL}.
I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.



FIG. 5
TIMING WAVEFORM - READ CYCLE

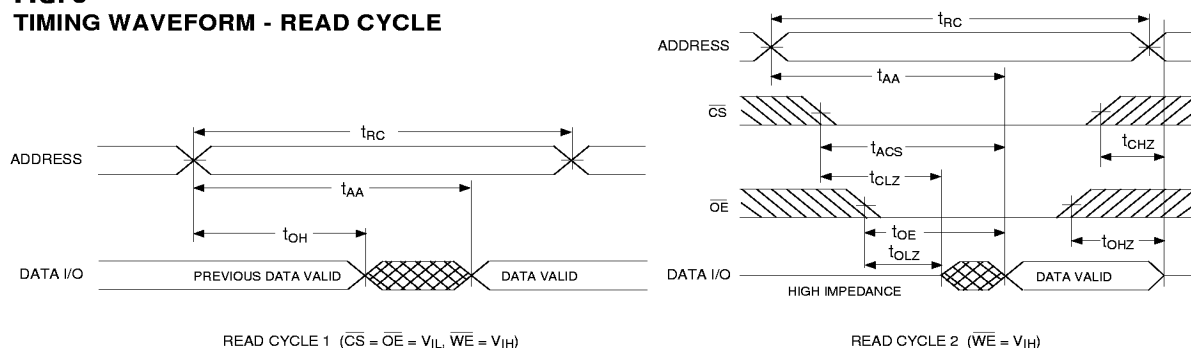


FIG. 6
WRITE CYCLE - $\overline{WE}$ CONTROLLED

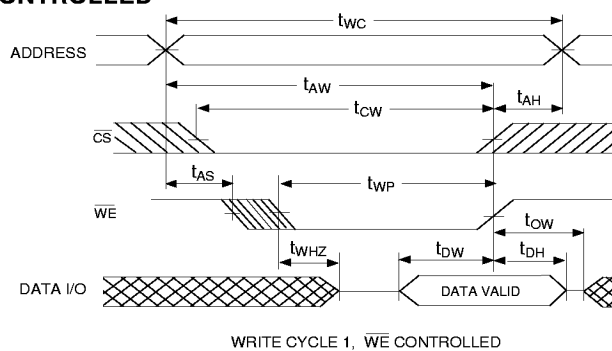
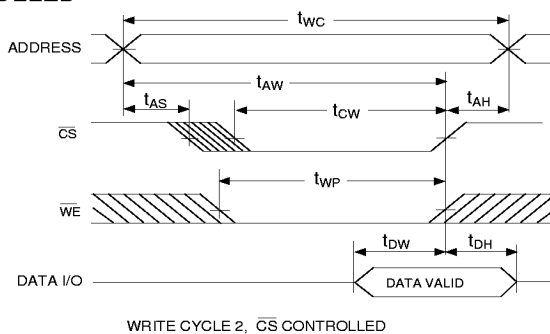
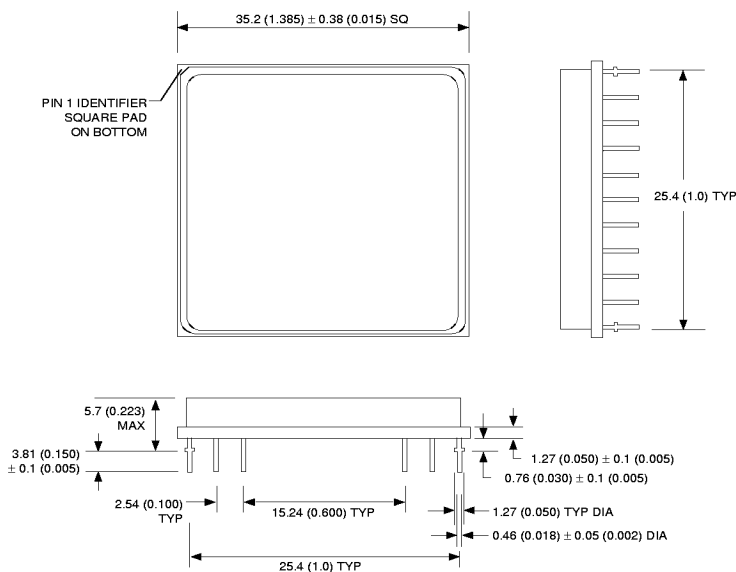
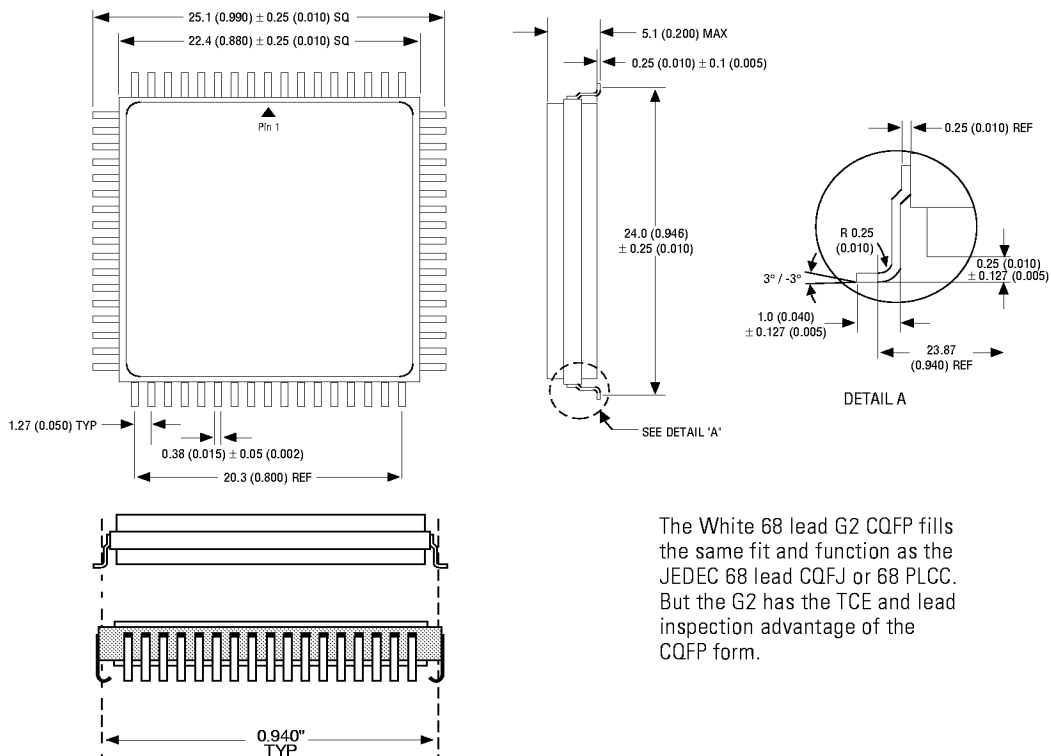


FIG. 7
WRITE CYCLE - $\overline{CS}$ CONTROLLED



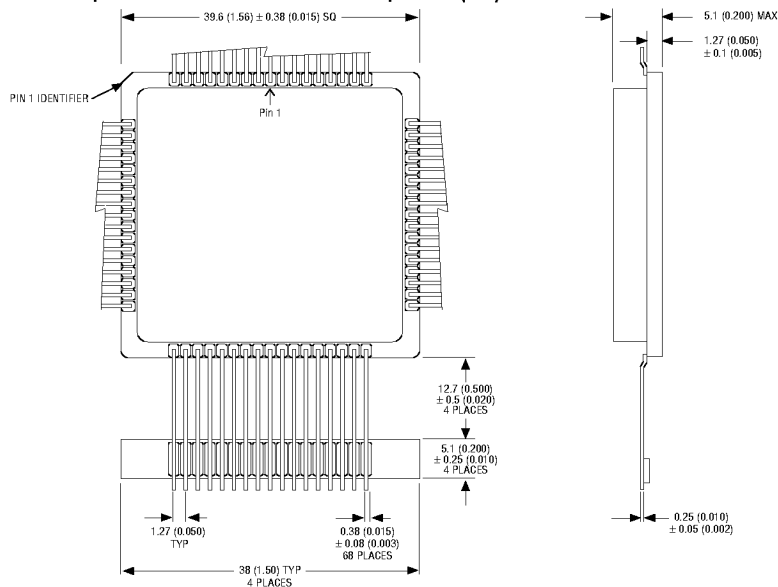
**PACKAGE 402: 66 PIN, PGA TYPE, CERAMIC HEX-IN-LINE PACKAGE, HIP (H2)**

ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

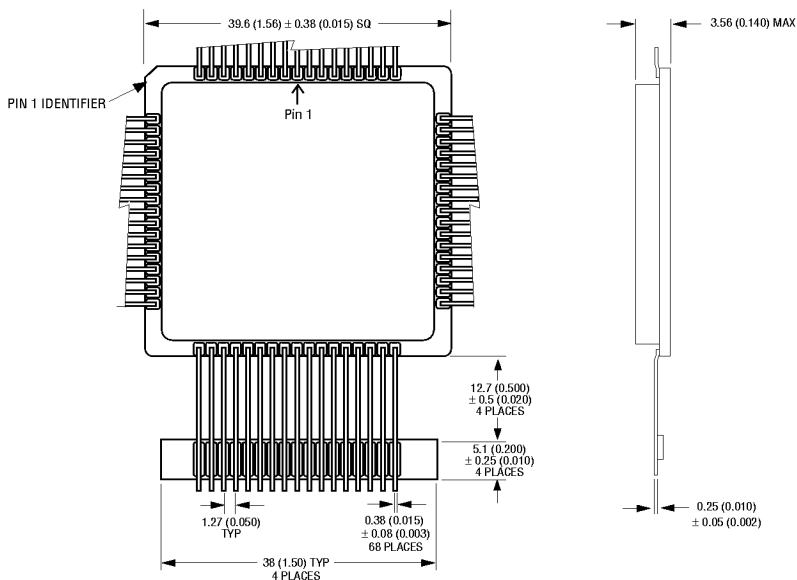
**PACKAGE 500: 68 LEAD, CERAMIC QUAD FLAT PACK, CQFP (G2)**

The White 68 lead G2 CQFP fills the same fit and function as the JEDEC 68 lead CQFJ or 68 PLCC. But the G2 has the TCE and lead inspection advantage of the CQFP form.

ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

**PACKAGE 501: 68 LEAD, CERAMIC QUAD FLAT PACK, CQFP (G4)**

ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

PACKAGE 502: 68 LEAD, CERAMIC QUAD FLAT PACK, LOW PROFILE CQFP (G4T)

ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

**ORDERING INFORMATION****W S 512K 32 X - XXX X X****DEVICE GRADE:**

Q = MIL-STD-883 Compliant
M = Military Screened -55°C to +125°C
I = Industrial -40°C to 85°C
C = Commercial 0°C to +70°C

PACKAGE TYPE:

H2 = Ceramic Hex-In-line Package, HIP (Package 402)
G2 = 22mm Ceramic Quad Flat Pack, CQFP (Package 500)
G4 = 40mm Ceramic Quad Flat Pack, CQFP (Package 501)
G4T = 40mm Low Profile CQFP (Package 502)

ACCESS TIME IN nS**IMPROVEMENT MARK:**

N = No Connect at pin 21 and 39 in HIP for Upgrades
F = Low Capacitance CQFP

ORGANIZATION, 512Kx32

User configurable as 1Mx16 or 2Mx8

SRAM**WHITE MICROELECTRONICS**



DEVICE TYPE	SPEED	PACKAGE	SMD NO.
128K x 32 SRAM Module	55nS	66 pin HIP (H1)	5962-94611 05HXX
128K x 32 SRAM Module	45nS	66 pin HIP (H1)	5962-94611 06HXX
128K x 32 SRAM Module	35nS	66 pin HIP (H1)	5962-94611 07HXX
128K x 32 SRAM Module	25nS	66 pin HIP (H1)	5962-94611 08HXX
128K x 32 SRAM Module	20nS	66 pin HIP (H1)	5962-94611 09HXX
128K x 32 SRAM Module	17nS	66 pin HIP (H1)	5962-94611 10HXX
512K x 32 SRAM Module	55nS	68 lead CQFP Low Profile (G4T)	5962-94611 05HYX
512K x 32 SRAM Module	45nS	68 lead CQFP Low Profile (G4T)	5962-94611 06HYX
512K x 32 SRAM Module	35nS	68 lead CQFP Low Profile (G4T)	5962-94611 07HYX
512K x 32 SRAM Module	25nS	68 lead CQFP Low Profile (G4T)	5962-94611 08HYX
512K x 32 SRAM Module	20nS	68 lead CQFP Low Profile (G4T)	5962-94611 09HYX
512K x 32 SRAM Module	17nS	68 lead CQFP Low Profile (G4T)	5962-94611 10HYX
512K x 32 SRAM Module	55nS	68 lead CQFP/J (G2)	5962-94611 05HMX
512K x 32 SRAM Module	45nS	68 lead CQFP/J (G2)	5962-94611 06HMX
512K x 32 SRAM Module	35nS	68 lead CQFP/J (G2)	5962-94611 07HMX
512K x 32 SRAM Module	25nS	68 lead CQFP/J (G2)	5962-94611 08HMX
512K x 32 SRAM Module	20nS	68 lead CQFP/J (G2)	5962-94611 09HMX
512K x 32 SRAM Module	17nS	68 lead CQFP/J (G2)	5962-94611 10HMX
512K x 32 SRAM Module	55nS	68 lead CQFP Low Capacitance (G4)	5962-95624 05HNX
512K x 32 SRAM Module	45nS	68 lead CQFP Low Capacitance (G4)	5962-95624 06HNX
512K x 32 SRAM Module	35nS	68 lead CQFP Low Capacitance (G4)	5962-95624 07HNX
512K x 32 SRAM Module	25nS	68 lead CQFP Low Capacitance (G4)	5962-95624 08HNX
512K x 32 SRAM Module	20nS	68 lead CQFP Low Capacitance (G4)	5962-95624 09HNX
512K x 32 SRAM Module	17nS	68 lead CQFP Low Capacitance (G4)	5962-95624 10HNX