

MOS INTEGRATED CIRCUIT

μ PD42S16190, 42S17190, 42S18190

16 M BIT DYNAMIC RAM
(FAST PAGE MODE & BYTE WRITE MODE)

PRELIMINARY

DESCRIPTION

The NEC μ PD42S16190, μ PD42S17190 and μ PD42S18190 are 1 048 576 words by 18 bits dynamic CMOS RAM with optional fast page mode. CMOS sense amplifier, peripheral circuits and 1 transistor memory cell technique realize high speed access, cycle time and low power dissipation.

Refresh is accomplished by performing $\overline{\text{RAS}}$ only refresh cycles, hidden refresh cycles, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycles, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh cycles or normal read or write cycles on the 4096 address combinations of A0 to A11 (for μ PD42S16190) or 2048 address combinations of A0 to A10 (for μ PD42S17190) or 1024 address combinations of A0 to A9 (for μ PD42S18190) during a 256 ms period.

The μ PD42S16190, μ PD42S17190 and μ PD42S18190 are packaged in 42-pin plastic SOJ and 50-pin plastic TSOP.

FEATURES

- 1 048 576 words by 18 bits organization
- Single +5V $\pm$ 10% power supply
- On-chip substrate bias generator
- Non latched I/O, TTL-compatible
- Multiplexed address inputs
- Read-modify-write, Fast Page Mode and Byte Write Mode capability
- $\overline{\text{RAS}}$ only refresh, hidden refresh and $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ internal address refresh
- $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh

DEVICE	Row Address	Column Address	Refresh cycle
μ PD42S16190	A0 to A11	A0 to A7	4096 cycles/256 ms
μ PD42S17190	A0 to A10	A0 to A8	2048 cycles/256 ms
μ PD42S18190	A0 to A9	A0 to A9	1024 cycles/256 ms

● 4 performance ranges

DEVICE	ACCESS TIME (MAX.)	R/W CYCLE (MIN.)	PAGE MODE CYCLE (MIN.)	Low power dissipation	
				Active(MAX.)	Standby
μ PD42S16190-50	50 ns	90 ns	35 ns	660 mW	2.2 mW (MAX.) (CMOS level)
μ PD42S17190-50				770 mW	
μ PD42S18190-50				1045 mW	
μ PD42S16190-60	60 ns	110 ns	40 ns	605 mW	
μ PD42S17190-60				715 mW	
μ PD42S18190-60				990 mW	
μ PD42S16190-70	70 ns	130 ns	45 ns	550 mW	
μ PD42S17190-70				660 mW	
μ PD42S18190-70				935 mW	
μ PD42S16190-80	80 ns	150 ns	50 ns	495 mW	
μ PD42S17190-80				605 mW	
μ PD42S18190-80				880 mW	

ORDERING INFORMATION

PART NUMBER	ACCESS TIME (MAX.)	PACKAGE	QUALITY GRADE
μ PD42S16190LE-50	50ns	42-pin Plastic SOJ	STANDARD
μ PD42S17190LE-50			
μ PD42S18190LE-50			
μ PD42S16190LE-60	60ns		
μ PD42S17190LE-60			
μ PD42S18190LE-60			
μ PD42S16190LE-70	70ns		
μ PD42S17190LE-70			
μ PD42S18190LE-70			
μ PD42S1610LE-80	80ns		
μ PD42S17190LE-80			
μ PD42S18190LE-80			
μ PD42S16190G5-50-7JF	50ns	50-pin Plastic TSOP	
μ PD42S17190G5-50-7JF			
μ PD42S18190G5-50-7JF			
μ PD42S16190G5-60-7JF	60ns		
μ PD42S17190G5-60-7JF			
μ PD42S18190G5-60-7JF			
μ PD42S16190G5-70-7JF	70ns		
μ PD42S17190G5-70-7JF			
μ PD42S18190G5-70-7JF			
μ PD42S16190G5-80-7JF	80ns		
μ PD42S17190G5-80-7JF			
μ PD42S18190G5-80-7JF			
μ PD42S16190G5-50-7KF	50ns	50-pin Plastic TSOP (Reverse bent)	
μ PD42S17190G5-50-7KF			
μ PD42S18190G5-50-7KF			
μ PD42S16190G5-60-7KF	60ns		
μ PD42S17190G5-60-7KF			
μ PD42S18190G5-60-7KF			
μ PD42S16190G5-70-7KF	70ns		
μ PD42S17190G5-70-7KF			
μ PD42S18190G5-70-7KF			
μ PD42S16190G5-80-7KF	80ns		
μ PD42S17190G5-80-7KF			
μ PD42S18190G5-80-7KF			

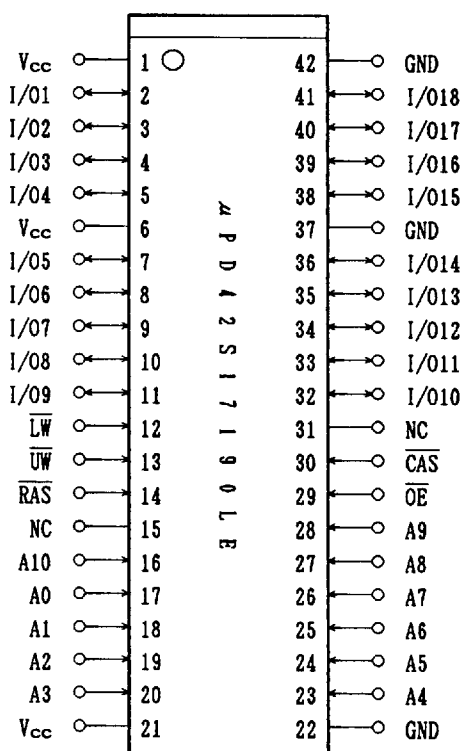
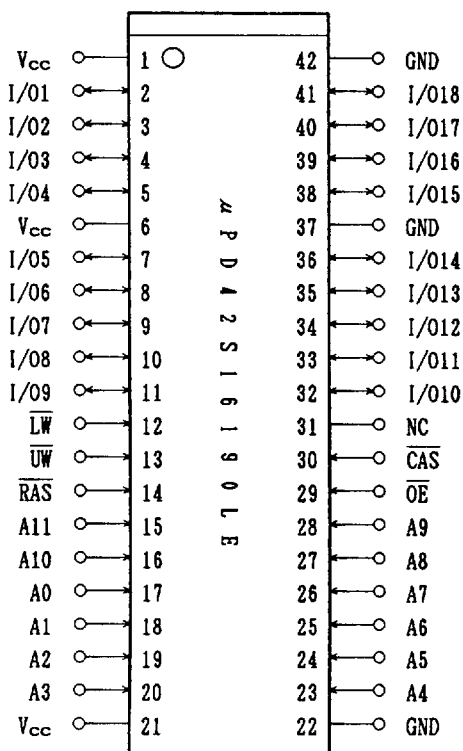
Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

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PIN CONFIGURATION (Marking Side)

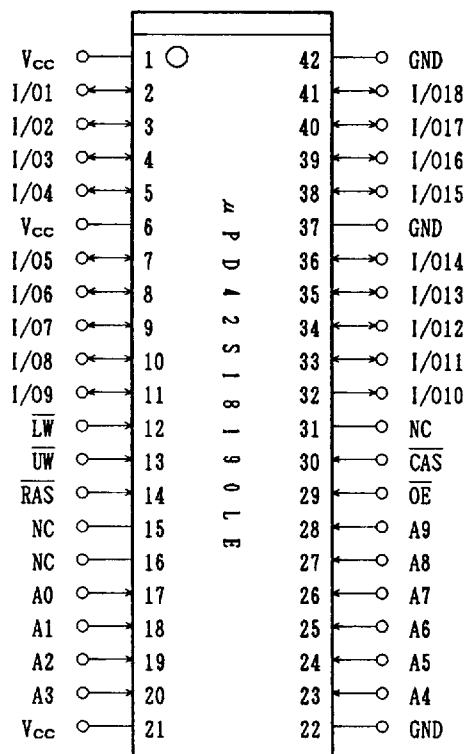
A0 to A9/A10/A11 : Address Inputs
 I/O1 to I/O18 : Data Inputs/Outputs
 $\overline{\text{RAS}}$: Row Address Strobe
 $\overline{\text{CAS}}$: Column Address Strobe
 $\overline{\text{UW}}$: Upper Byte Write Enable
 $\overline{\text{LW}}$: Lower Byte Write Enable
 OE : Output Enable
 V_{cc} : Supply Voltage
 GND : Ground
 NC : No Connection

42-pin Plastic SOJ (400 mil)



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42-pin Plastic SOJ (400 mil)

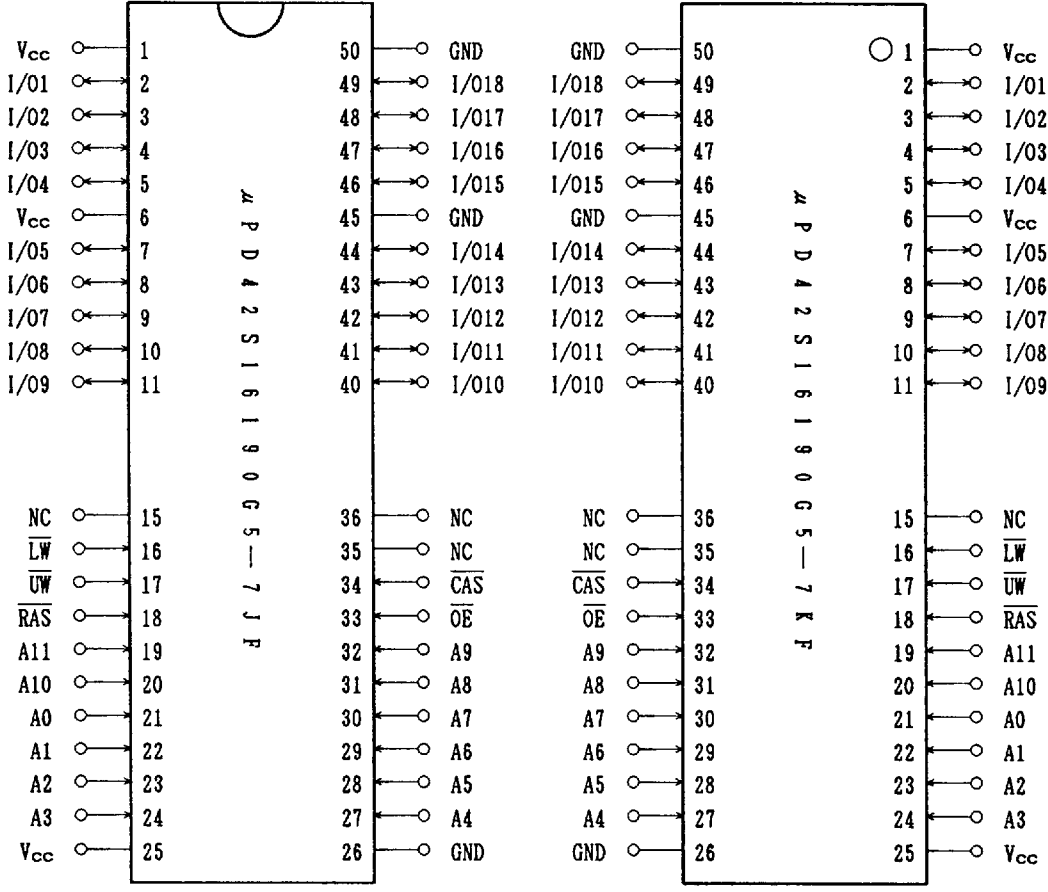


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50-pin Plastic TSOP (400 mil)

【μPD42S16190】

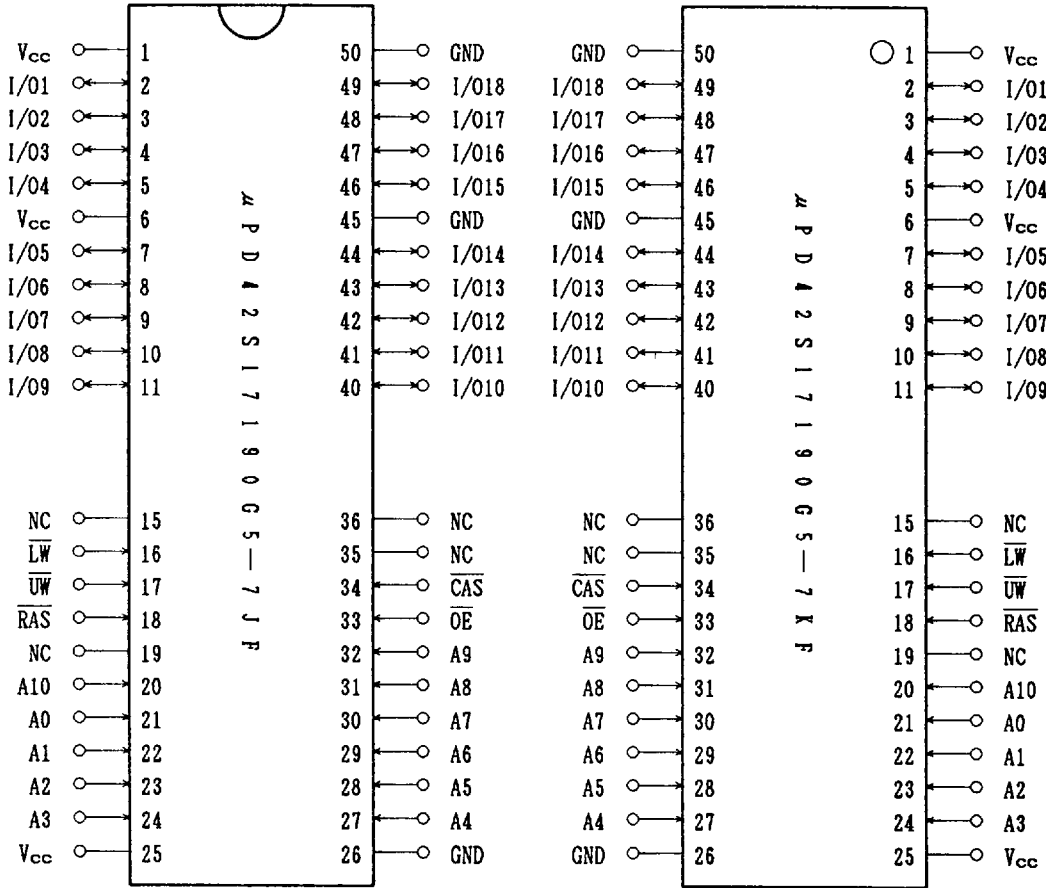
Reverse bent



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【 μ PD42S17190】

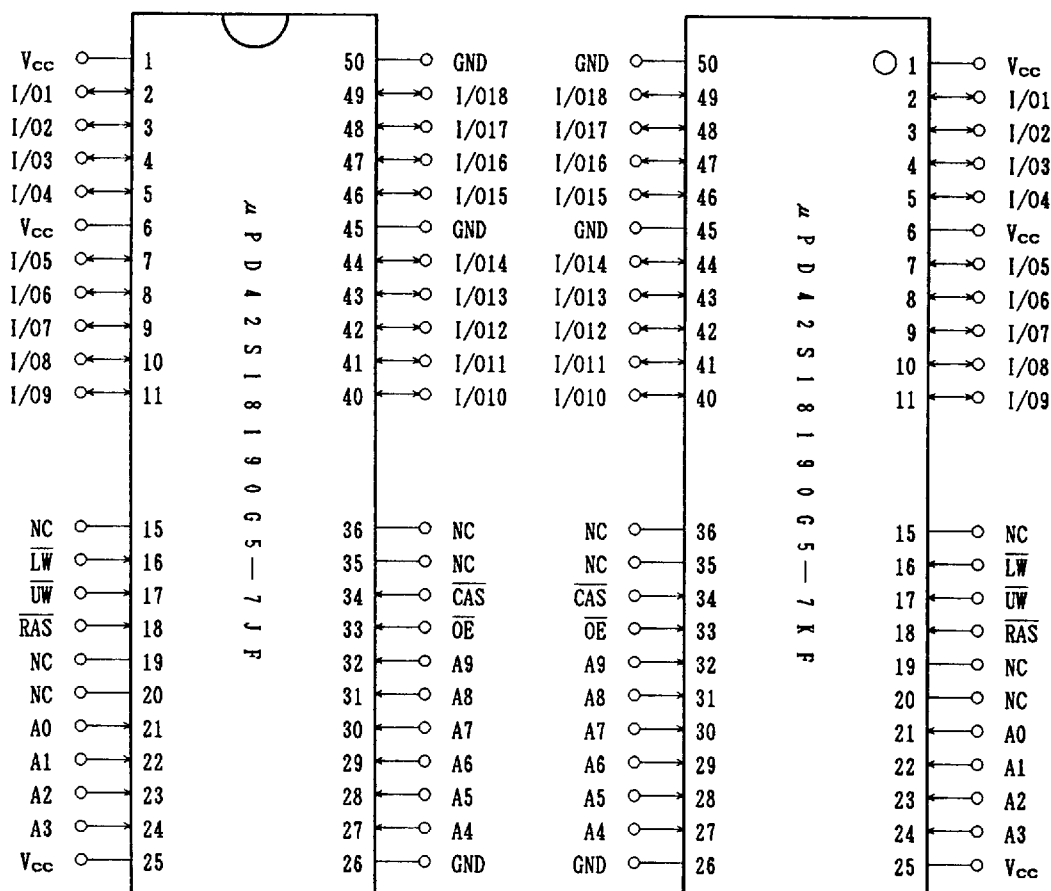
Reverse bent



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【μPD42S18190】

Reverse bent



μPD42S16190,42S17190,42S18190**ELECTRICAL SPECIFICATIONS****ABSOLUTE MAXIMUM RATINGS***

PARAMETER	SYMBOL	TEST CONDITION	RATING	UNIT
Voltage on Any Pin Relative to GND	V_T		-1.0 to +7.0	V
Short Circuit Output Current	I_O		50	mA
Power Dissipation	P_D		1	W
Operating Temperature	T_{opt}		0 to 70	°C
Storage Temperature	T_{stg}		-55 to +125	°C

*COMMENT : Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS NOTES:1,2

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{CC}		4.5	5.0	5.5	V
High Level Input Voltage	V_{IH}		2.4		$V_{CC}+1.0$	V
Low Level Input Voltage	V_{IL}		-1.0		0.8	V
Ambient Temperature	T_a		0		70	°C

CAPACITANCE ($T_a=25^\circ\text{C}$, $f=1\text{ MHz}$)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Input Capacitance	C_{I1}	A0 to A9/A10/A11			5	pF
	C_{I2}	$\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{UW}}$, $\overline{\text{LW}}$, $\overline{\text{OE}}$			7	pF
Data Input/Output Capacitance	C_D	I/O1 to I/O18			7	pF

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DC CHARACTERISTICS (Recommended Operating Conditions unless Otherwise noted)

【μPD42S16190】

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	NOTES
Operating Current	I _{CC1}	RAS, CAS Cycling			120	mA	3
		μPD42S16190-50			110		
		μPD42S16190-60			100		
		μPD42S16190-70			90		
Standby Current	I _{CC2}	RAS, CAS ≥ V _{IH(MIN.)} , I _O =0mA			2	mA	
		RAS, CAS ≥ V _{CC} -0.2V, I _O =0mA			0.4		
Refresh Current (RAS Only Refresh)	I _{CC3}	RAS Cycling,			120	mA	3
		CAS ≥ V _{IH(MIN.)}			110		
		t _{RC} = t _{RC(MIN.)} , I _O =0mA			100		
		μPD42S16190-80			90		
Operating Current (Fast Page Mode)	I _{CC4}	CAS Cycling,			100	mA	3
		RAS ≤ V _{IL(MAX.)}			90		
		t _{PC} = t _{PC(MIN.)} , I _O =0mA			80		
		μPD42S16190-80			70		
Refresh Current (CAS before RAS Refresh)	I _{CC5}	RAS Cycling,			120	mA	3
		t _{RC} = t _{RC(MIN.)} , I _O =0mA			110		
		μPD42S16190-70			100		
		μPD42S16190-80			90		
Battery back-up Current (Standby with CAS before RAS Refresh)	I _{CC6}	Standby: V _{CC} -0.2V ≤ RAS, CAS before RAS Refresh: 4096 Cycle/256 ms RAS, CAS: 0V ≤ V _{IL} ≤ 0.2V V _{CC} -0.2V ≤ V _{IH} ≤ V _{IH MAX.} WE, OE: V _{IH} Address: Don't care Output: OPEN	t _{RAS} ≤ 300ns		350	μA	
			t _{RAS} ≤ 1μs		500		
Self Refresh Current (CAS before RAS Self Refresh)	I _{CC7}	RAS, CAS: 0V ≤ V _{IL} ≤ 0.2V V _{CC} -0.2V ≤ V _{IH} ≤ V _{IH MAX.} , I _O =0mA			200	μA	
Input Leakage Current	I _{I(L)}	V _I =0 to 5.5V, all other pins= 0V	-10		10	μA	
Output Leakage Current	I _{O(L)}	D _{OUT} is disabled, V _O =0 to 5.5V	-10		10	μA	
Output High Voltage	V _{OH}	I _O =-2.5mA	2.4			V	
Output Low Voltage	V _{OL}	I _O =2.1mA			0.4	V	

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【μPD42S17190】

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	NOTES
Operating Current	I _{CC1}	$\overline{\text{RAS}}, \overline{\text{CAS}}$ Cycling $t_{\text{RC}}=t_{\text{RC(MIN.)}}, I_{\text{O}}=0\text{mA}$	μPD42S17190-50		140	mA	3
			μPD42S17190-60		130		
			μPD42S17190-70		120		
			μPD42S17190-80		110		
Standby Current	I _{CC2}	$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{IH(MIN.)}}, I_{\text{O}}=0\text{mA}$			2	mA	
		$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{CC}}-0.2\text{V}, I_{\text{O}}=0\text{mA}$			0.4		
Refresh Current ($\overline{\text{RAS}}$ Only Refresh)	I _{CC3}	$\overline{\text{RAS}}$ Cycling, $\overline{\text{CAS}} \geq V_{\text{IH(MIN.)}}$ $t_{\text{RC}}=t_{\text{RC(MIN.)}}, I_{\text{O}}=0\text{mA}$	μPD42S17190-50		140	mA	3
			μPD42S17190-60		130		
			μPD42S17190-70		120		
			μPD42S17190-80		110		
Operating Current (Fast Page Mode)	I _{CC4}	$\overline{\text{CAS}}$ Cycling, $\overline{\text{RAS}} \leq V_{\text{IL(MAX.)}}$ $t_{\text{PC}}=t_{\text{PC(MIN.)}}, I_{\text{O}}=0\text{mA}$	μPD42S17190-50		100	mA	3
			μPD42S17190-60		90		
			μPD42S17190-70		80		
			μPD42S17190-80		70		
Refresh Current ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh)	I _{CC5}	$\overline{\text{RAS}}$ Cycling, $t_{\text{RC}}=t_{\text{RC(MIN.)}}, I_{\text{O}}=0\text{mA}$	μPD42S17190-50		140	mA	3
			μPD42S17190-60		130		
			μPD42S17190-70		120		
			μPD42S17190-80		110		
Battery back-up Current (Standby with $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh)	I _{CC6}	Standby: $V_{\text{CC}}-0.2\text{V} \leq \overline{\text{RAS}}, \overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh: 2048 Cycle/256 ms $\overline{\text{RAS}}, \overline{\text{CAS}}: 0\text{V} \leq V_{\text{IL}} \leq 0.2\text{V}$ $V_{\text{CC}}-0.2\text{V} \leq V_{\text{IH}} \leq V_{\text{IH MAX.}}$ $\overline{\text{WE}}, \overline{\text{OE}}: V_{\text{IH}}$ Address: Don't care Output: OPEN	$t_{\text{RAS}} \leq 300\text{ns}$		300	μA	
			$t_{\text{RAS}} \leq 1\mu\text{s}$		400		
Self Refresh Current ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Self Refresh)	I _{CC7}	$\overline{\text{RAS}}, \overline{\text{CAS}}: 0\text{V} \leq V_{\text{IL}} \leq 0.2\text{V}$ $V_{\text{CC}}-0.2\text{V} \leq V_{\text{IH}} \leq V_{\text{IH MAX.}}, I_{\text{O}}=0\text{mA}$			200	μA	16
Input Leakage Current	I _{I(L)}	$V_{\text{I}}=0$ to 5.5V, all other pins= 0V	-10		10	μA	
Output Leakage Current	I _{O(L)}	D _{OUT} is disabled, $V_{\text{O}}=0$ to 5.5V	-10		10	μA	
Output High Voltage	V _{OH}	$I_{\text{O}}=-2.5\text{mA}$	2.4			V	
Output Low Voltage	V _{OL}	$I_{\text{O}}=2.1\text{mA}$			0.4	V	

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【μPD42S18190】

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	NOTES
Operating Current	I _{CC1}	$\overline{\text{RAS}}, \overline{\text{CAS}}$ Cycling $t_{\text{RC}}=t_{\text{RC(MIN.)}}, I_{\text{O}}=0\text{mA}$	μPD42S18190-50		190	mA	3
			μPD42S18190-60		180		
			μPD42S18190-70		170		
			μPD42S18190-80		160		
Standby Current	I _{CC2}	$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{IH(MIN.)}}, I_{\text{O}}=0\text{mA}$			2	mA	
		$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{CC}}-0.2\text{V}, I_{\text{O}}=0\text{mA}$			0.4		
Refresh Current ($\overline{\text{RAS}}$ Only Refresh)	I _{CC3}	$\overline{\text{RAS}}$ Cycling, $\overline{\text{CAS}} \geq V_{\text{IH(MIN.)}}$ $t_{\text{RC}}=t_{\text{RC(MIN.)}}, I_{\text{O}}=0\text{mA}$	μPD42S18190-50		190	mA	3
			μPD42S18190-60		180		
			μPD42S18190-70		170		
			μPD42S18190-80		160		
Operating Current (Fast Page Mode)	I _{CC4}	$\overline{\text{CAS}}$ Cycling, $\overline{\text{RAS}} \leq V_{\text{IL(MAX.)}}$ $t_{\text{PC}}=t_{\text{PC(MIN.)}}, I_{\text{O}}=0\text{mA}$	μPD42S18190-50		100	mA	3
			μPD42S18190-60		90		
			μPD42S18190-70		80		
			μPD42S18190-80		70		
Refresh Current ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh)	I _{CC5}	$\overline{\text{RAS}}$ Cycling, $t_{\text{RC}}=t_{\text{RC(MIN.)}}, I_{\text{O}}=0\text{mA}$	μPD42S18190-50		190	mA	3
			μPD42S18190-60		180		
			μPD42S18190-70		170		
			μPD42S18190-80		160		
Battery back-up Current (Standby with $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh)	I _{CC6}	Standby: $V_{\text{CC}}-0.2\text{V} \leq \overline{\text{RAS}}, \overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh: 1024 Cycle/256 ms $\overline{\text{RAS}}, \overline{\text{CAS}}: 0\text{V} \leq V_{\text{IL}} \leq 0.2\text{V}$ $V_{\text{CC}}-0.2\text{V} \leq V_{\text{IH}} \leq V_{\text{IH MAX.}}$ $\overline{\text{WE}}, \overline{\text{OE}}: V_{\text{IH}}$ Address: Don't care Output: OPEN	$t_{\text{RAS}} \leq 300\text{ns}$		250	μA	
			$t_{\text{RAS}} \leq 1\mu\text{s}$		300		
Self Refresh Current ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Self Refresh)	I _{CC7}	$\overline{\text{RAS}}, \overline{\text{CAS}}: 0\text{V} \leq V_{\text{IL}} \leq 0.2\text{V}$ $V_{\text{CC}}-0.2\text{V} \leq V_{\text{IH}} \leq V_{\text{IH MAX.}}, I_{\text{O}}=0\text{mA}$			200	μA	16
Input Leakage Current	I _{I(L)}	$V_{\text{I}}=0$ to 5.5V, all other pins= 0V	-10		10	μA	
Output Leakage Current	I _{O(L)}	D _{OUT} is disabled, $V_{\text{O}}=0$ to 5.5V	-10		10	μA	
Output High Voltage	V _{OH}	$I_{\text{O}}=-2.5\text{mA}$	2.4			V	
Output Low Voltage	V _{OL}	$I_{\text{O}}=2.1\text{mA}$			0.4	V	

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AC CHARACTERISTICS

(Recommended Operating Conditions unless Otherwise noted) NOTES:2,4,5

(1/2)

PARAMETER	SYMBOL	μPD42S16190-50		μPD42S16190-60		μPD42S16190-70		μPD42S16190-80		UNIT	NOTES
		μPD42S17190-50		μPD42S17190-60		μPD42S17190-70		μPD42S17190-80			
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Random Read or Write Cycle Time	t _{RC}	90		110		130		150		ns	6
Read Write Cycle Time	t _{RWC}	140		160		180		200		ns	6
Fast Page Mode Cycle Time(Read or Write)	t _{PC}	35		40		45		50		ns	6
Read Modify Write Cycle Time(Fast Page Mode)	t _{PRWC}	80		85		90		105		ns	6
Access Time from $\overline{\text{RAS}}$	t _{RAC}		50		60		70		80	ns	7, 8
Access Time from $\overline{\text{CAS}}$ (Falling Edge)	t _{CAC}		15		15		20		20	ns	7, 8
Access Time from Column Address	t _{AA}		25		30		35		40	ns	7, 8
Access Time from $\overline{\text{CAS}}$ Precharge	t _{ACP}		30		35		40		45	ns	7
Access Time from $\overline{\text{OE}}$	t _{OEA}		15		15		20		20	ns	
$\overline{\text{RAS}}$ to Column Address Delay Time	t _{RAD}	13	25	15	30	15	35	17	40	ns	8
$\overline{\text{CAS}}$ -Data Set-up Time	t _{CLZ}	0		0		0		0		ns	7
$\overline{\text{OE}}$ -Data Set-up Time	t _{OLZ}	0		0		0		0		ns	7
Output Buffer Turn-off Delay ($\overline{\text{CAS}}$)	t _{OFF}	0	10	0	13	0	15	0	15	ns	9
$\overline{\text{OE}}$ Data Delay Time	t _{OED}	10		13		15		15		ns	
Output Buffer Turn-off Delay ($\overline{\text{OE}}$)	t _{OEZ}	0	10	0	13	0	15	0	15	ns	9
$\overline{\text{OE}}$ Command Hold Time	t _{OBH}	0		0		0		0		ns	
$\overline{\text{OE}}$ to $\overline{\text{RAS}}$ inactive Set-up Time	t _{OES}	0		0		0		0		ns	
Transition Time (Rise and Fall)	t _T	3	50	3	50	3	50	3	50	ns	
$\overline{\text{RAS}}$ Precharge Time	t _{RP}	30		40		50		60		ns	
$\overline{\text{RAS}}$ Pulse Width (Random Read,Write Cycle)	t _{RAS}	50	10000	60	10000	70	10000	80	10000	ns	
$\overline{\text{RAS}}$ Pulse Width (Fast Page Mode)	t _{RASP}	50	125000	60	125000	70	125000	80	125000	ns	
$\overline{\text{RAS}}$ Hold Time	t _{RSH}	13		15		18		20		ns	
$\overline{\text{CAS}}$ Pulse Width	t _{CAS}	13	10000	15	10000	20	10000	20	10000	ns	
$\overline{\text{CAS}}$ Hold Time	t _{CSH}	50		60		70		80		ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	t _{RCD}	18	32	20	45	20	50	25	60	ns	8
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	t _{CRP}	5		5		5		5		ns	10
$\overline{\text{CAS}}$ Precharge Time	t _{CPN}	8		10		10		10		ns	
$\overline{\text{CAS}}$ Precharge Time (Fast Page Mode)	t _{CP}	8		10		10		10		ns	
$\overline{\text{RAS}}$ Precharge $\overline{\text{CAS}}$ Hold Time	t _{RPC}	5		5		5		5		ns	
$\overline{\text{RAS}}$ Hold Time from $\overline{\text{CAS}}$ Precharge	t _{RHCP}	30		35		40		45		ns	
Row Address Set-up Time	t _{ASR}	0		0		0		0		ns	
Row Address Hold Time	t _{RAH}	8		10		10		12		ns	

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PARAMETER	SYMBOL	μPD42S16190-50		μPD42S16190-60		μPD42S16190-70		μPD42S16190-80		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Column Address Set-up Time	t _{ASC}	0		0		0		0		ns	
Column Address Hold Time	t _{CAH}	13		15		15		15		ns	
Column Address Lead Time Referenced to $\overline{\text{RAS}}$	t _{RAL}	25		30		35		40		ns	
Read Command Set-up Time	t _{RCS}	0		0		0		0		ns	
Read Command Hold Time Referenced to $\overline{\text{RAS}}$	t _{RRH}	0		0		0		0		ns	11
Read Command Hold Time Referenced to $\overline{\text{CAS}}$	t _{RCH}	0		0		0		0		ns	11
Write Command Hold Time Referenced to $\overline{\text{CAS}}$	t _{WCH}	8		10		10		15		ns	12
Write Command Pulse Width	t _{WP}	8		10		10		15		ns	12
Data-in Set-up Time	t _{DS}	0		0		0		0		ns	13
Data-in Hold Time	t _{DH}	10		10		15		15		ns	13
$\overline{\text{WE}}$ Command Set-up Time	t _{WCS}	0		0		0		0		ns	14
$\overline{\text{CAS}}$ Precharge to $\overline{\text{WE}}$ Delay Time(Fast Page)	t _{CPWD}	55		60		65		70		ns	15
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay	t _{CWD}	33		38		40		45		ns	15
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay	t _{RWD}	70		83		95		105		ns	15
Column Address to $\overline{\text{WE}}$ Delay Time	t _{AWD}	45		53		60		65		ns	15
Write Command to $\overline{\text{RAS}}$ Lead Time	t _{RWL}	18		20		20		20		ns	
Write Command to $\overline{\text{CAS}}$ Lead Time	t _{CWL}	13		15		15		15		ns	
$\overline{\text{CAS}}$ Set-up Time for CBR Refresh	t _{CSR}	5		5		5		5		ns	
$\overline{\text{CAS}}$ Hold Time for CBR Refresh	t _{CHR}	10		10		10		10		ns	
Masked Write Set-up Time	t _{MCS}	0		0		0		0		ns	
Masked Write Hold Time Referenced to $\overline{\text{RAS}}$	t _{MRH}	0		0		0		0		ns	
Masked Write Hold Time Referenced to $\overline{\text{CAS}}$	t _{MCH}	0		0		0		0		ns	
$\overline{\text{RAS}}$ Pulse Width (Self Refresh Cycle)	t _{RASS}	100		100		100		100		μs	
$\overline{\text{RAS}}$ Precharge Time (Self Refresh Cycle)	t _{RPS}	90		110		130		150		ns	
$\overline{\text{CAS}}$ Hold Time (Self Refresh Cycle)	t _{CHS}	-50		-50		-50		-50		ns	
Refresh Period	t _{REF}		256		256		256		256	ms	16

NOTES:

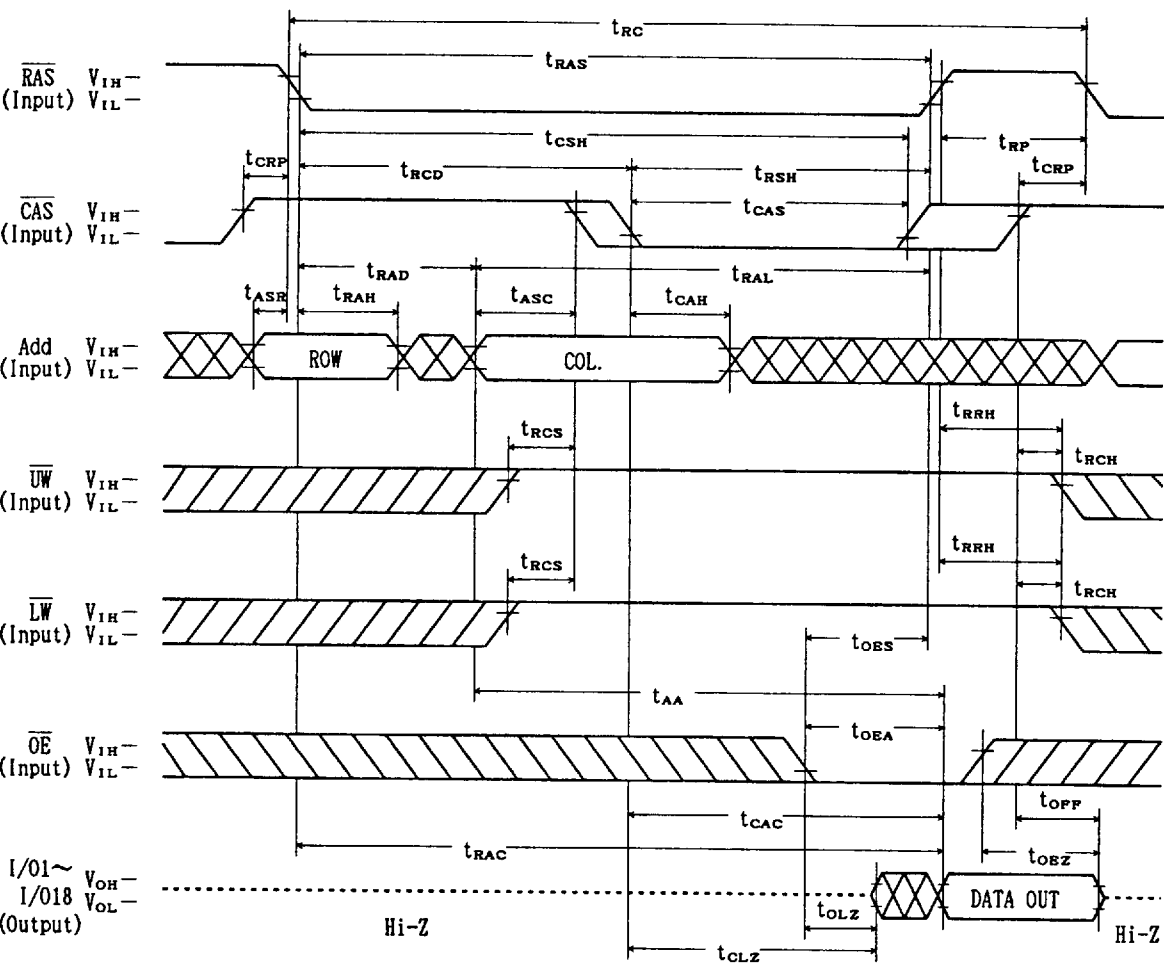
1. All voltages referenced to GND.
2. An initial pause of 100 μ s required after power-on followed by 8 refresh ($\overline{\text{RAS}}$ only refresh or $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh) cycles before proper device operation is achieved.
3. I_{CC1} , I_{CC3} , I_{CC4} and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. In addition to this, I_{CC3} is measured on condition that column addresses in $\overline{\text{RAS}}$ only cycle are held high or low level and I_{CC4} is measured on condition that column addresses in fast page mode are changed only one time during $t_{PC(MIN.)}$.
4. AC measurements assume $t_T=5\text{ns}$
5. $V_{IH(MIN.)}$ and $V_{IL(MAX.)}$ are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} .
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($T_a=0$ to 70°C) is assured.
7. Load = 1 TTL loads and 100pF
8. The access time is determined by $\overline{\text{RAS}}$ access time t_{RAC} , address access time t_{AA} , and $\overline{\text{CAS}}$ address time t_{CAC} . The relationship between these access time and t_{RCD} , t_{RAD} is as follows.

CONDITION	ACCESS TIME
$t_{RAD} \leq t_{RAD(MAX.)}$ and $t_{RCD} \leq t_{RCD(MAX.)}$	$t_{RAC(MAX.)}$
$t_{RAD} \geq t_{RAD(MAX.)}$	$t_{AA(MAX.)}$
$t_{RCD} \geq t_{RCD(MAX.)}$	$t_{CAC(MAX.)}$

9. $t_{OFF(MAX.)}$ and $t_{OEZ(MAX.)}$ defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL} .
10. t_{CRP} requirement should be applicable for $\overline{\text{RAS}}$ / $\overline{\text{CAS}}$ cycles preceded by any cycles.
11. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
12. t_{WP} is applicable for late write cycle. If the cycle is early write, it should be satisfied value of t_{WCH} .
13. These parameters are referenced to $\overline{\text{CAS}}$ leading edge in early write cycles and to $\overline{\text{UW/LW}}$ leading edge in late write or read-modify-write cycles.
14. If $t_{WCS} \geq t_{WCS(MIN.)}$ the cycle is an early write cycle and the data output will remain open circuit throughout the entire cycle.
15. If $t_{CPWD} \geq t_{CPWD(MIN.)}$, $t_{CWD} \geq t_{CWD(MIN.)}$, $t_{RWD} \geq t_{RWD(MIN.)}$, $t_{AWD} \geq t_{AWD(MIN.)}$ the cycle is a read-write and the data output will contain data read from the selected cell. If neither of the above conditions are met, the condition of the data out (at access time and until $\overline{\text{CAS}}$ goes back to V_{IH}) is indeterminate.
16. How to enter into $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh mode.
 - In case of using distributed $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh
Refresh 4096 or 2048 or 1024 times during a 256ms (Before set into the $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh mode, and after reset).
 - In case of using burst $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh
Refresh 4096 times during a 64ms (μ PD42S16190) or 2048 times during a 32ms (μ PD42S17190) or 1024 times during a 16ms (μ PD42S18190) (Before set into the $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh mode, and after reset).
 - In case of use $\overline{\text{RAS}}$ only refresh
Refresh against all refresh address during 64ms (μ PD42S16190) or 32ms (μ PD42S17190) or 16ms (μ PD42S18190) (Before set into the $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh mode, and after reset).

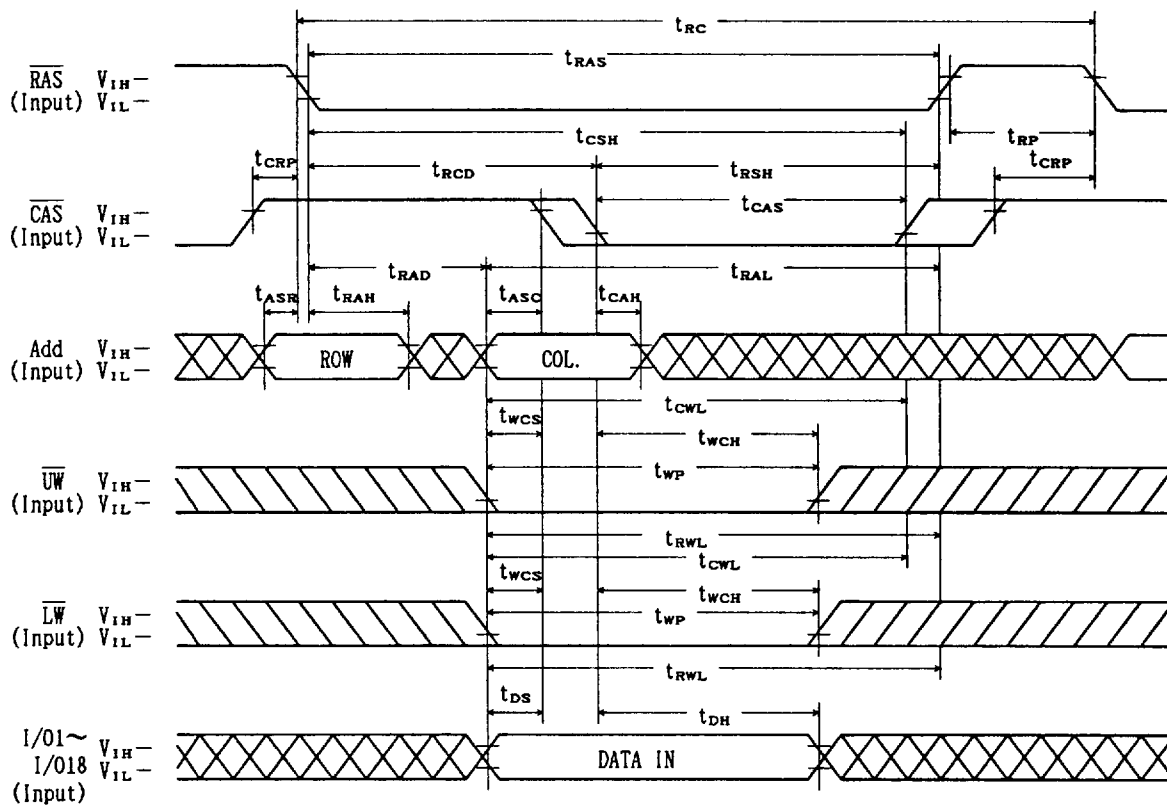
μPD42S16190,42S17190,42S18190

TIMING DIAGRAMS
READ CYCLE



μ PD42S16190,42S17190,42S18190

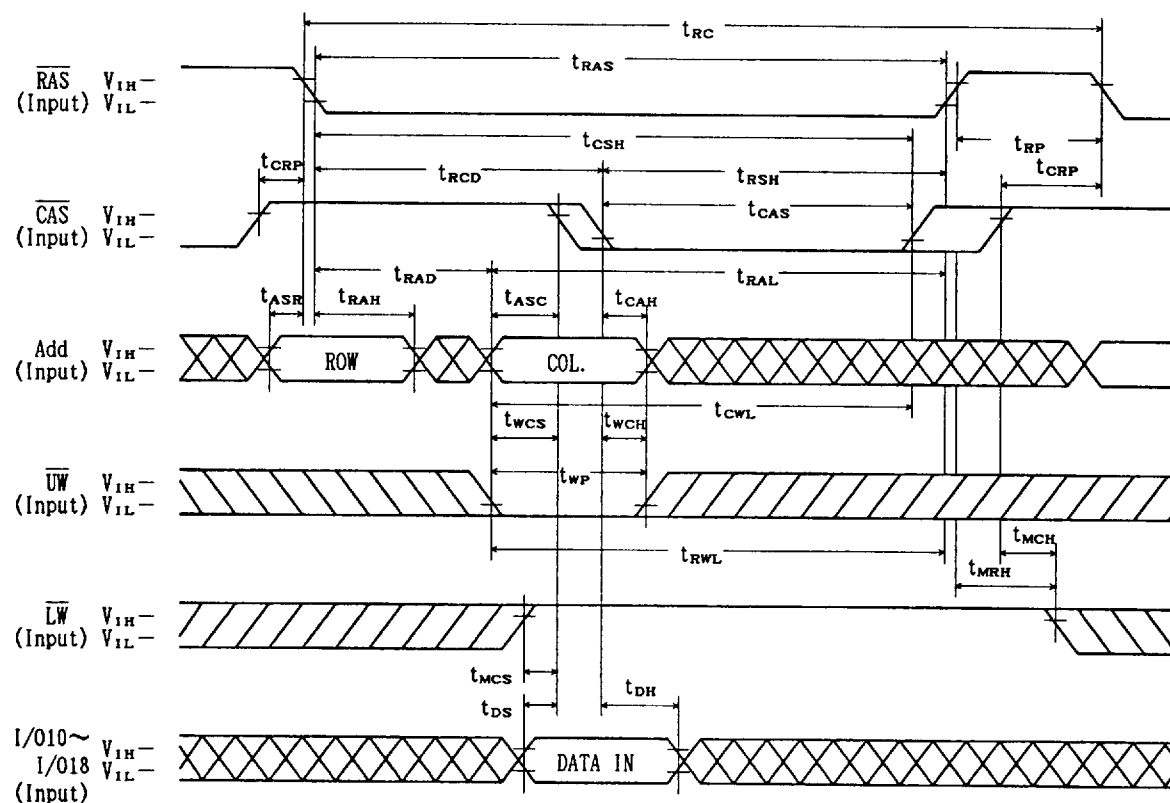
EARLY WRITE CYCLE



Note: $\overline{\text{OE}}$ = Don't care

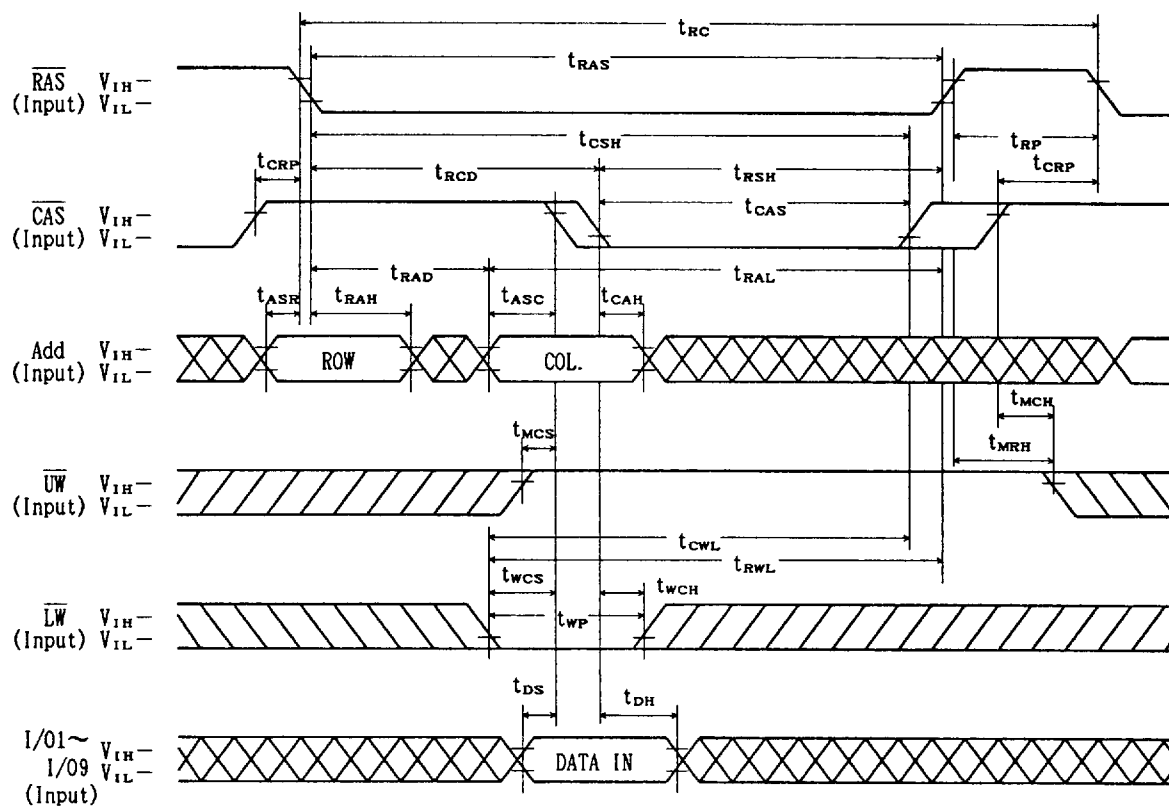
μPD42S16190,42S17190,42S18190

UPPER BYTE EARLY WRITE CYCLE



Note: $\overline{\text{OE}}$, I/O1~I/O9=Don't care

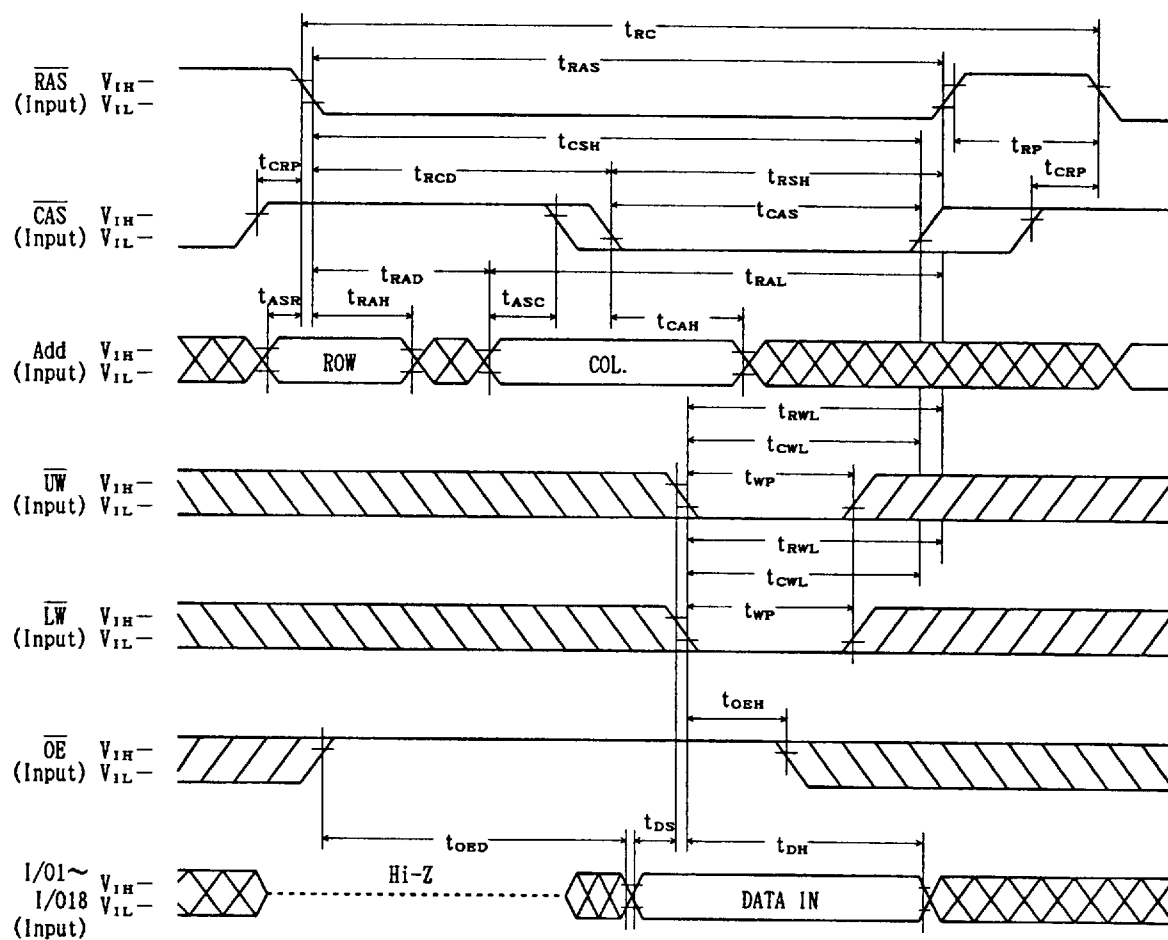
LOWER BYTE EARLY WRITE CYCLE



Note: $\overline{OE}$, I/O10~I/O18=Don't care

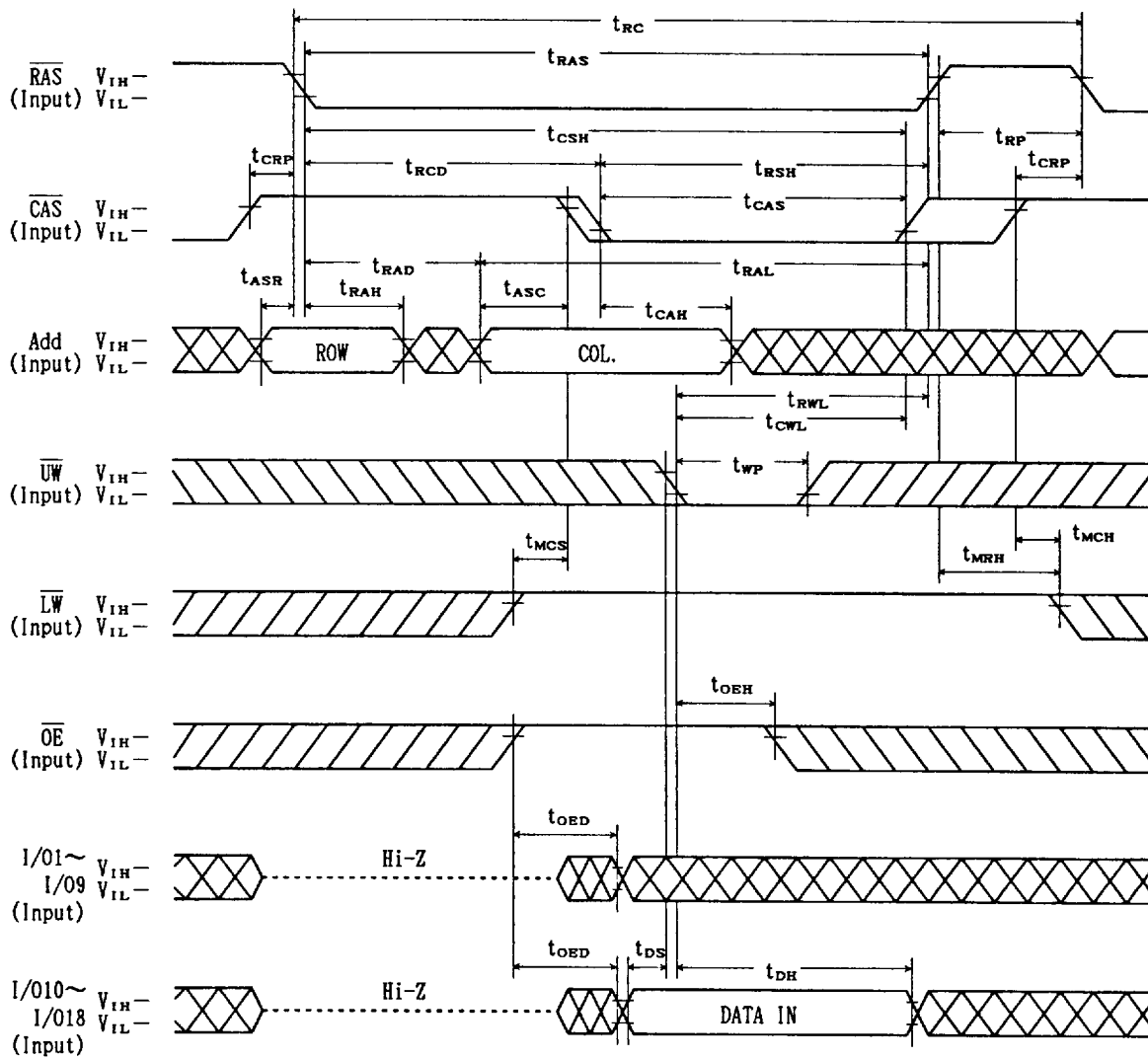
μPD42S16190,42S17190,42S18190

LATE WRITE CYCLE



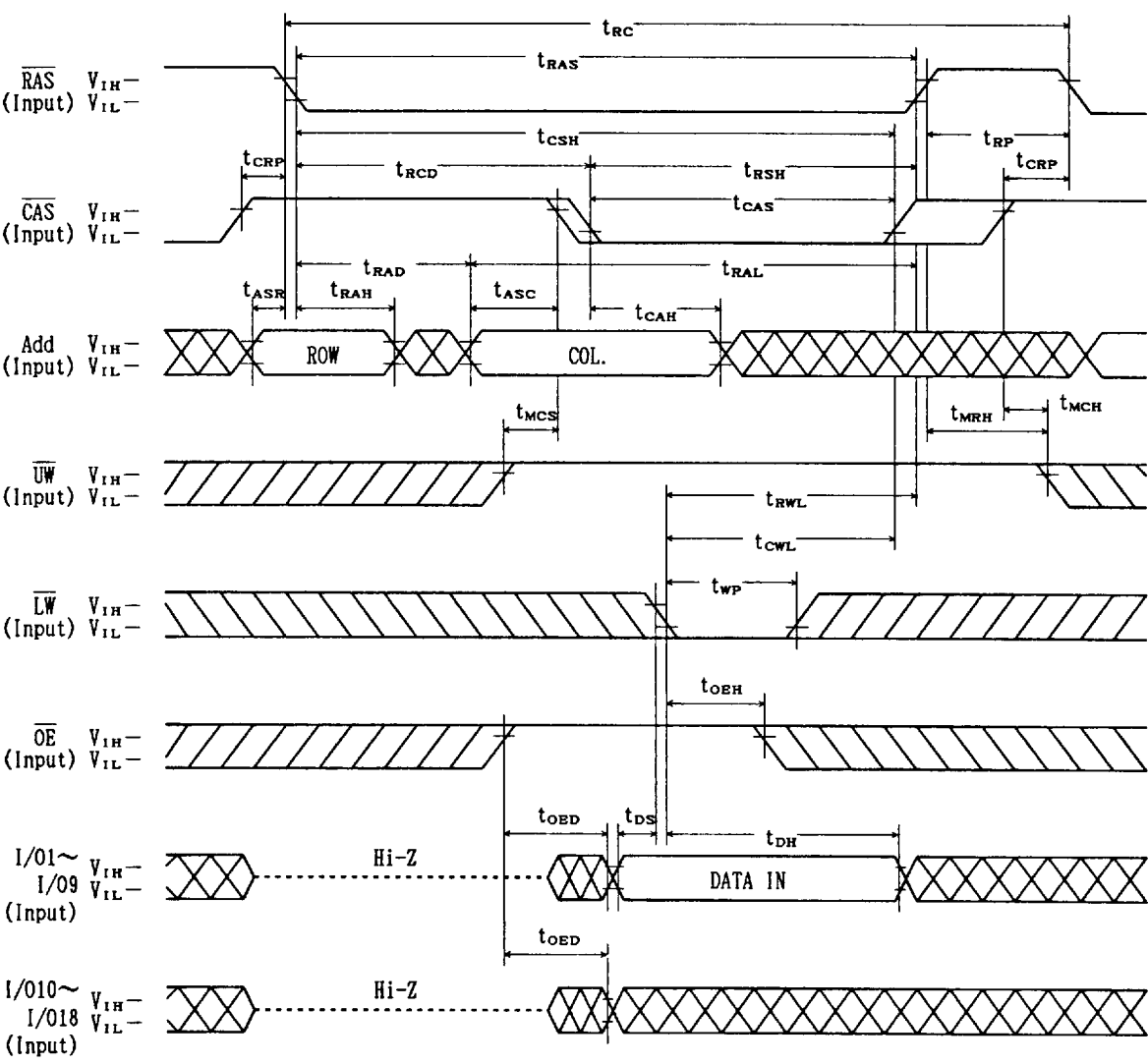
μ PD42S16190, 42S17190, 42S18190

UPPER BYTE LATE WRITE CYCLE

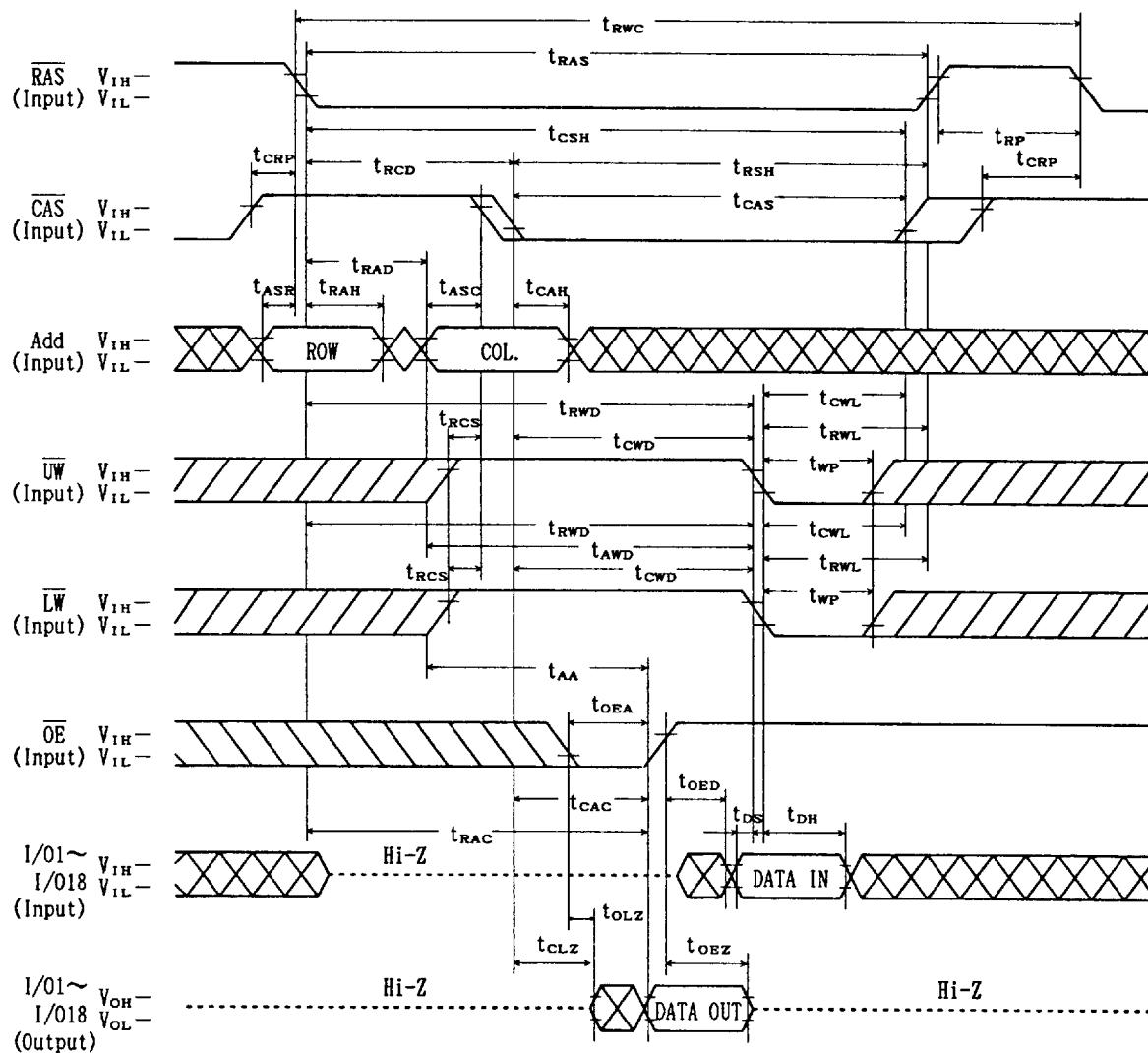


μPD42S16190,42S17190,42S18190

LOWER BYTE LATE WRITE CYCLE

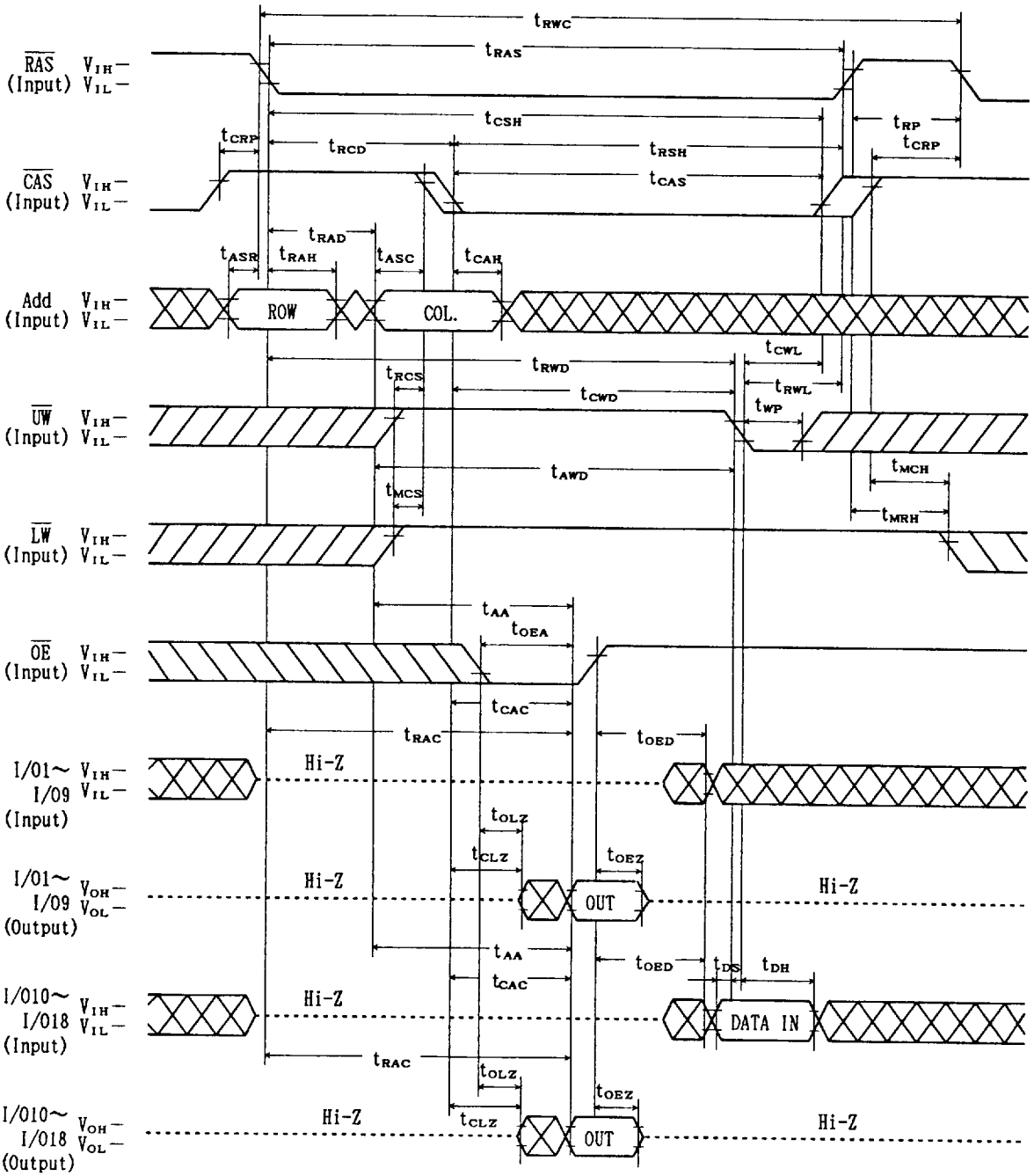


READ MODIFY WRITE CYCLE



μPD42S16190,42S17190,42S18190

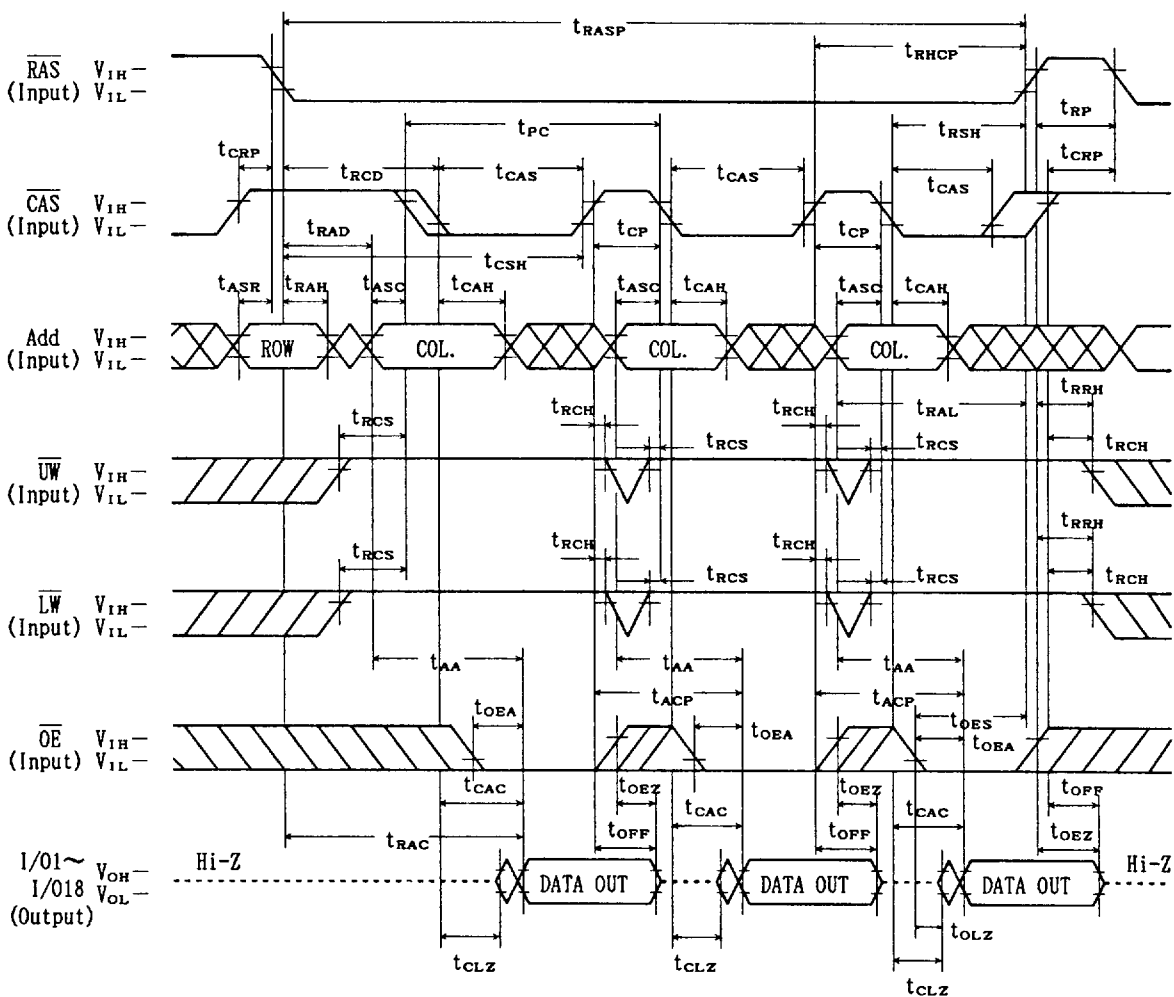
UPPER BYTE READ MODIFY WRITE CYCLE



[illegible]

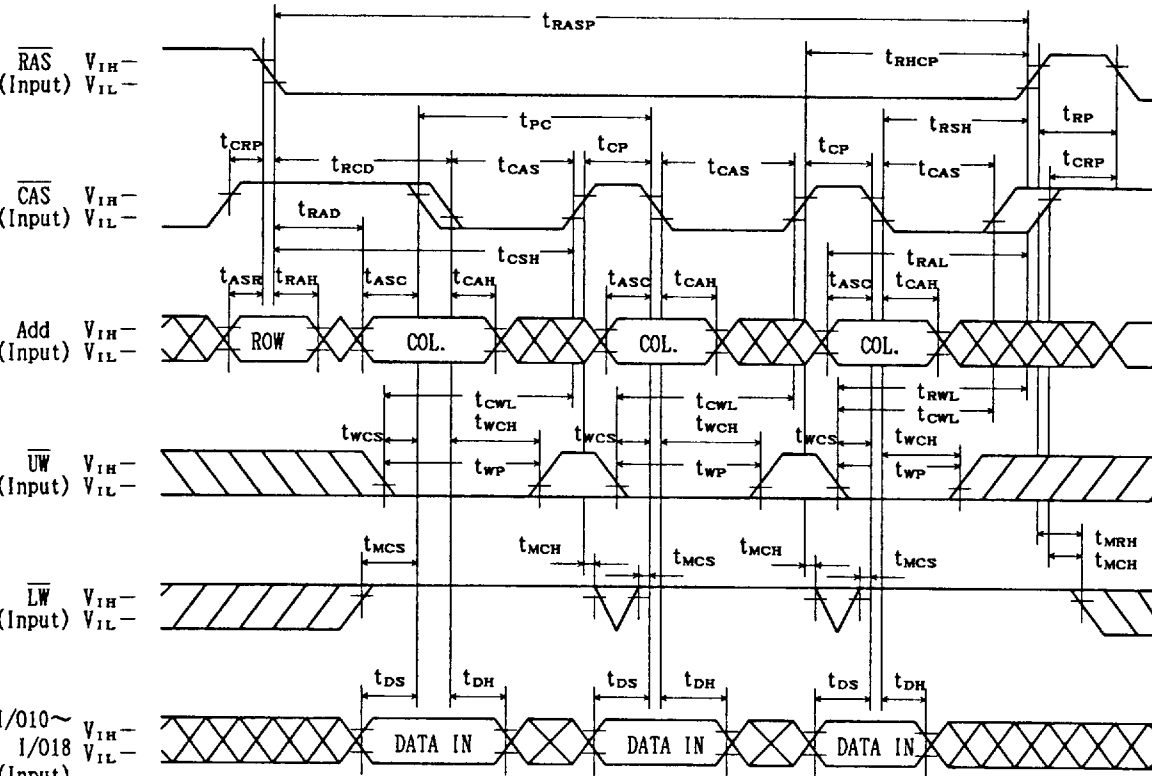
μ PD42S16190, 42S17190, 42S18190

FAST PAGE MODE READ CYCLE



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FAST PAGE MODE UPPER BYTE EARLY WRITE CYCLE

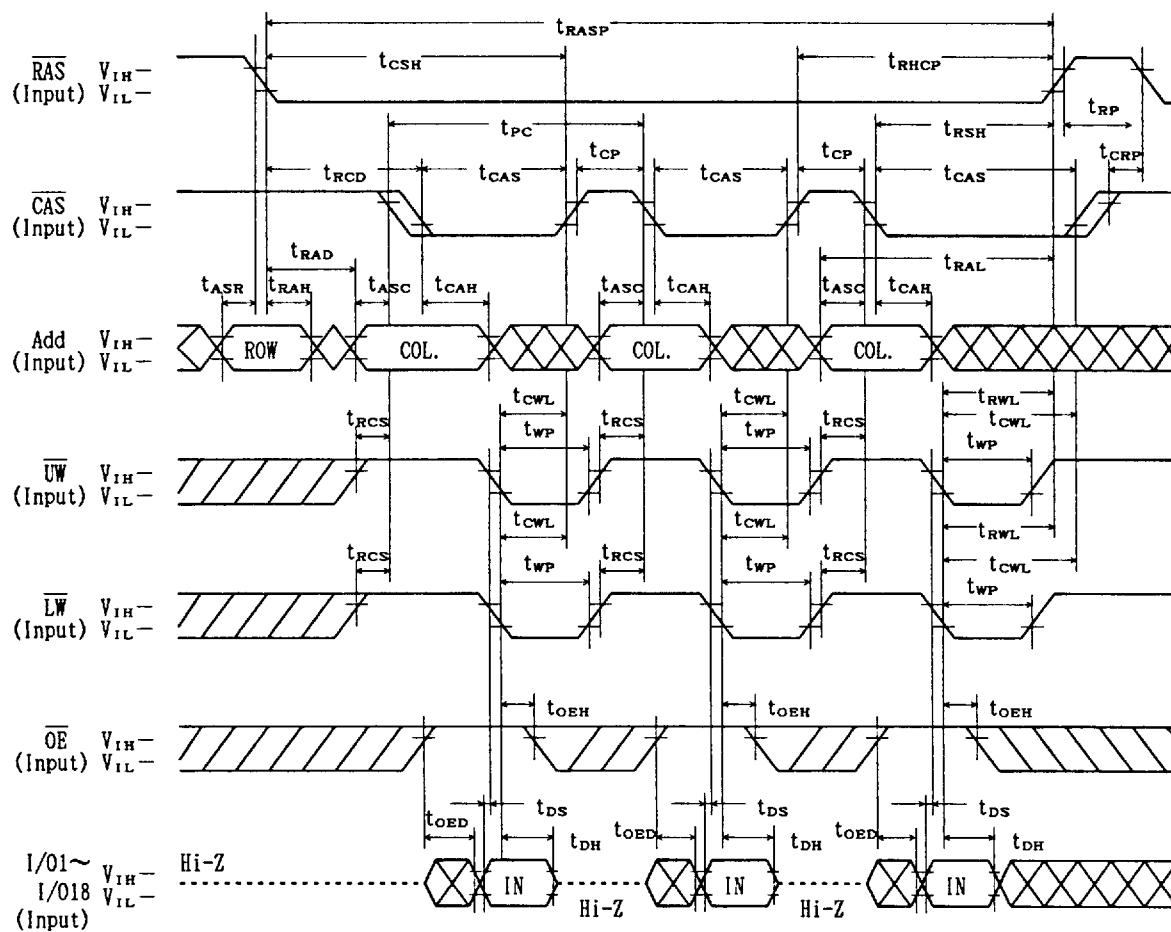


Note : $\overline{0E}$, 1/01~1/09=Don't care

441

μ PD42S16190, 42S17190, 42S18190

FAST PAGE MODE LATE WRITE CYCLE



The timing diagram illustrates the relationship between various control and data signals for the 64K1602 LCD module. The signals and their timing parameters are as follows:

- RAS (Input):** V_{IH} , V_{IL} . Timing parameters: t_{RASP} (total RAS pulse width), t_{CSH} (RAS setup time), t_{RHP} (RAS hold time), t_{RP} (RAS pulse width).
- CAS (Input):** V_{IH} , V_{IL} . Timing parameters: t_{PC} (CAS setup time), t_{CP} (CAS hold time), t_{CAS} (CAS pulse width), t_{RCD} (RAS to CAS delay), t_{ASC} (Address Setup time), t_{CAH} (Address Hold time), t_{RAD} (RAS to Address delay), t_{RAL} (RAS to Address delay).
- Add (Input):** V_{IH} , V_{IL} . Timing parameters: t_{ASR} (Address Setup time), t_{RAH} (Address Hold time), t_{ASC} (Address Setup time), t_{CAH} (Address Hold time), t_{ASR} (Address Setup time), t_{RAH} (Address Hold time), t_{ASC} (Address Setup time), t_{CAH} (Address Hold time), t_{ASR} (Address Setup time), t_{RAH} (Address Hold time), t_{ASC} (Address Setup time), t_{CAH} (Address Hold time).
- UW (Input):** V_{IH} , V_{IL} . Timing parameters: t_{RCS} (Row Setup time), t_{WPL} (Row Pulse Width), t_{MCH} (Row Setup time), t_{MCS} (Row Setup time), t_{MRH} (Row Hold time), t_{MCH} (Row Setup time).
- LW (Input):** V_{IH} , V_{IL} . Timing parameters: t_{MCS} (Row Setup time), t_{MCH} (Row Setup time), t_{MCS} (Row Setup time), t_{MCH} (Row Setup time), t_{MCS} (Row Setup time), t_{MCH} (Row Setup time), t_{MCS} (Row Setup time), t_{MCH} (Row Setup time).
- OE (Input):** V_{IH} , V_{IL} . Timing parameters: t_{OEH} (Output Enable Hold time), t_{OED} (Output Enable Delay time), t_{OEH} (Output Enable Hold time), t_{OED} (Output Enable Delay time), t_{OEH} (Output Enable Hold time), t_{OED} (Output Enable Delay time).
- I/O1~I/O9 (Input):** V_{IH} , V_{IL} . Timing parameters: t_{OED} (Output Enable Delay time), t_{DS} (Data Setup time), t_{DH} (Data Hold time), t_{OED} (Output Enable Delay time), t_{DS} (Data Setup time), t_{DH} (Data Hold time), t_{OED} (Output Enable Delay time), t_{DS} (Data Setup time), t_{DH} (Data Hold time).
- I/O10~I/O18 (Input):** V_{IH} , V_{IL} . Timing parameters: t_{OED} (Output Enable Delay time), t_{DS} (Data Setup time), t_{DH} (Data Hold time), t_{OED} (Output Enable Delay time), t_{DS} (Data Setup time), t_{DH} (Data Hold time), t_{OED} (Output Enable Delay time), t_{DS} (Data Setup time), t_{DH} (Data Hold time).

[illegible]

[illegible]

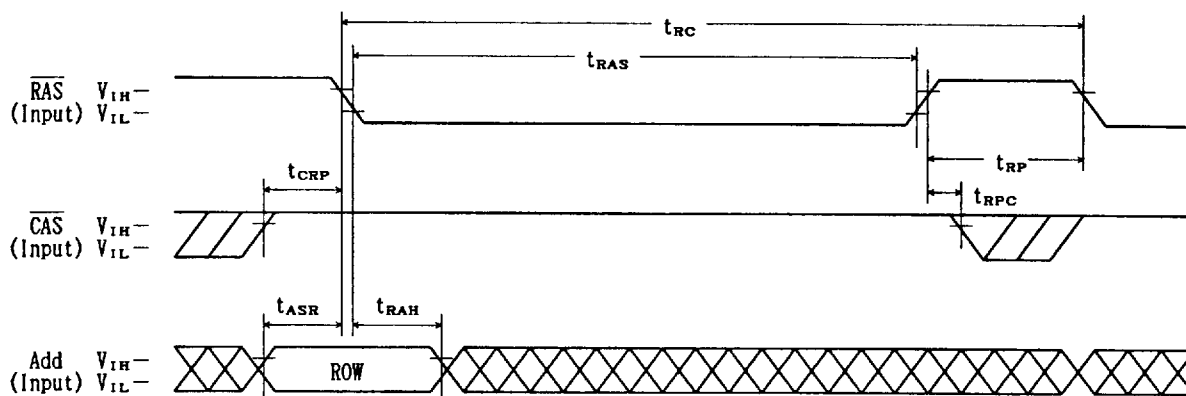
The diagram illustrates the timing relationships for the 64K1602 LCD controller. It shows the following signals and their timing parameters:

- RAS (Input):** V_{IH} , V_{IL} . Timing parameters: t_{RSP} (RAS pulse width), t_{CSH} (RAS setup time), t_{RSH} (RAS hold time), t_{RTP} (RAS to output delay), t_{CRP} (RAS to output delay).
- CAS (Input):** V_{IH} , V_{IL} . Timing parameters: t_{PRWC} (CAS pulse width), t_{RCD} (RAS to CAS delay), t_{CAS} (CAS setup/hold time), t_{CP} (CAS to output delay).
- Add (Input):** V_{IH} , V_{IL} . Timing parameters: t_{RAD} (RAS to address delay), t_{ASR} , t_{RAH} , t_{ASC} , t_{CAH} (address setup/hold time), t_{ASC} , t_{CAH} (address to output delay), t_{RAL} (address to output delay).
- UW (Input):** V_{IH} , V_{IL} . Timing parameters: t_{RCS} (RAS to UW delay), t_{CWD} (UW setup/hold time), t_{WP} (UW pulse width), t_{CPWD} (UW to output delay), t_{MCH} (UW to output delay).
- LW (Input):** V_{IH} , V_{IL} . Timing parameters: t_{MCS} (LW setup/hold time), t_{MCH} (LW to output delay).
- OE (Input):** V_{IH} , V_{IL} . Timing parameters: t_{AA} (OE pulse width), t_{CAC} (OE to output delay), t_{OED} (OE to output delay), t_{CLZ} (OE to output delay), t_{OEZ} (OE to output delay).
- I/O Signals:**
 - I/O1~I/O9 (Output):** V_{OH} , V_{OL} . Timing parameters: t_{OEA} (OE to output delay), t_{DHA} (OE to output delay), t_{DSD} (OE to output delay).
 - I/O1~I/O9 (Input):** V_{IH} , V_{IL} . Timing parameters: t_{RAC} (OE to output delay), t_{DHA} (OE to output delay), t_{DSD} (OE to output delay).
 - I/O10~I/O18 (Output):** V_{OH} , V_{OL} . Timing parameters: t_{DHA} (OE to output delay), t_{DSD} (OE to output delay).
 - I/O10~I/O18 (Input):** V_{IH} , V_{IL} . Timing parameters: t_{DHA} (OE to output delay), t_{DSD} (OE to output delay).

[illegible]

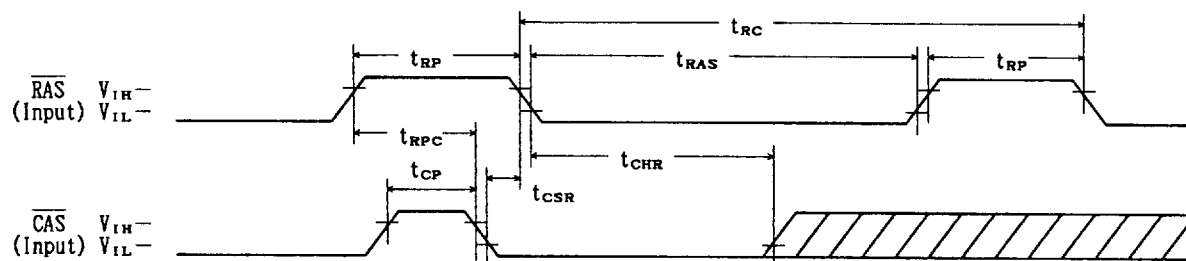
μ PD42S16190, 42S17190, 42S18190

RAS ONLY REFRESH CYCLE



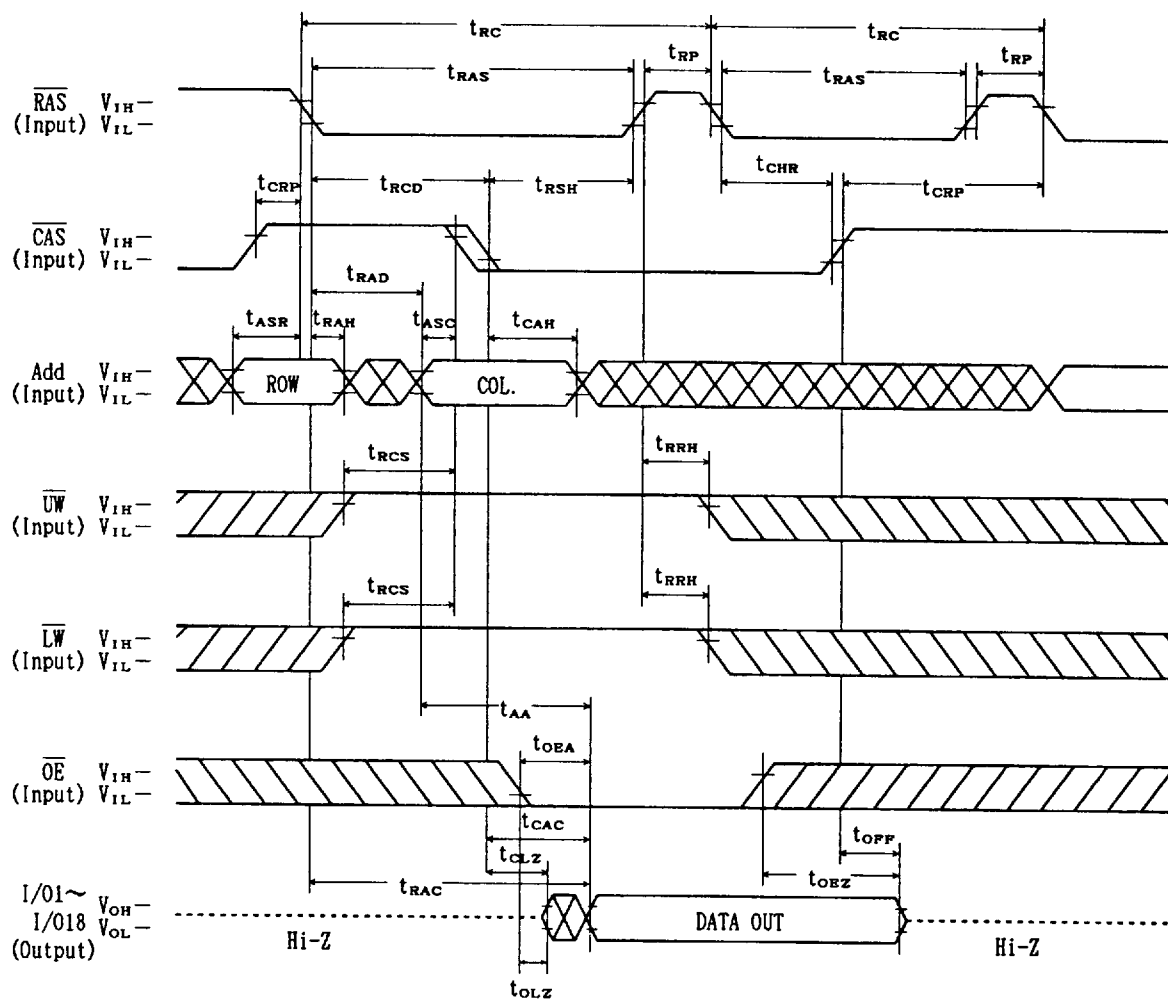
Note : I/O1~I/O18=Hi-Z

CAS BEFORE RAS REFRESH CYCLE

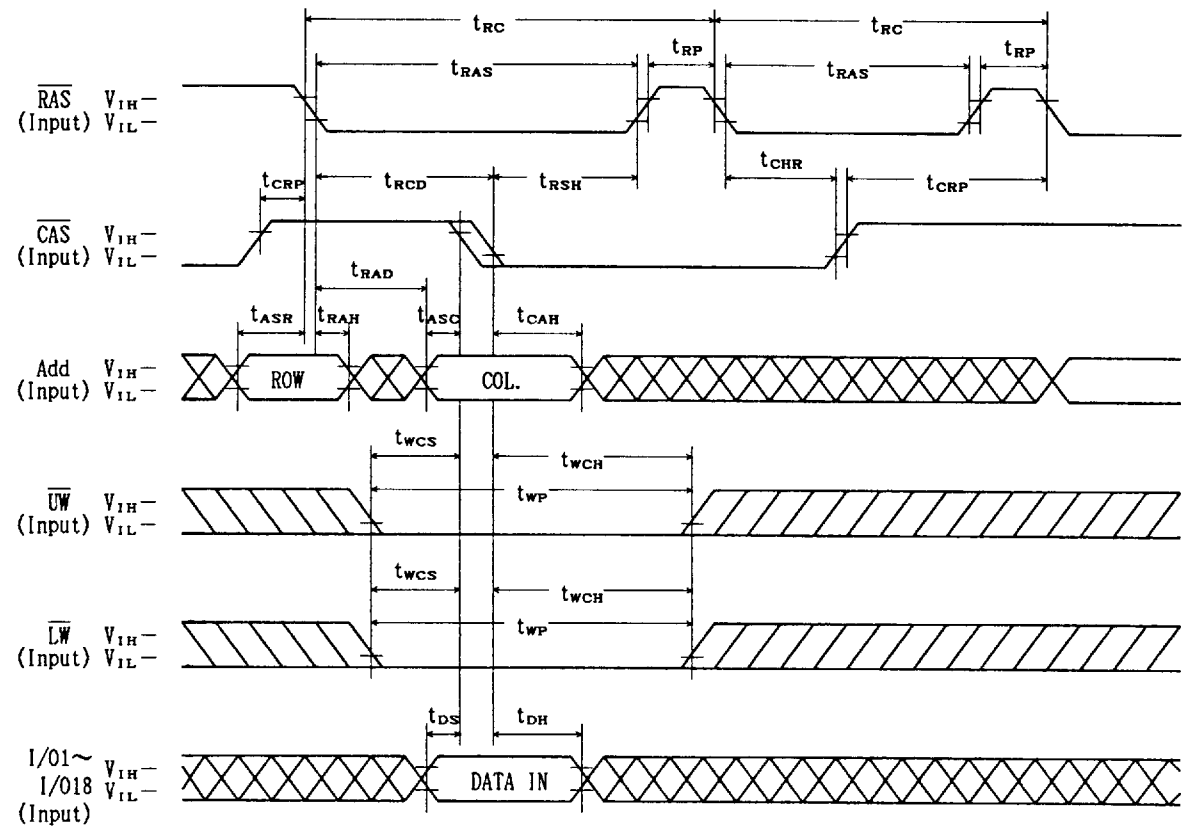


Note : Add=Don't care, I/O1~I/O18=Hi-Z

HIDDEN REFRESH CYCLE (READ)

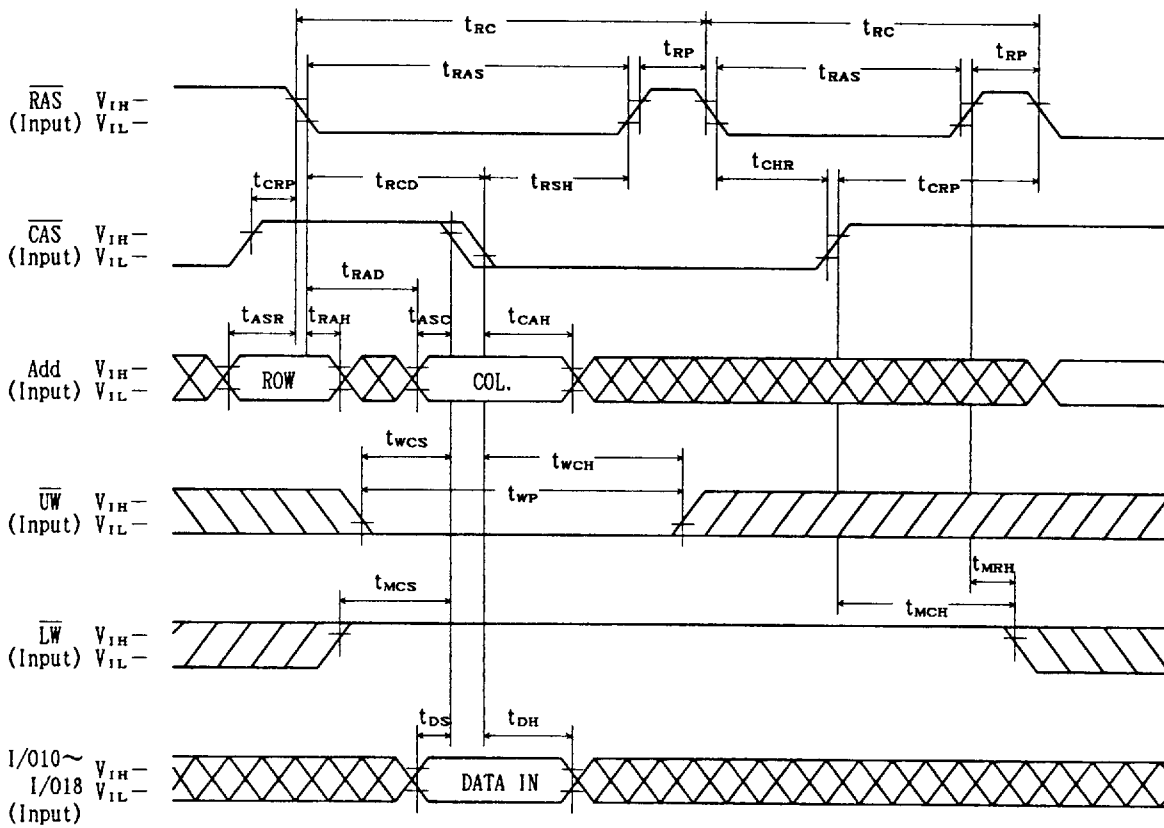


HIDDEN REFRESH CYCLE (WRITE)



Note : $\overline{OE}$ = Don't care

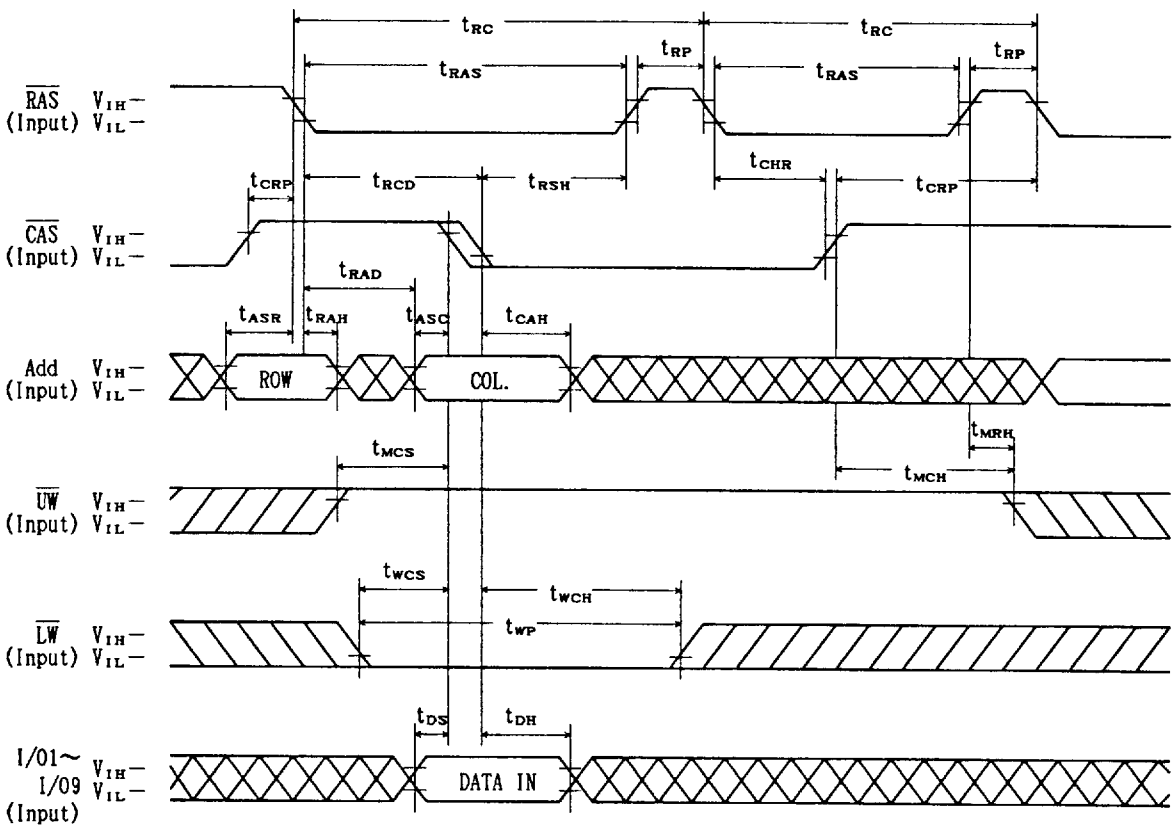
HIDDEN REFRESH CYCLE (UPPER BYTE WRITE)



Note: $\overline{OE}$, I/O1~I/O9=Don't care

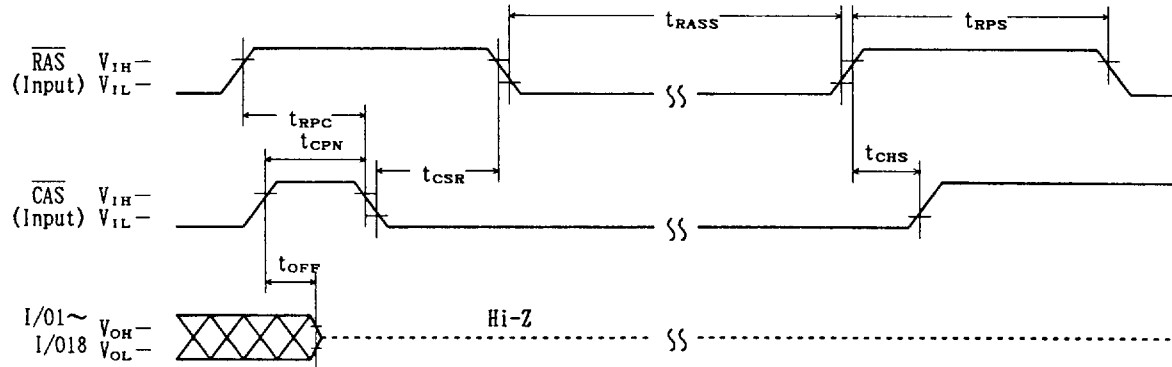
μPD42S16190,42S17190,42S18190

HIDDEN REFRESH CYCLE (LOWER BYTE WRITE)



Note : $\overline{OE}$, I/O10~I/O18=Don't care

CAS BEFORE RAS SELF REFRESH CYCLE



3. PACKAGE DRAWINGS

26 PIN PLASTIC SOJ (300mil)	24 Leads	495
28 PIN PLASTIC SOJ (400mil)	24 Leads	496
28 PIN PLASTIC SOJ (400mil)	28 Leads	497
32 PIN PLASTIC SOJ (400mil)		498
42 PIN PLASTIC SOJ (400mil)		499
26 PIN PLASTIC TSOP (300mil) *	24 Leads	500
26 PIN PLASTIC TSOP (300mil) *	24 Leads Reverse bent	501
28 PIN PLASTIC TSOP (400mil)	24 Leads	502
28 PIN PLASTIC TSOP (400mil)	24 Leads Reverse bent	503
28 PIN PLASTIC TSOP (400mil)	28 Leads	504
28 PIN PLASTIC TSOP (400mil)	28 Leads Reverse bent	505
32 PIN PLASTIC TSOP (400mil)		506
32 PIN PLASTIC TSOP (400mil)	Reverse bent	507
50 PIN PLASTIC TSOP (400mil)	44 Leads	508
50 PIN PLASTIC TSOP (400mil)	44 Leads Reverse bent	509
24 PIN PLASTIC ZIP (475mil)		510
28 PIN PLASTIC ZIP (475mil)		511
32 PIN PLASTIC ZIP (475mil)		512

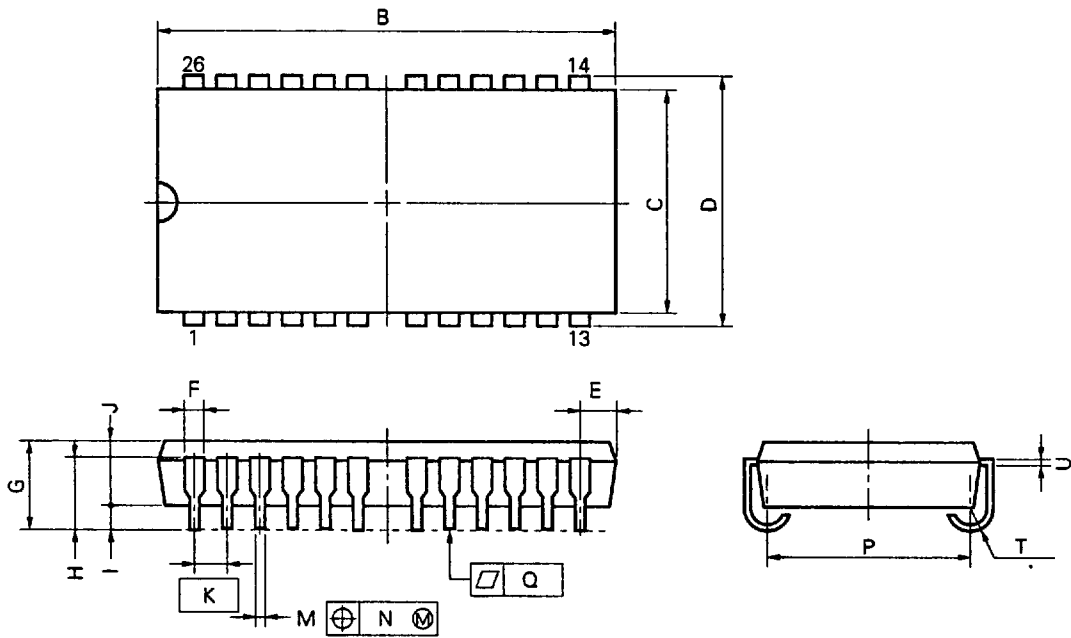
* : under development

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494

26 PIN PLASTIC SOJ (300mil)
24 Leads

NEC Cord:S26LA-300A

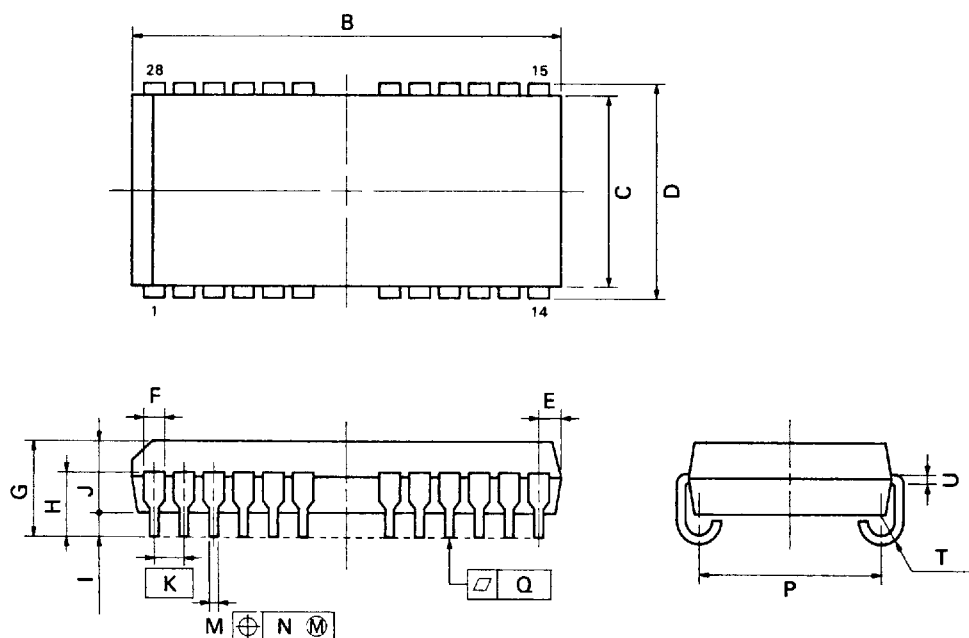


NOTE
Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

S26LA-300A		
ITEM	MILLIMETERS	INCHES
B	17.1 ^{+0.25} _{-0.05}	0.673 ^{+0.010} _{-0.002}
C	7.62	0.300
D	8.47±0.2	0.333 ^{+0.009} _{-0.008}
E	1.03±0.15	0.041 ^{+0.006} _{-0.007}
F	0.74	0.029
G	3.5±0.2	0.138±0.008
H	2.545±0.2	0.100±0.008
I	0.8 MIN.	0.031 MIN.
J	2.6	0.102
K	1.27 (T.P.)	0.050 (T.P.)
M	0.40±0.10	0.016 ^{+0.004} _{-0.005}
N	0.12	0.005
P	6.73±0.20	0.265±0.008
Q	0.10	0.004
T	R 0.85	R 0.033
U	0.20 ^{+0.10} _{-0.05}	0.008 ^{+0.004} _{-0.002}

28 PIN PLASTIC SOJ (400mil)
24 Leads

NEC Cord:P28LE-400A



P28LE-400A

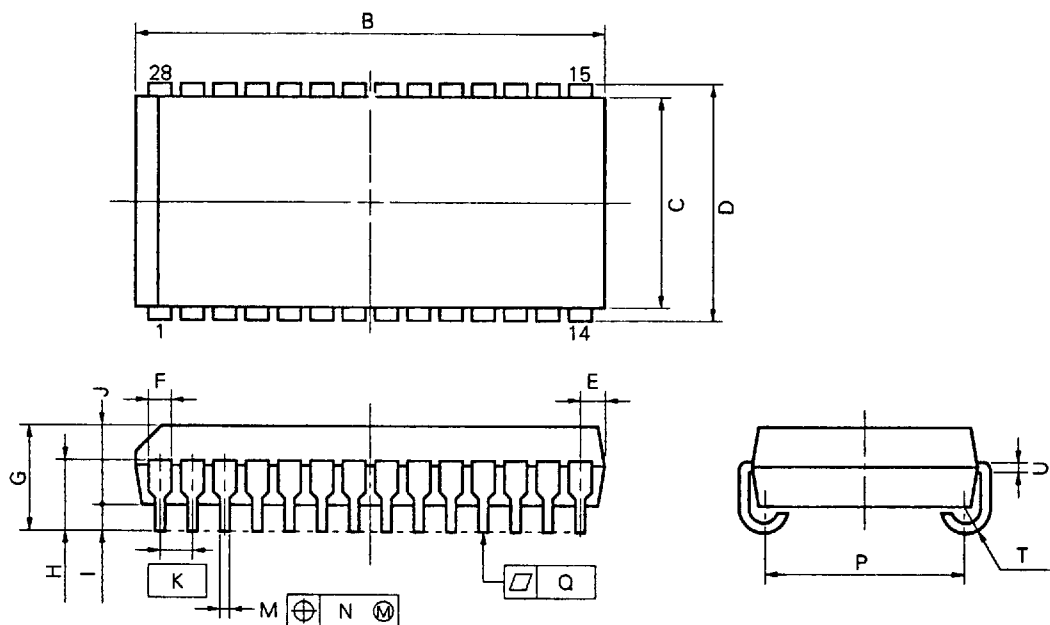
NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
B	18.67 ^{+0.25} _{-0.35}	0.735 ^{+0.008} _{-0.013}
C	10.16	0.400
D	11.18 ^{+0.2} _{-0.2}	0.440 ^{+0.008} _{-0.007}
E	1.08 ^{+0.15} _{-0.15}	0.043 ^{+0.006} _{-0.007}
F	0.7	0.028
G	3.5 ^{+0.2} _{-0.2}	0.138 ^{+0.008} _{-0.008}
H	2.4 ^{+0.2} _{-0.2}	0.094 ^{+0.008} _{-0.008}
I	0.8 MIN.	0.031 MIN.
J	2.6	0.102
K	1.27 (T.P.)	0.050 (T.P.)
M	0.40 ^{+0.10} _{-0.10}	0.016 ^{+0.004} _{-0.004}
N	0.12	0.005
P	9.40 ^{+0.20} _{-0.20}	0.370 ^{+0.008} _{-0.007}
Q	0.15	0.006
T	R0.85	R0.033
U	0.20 ^{+0.10} _{-0.10}	0.008 ^{+0.004} _{-0.004}

28 PIN PLASTIC SOJ (400mil)
28 Leads

NEC Cord:P28LE-400A1



NOTE

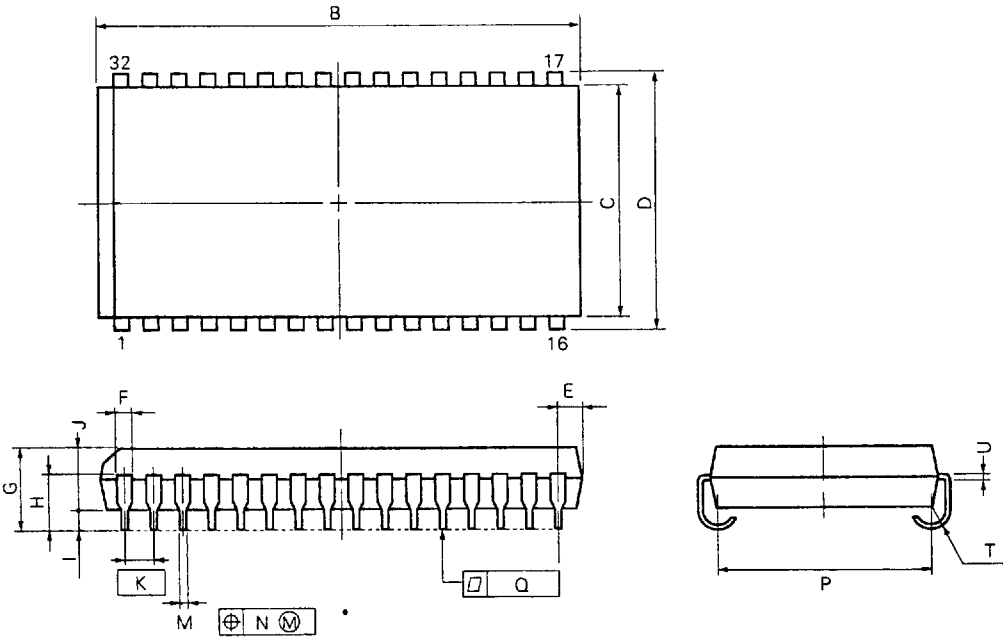
Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

P28LE-400A1

ITEM	MILLIMETERS	INCHES
B	$18.67^{+0.2}_{-0.35}$	$0.735^{+0.008}_{-0.013}$
C	10.16	0.400
D	11.18 ± 0.2	$0.440^{+0.008}_{-0.007}$
E	1.08 ± 0.15	$0.043^{+0.006}_{-0.007}$
F	0.74	0.029
G	3.5 ± 0.2	$0.138^{+0.008}_{-0.007}$
H	2.545 ± 0.2	0.100 ± 0.008
I	0.8 MIN	0.031 MIN.
J	2.6	0.102
K	1.27 (T.P.)	0.050 (T.P.)
M	0.40 ± 0.10	$0.016^{+0.004}_{-0.005}$
N	0.12	0.005
P	9.40 ± 0.20	$0.370^{+0.008}_{-0.007}$
Q	0.10	0.004
T	R 0.85	R 0.033
U	$0.20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$

32 PIN PLASTIC SOJ (400mil)

NEC Cord:P32LE-400A

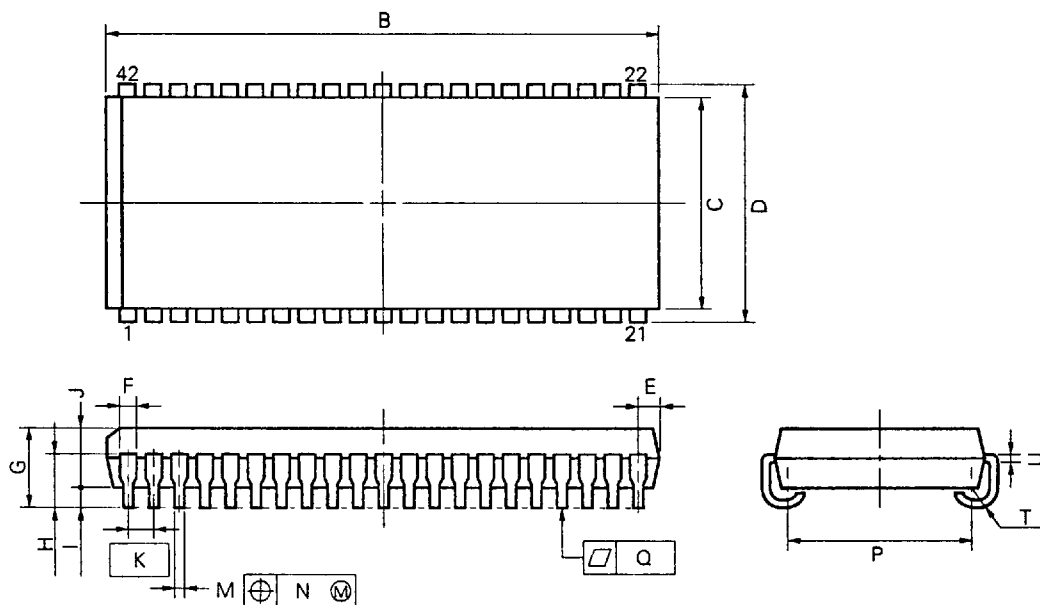


NOTE
Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition

P32LE-400A		
ITEM	MILLIMETERS	INCHES
B	21.06±0.2	0.829±0.008
C	10.16	0.400
D	11.18±0.2	0.440±0.008
E	1.005±0.1	0.040 ^{+0.004} _{-0.005}
F	0.74	0.029
G	3.5±0.2	0.138±0.008
H	2.545±0.2	0.100±0.008
I	0.8 MIN	0.031 MIN
J	2.6	0.102
K	1.27 (T.P.)	0.050 (T.P.)
M	0.40±0.10	0.016 ^{+0.004} _{-0.005}
N	0.12	0.005
P	9.4±0.20	0.370±0.008
Q	0.1	0.004
T	R 0.85	R 0.033
U	0.20 ^{+0.10} _{-0.02}	0.008 ^{+0.004} _{-0.002}

42 PIN PLASTIC SOJ (400mil)

NEC Cord:P42LE-400A

**NOTE**

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

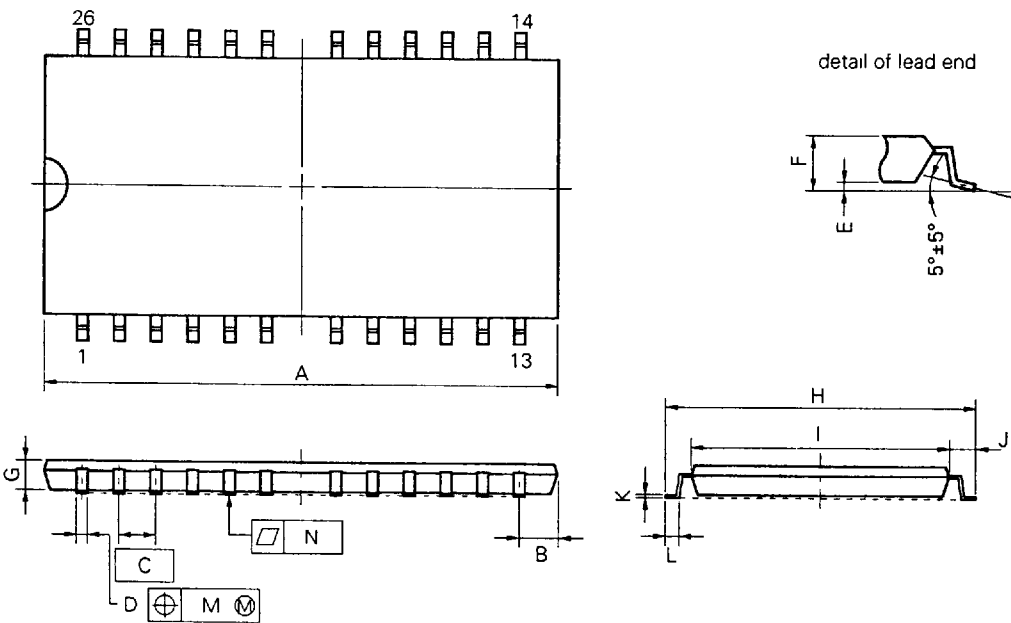
P42LE-400A

ITEM	MILLIMETERS	INCHES
B	$27.56^{+0.2}_{-0.35}$	$1.085^{+0.008}_{-0.014}$
C	10.16	0.400
D	11.18 ± 0.2	0.440 ± 0.008
E	1.08 ± 0.15	$0.043^{+0.006}_{-0.007}$
F	0.74	0.029
G	3.5 ± 0.2	0.138 ± 0.008
H	2.545 ± 0.2	0.100 ± 0.008
I	0.8 MIN.	0.031 MIN.
J	2.6	0.102
K	1.27 (T.P.)	0.050 (T.P.)
M	0.40 ± 0.10	$0.016^{+0.004}_{-0.005}$
N	0.12	0.005
P	9.4 ± 0.20	0.370 ± 0.008
Q	0.10	0.004
T	R 0.85	R 0.033
U	$0.20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$

26 PIN PLASTIC TSOP (300mil) *
 24 Leads

* : under development

NEC Cord:S26G3-50-7JD



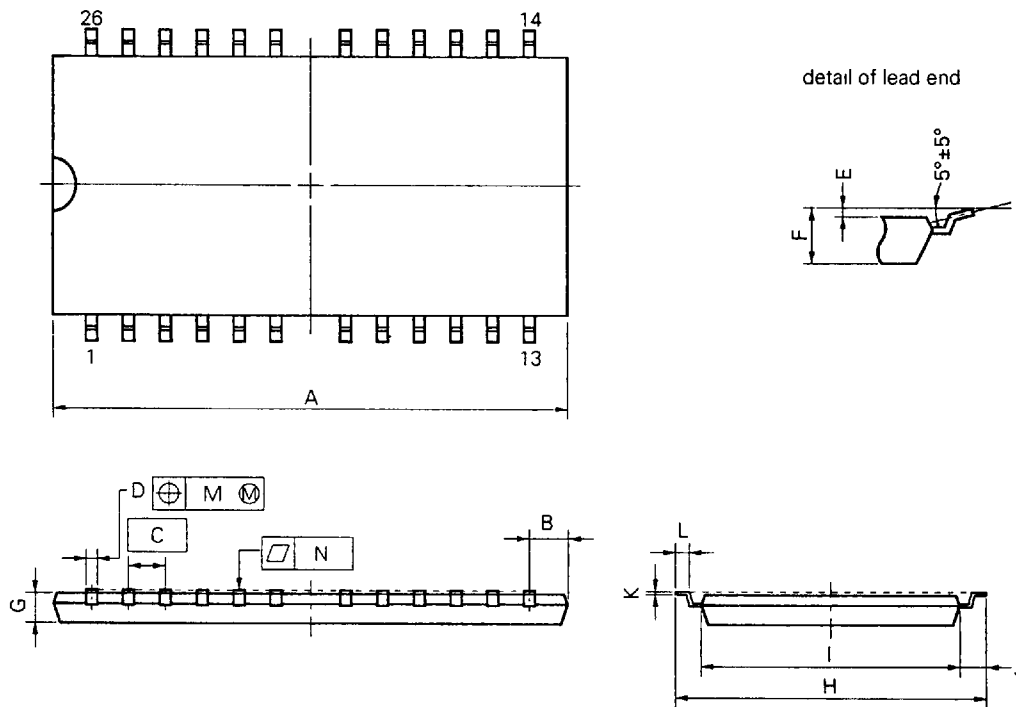
NOTE
 Each lead centerline is located within 0.21 mm (0.009 inch) of its true position (T.P.) at maximum material condition.

S26G3-50-7JD		
ITEM	MILLIMETERS	INCHES
A	17.40 MAX.	0.685 MAX.
B	1.06 MAX.	0.042 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	0.40±0.10	0.016 ^{+0.004} _{-0.005}
E	0.05±0.05	0.002±0.002
F	1.1 MAX.	0.044 MAX.
G	0.97	0.038
H	9.22±0.2	0.363±0.008
I	7.62±0.1	0.300±0.004
J	0.8±0.2	0.031 ^{+0.009} _{-0.008}
K	0.125 ^{+0.10} _{-0.05}	0.005 ^{+0.004} _{-0.002}
L	0.5±0.1	0.020 ^{+0.004} _{-0.005}
M	0.21	0.009
N	0.10	0.004

26 PIN PLASTIC TSOP (300mil) *
24 Leads Reverse bent

* : under development

NEC Cord:S26G3-50-7KD



NOTE

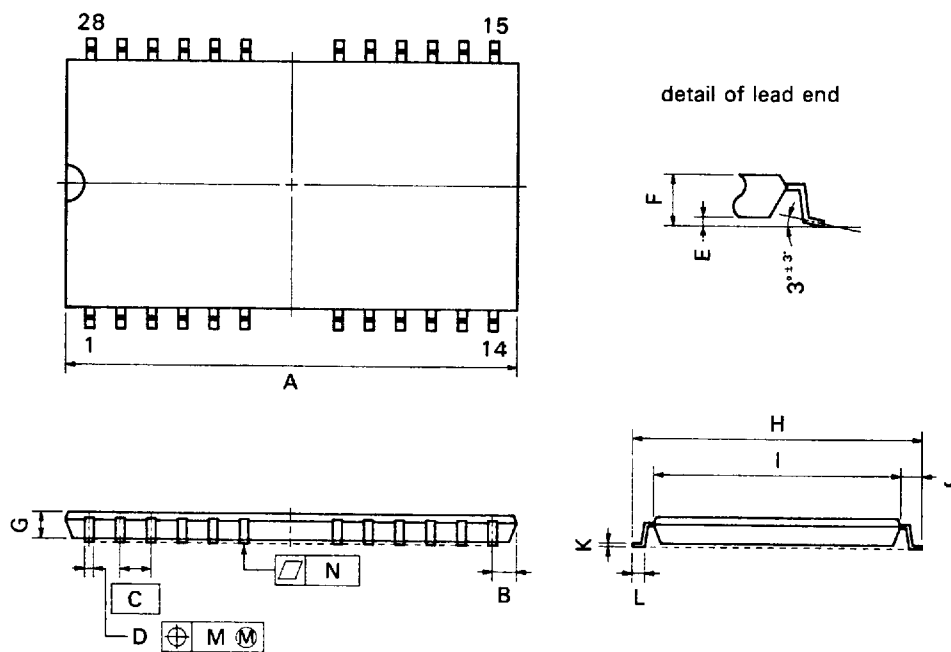
Each lead centerline is located within 0.21 mm (0.009 inch) of its true position (T.P) at maximum material condition

S26G3-50-7KD

ITEM	MILLIMETERS	INCHES
A	17.40 MAX.	0.685 MAX.
B	1.06 MAX.	0.042 MAX.
C	1.27 (T P)	0.050 (T.P.)
D	0.40±0.10	0.016 ^{+0.004} _{-0.005}
E	0.05±0.05	0.002±0.002
F	1.1 MAX.	0.044 MAX.
G	0.97	0.038
H	9.22±0.2	0.363±0.008
I	7.62±0.1	0.300±0.004
J	0.8±0.2	0.031 ^{+0.009} _{-0.008}
K	0.125 ^{+0.10} _{-0.05}	0.005 ^{+0.004} _{-0.002}
L	0.5±0.1	0.020 ^{+0.004} _{-0.005}
M	0.21	0.009
N	0.10	0.004

28 PIN PLASTIC TSOP (400mil)
24 Leads

NEC Cord:S28G5-50-7JD1



NOTE

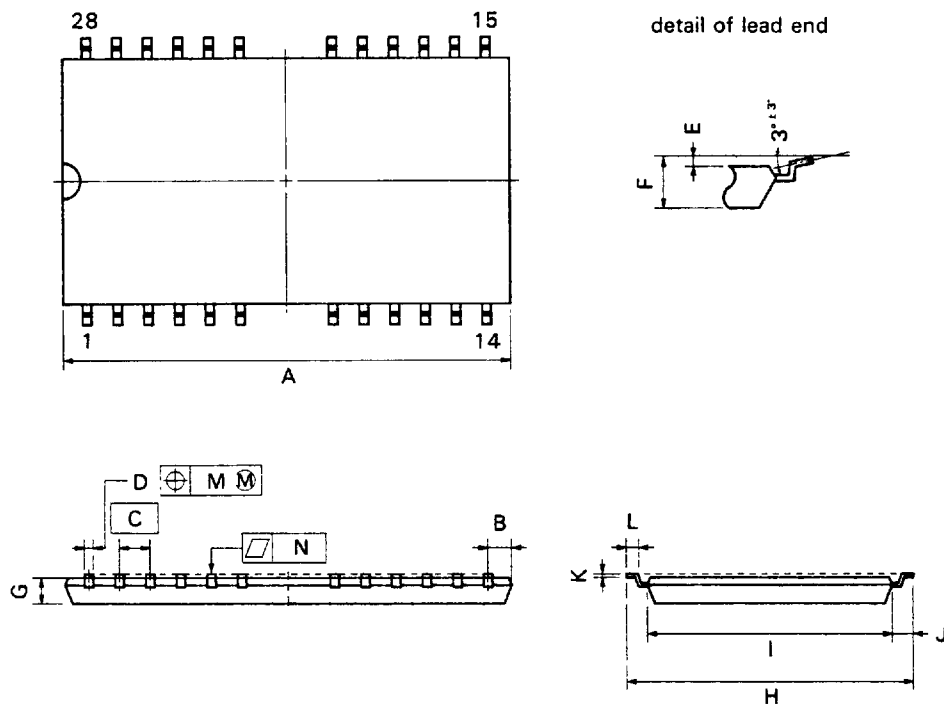
Each lead centerline is located within 0.21 mm (0.009 inch) of its true position (T.P.) at maximum material condition.

S28G5-50-7JD1

ITEM	MILLIMETERS	INCHES
A	18.81 MAX.	0.741 MAX.
B	1.15 MAX.	0.046 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	0.40 ± 0.10	0.016 ± 0.004
E	0.05 ± 0.05	0.002 ± 0.002
F	1.1 MAX.	0.044 MAX.
G	0.97	0.038
H	11.76 ± 0.2	0.463 ± 0.008
I	10.16 ± 0.1	0.400 ± 0.004
J	0.8 ± 0.2	0.031 ± 0.008
K	0.125 ± 0.10	0.005 ± 0.004
L	0.5 ± 0.1	0.020 ± 0.004
M	0.21	0.009
N	0.10	0.004

28 PIN PLASTIC TSOP (400mil)
24 Leads Reverse bent

NEC Cord:S28G5-50-7KD1



NOTE

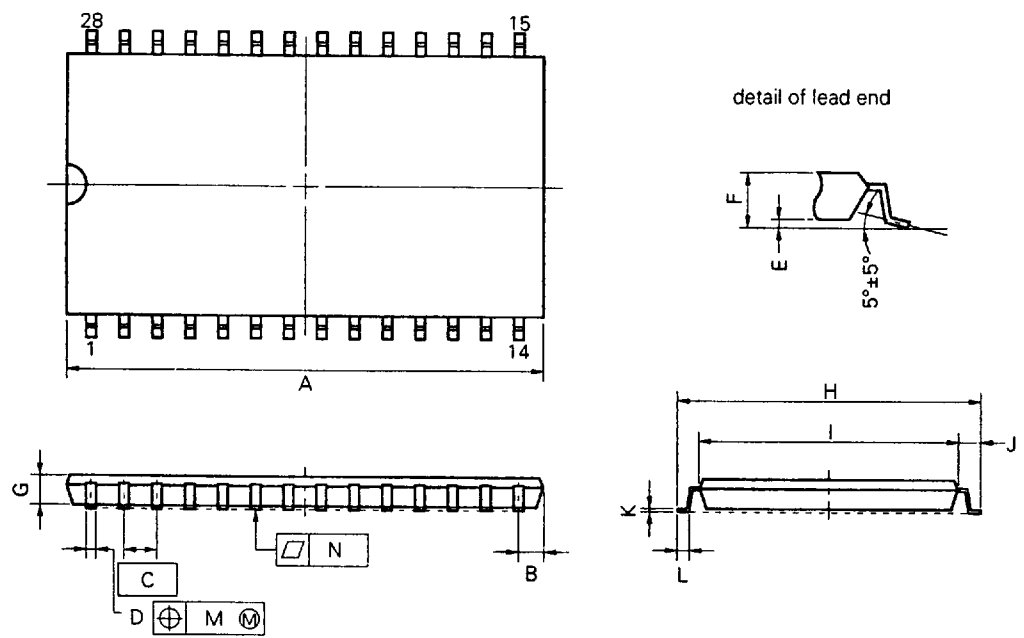
Each lead centerline is located within 0.21 mm (0.009 inch) of its true position (T.P.) at maximum material condition.

S28G5-50-7KD1

ITEM	MILLIMETERS	INCHES
A	18.81 MAX.	0.741 MAX.
B	1.15 MAX.	0.046 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	0.40 $\pm$ 0.10	0.016 $\pm$ 0.004
E	0.05 $\pm$ 0.05	0.002 $\pm$ 0.002
F	1.1 MAX.	0.044 MAX.
G	0.97	0.038
H	11.76 $\pm$ 0.2	0.463 $\pm$ 0.008
I	10.16 $\pm$ 0.1	0.400 $\pm$ 0.004
J	0.8 $\pm$ 0.2	0.031 $\pm$ 0.008
K	0.125 $\pm$ 0.02	0.005 $\pm$ 0.001
L	0.5 $\pm$ 0.1	0.020 $\pm$ 0.004
M	0.21	0.009
N	0.10	0.004

28 PIN PLASTIC TSOP (400mil)
28 Leads

NEC Cord:S28G5-50-7JD2

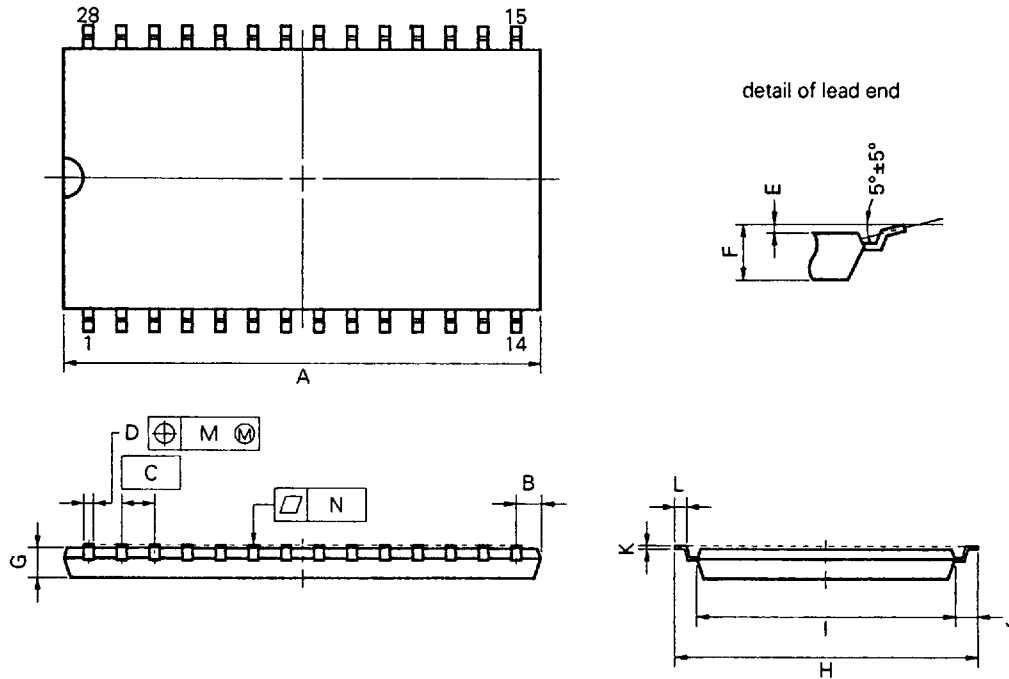


NOTE
Each lead centerline is located within 0.21 mm (0.009 inch) of its true position (T.P.) at maximum material condition.

S28G5-50-7JD2		
ITEM	MILLIMETERS	INCHES
A	18.81 MAX.	0.741 MAX.
B	1.15 MAX.	0.046 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	0.40±0.10	0.016 ^{+0.004} _{-0.005}
E	0.05±0.05	0.002±0.002
F	1.1 MAX.	0.044 MAX.
G	0.97	0.038
H	11.76±0.2	0.463±0.008
I	10.16±0.1	0.400±0.004
J	0.8±0.2	0.031 ^{+0.009} _{-0.008}
K	0.125 ^{+0.10} _{-0.05}	0.005 ^{+0.004} _{-0.002}
L	0.5±0.15	0.020 ^{+0.006} _{-0.007}
M	0.21	0.009
N	0.10	0.004

28 PIN PLASTIC TSOP (400mil)
28 Leads Reverse bent

NEC Cord:S28G5-50-7KD2



NOTE

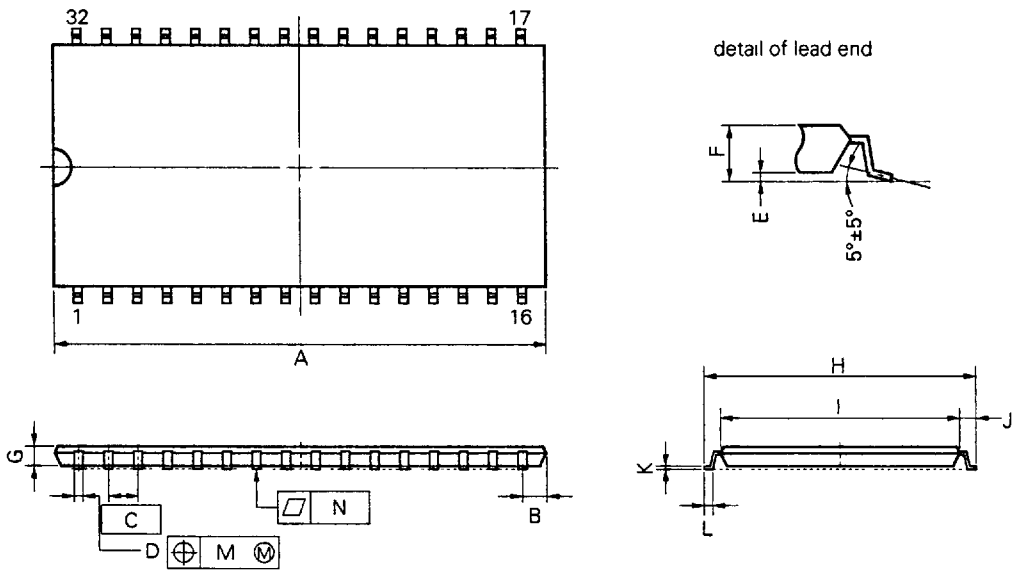
Each lead centerline is located within 0.21 mm (0.009 inch) of its true position (T.P.) at maximum material condition.

S28G5-50-7KD2

ITEM	MILLIMETERS	INCHES
A	18.81 MAX.	0.741 MAX.
B	1.15 MAX.	0.046 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	0.40±0.10	0.016 ^{+0.004} _{-0.005}
E	0.05±0.05	0.002±0.002
F	1.1 MAX.	0.044 MAX.
G	0.97	0.038
H	11.76±0.2	0.463±0.008
I	10.16±0.1	0.400±0.004
J	0.8±0.2	0.031 ^{+0.009} _{-0.008}
K	0.125 ^{+0.10} _{-0.05}	0.005 ^{+0.004} _{-0.002}
L	0.5±0.15	0.020 ^{+0.006} _{-0.007}
M	0.21	0.009
N	0.10	0.004

32 PIN PLASTIC TSOP (400mil)

NEC Cord:S32G5-50-7JD1

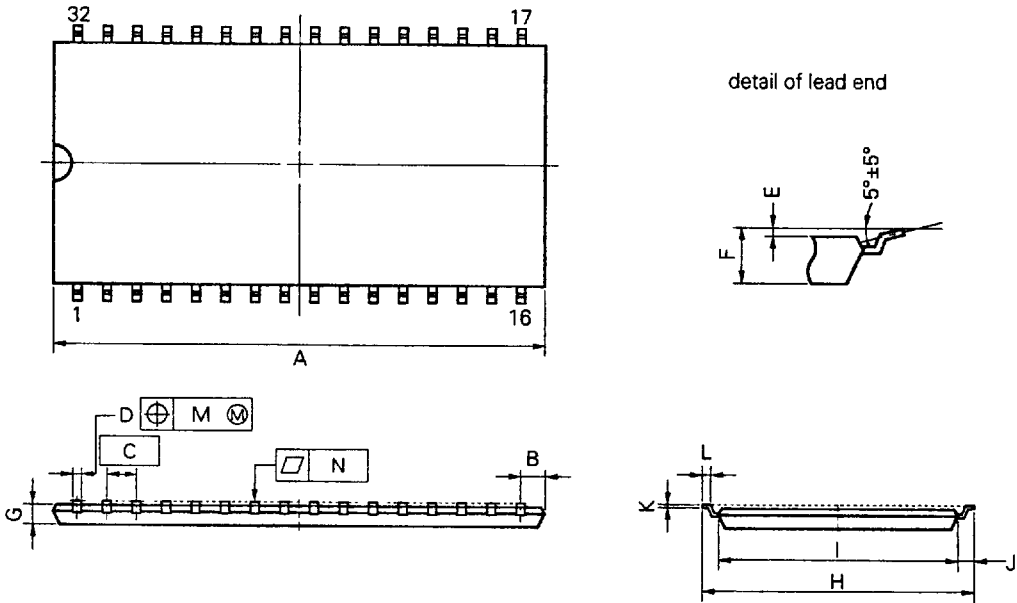


NOTE
Each lead centerline is located within 0.21 mm (0.009 inch) of its true position (T.P.) at maximum material condition.

S32G5-50-7JD1		
ITEM	MILLIMETERS	INCHES
A	21.17 MAX.	0.834 MAX.
B	1.06 MAX.	0.042 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	0.40±0.10	0.016 ^{+0.004} _{-0.005}
E	0.05±0.05	0.002±0.002
F	1.1 MAX.	0.044 MAX.
G	0.97	0.038
H	11.76±0.2	0.463±0.008
I	10.16±0.1	0.400±0.004
J	0.8±0.2	0.031 ^{+0.009} _{-0.008}
K	0.125 ^{+0.10} _{-0.05}	0.005 ^{+0.004} _{-0.002}
L	0.5±0.15	0.020 ^{+0.006} _{-0.007}
M	0.21	0.009
N	0.10	0.004

32 PIN PLASTIC TSOP (400mil)
Reverse bent

NEC Cord:S32G5-50-7KD1

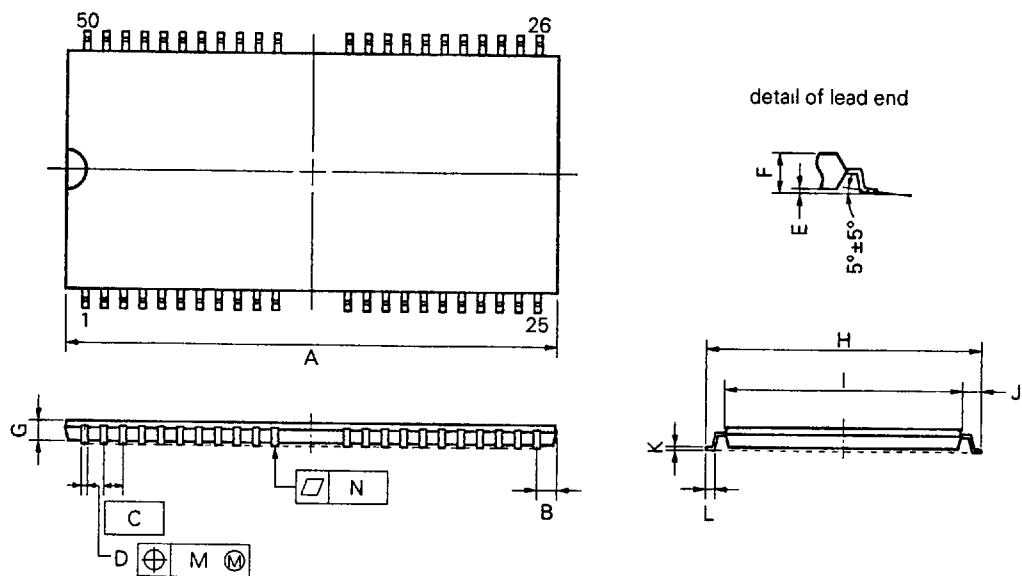


NOTE
Each lead centerline is located within 0.21 mm (0.009 inch) of its true position (T.P.) at maximum material condition.

S32G5-50-7KD1		
ITEM	MILLIMETERS	INCHES
A	21.17 MAX.	0.834 MAX.
B	1.06 MAX.	0.042 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	0.40±0.10	0.016 ^{+0.004} _{-0.005}
E	0.05±0.05	0.002±0.002
F	1.1 MAX.	0.044 MAX.
G	0.97	0.038
H	11.76±0.2	0.463±0.008
I	10.16±0.1	0.400±0.004
J	0.8±0.2	0.031 ^{+0.009} _{-0.008}
K	0.125 ^{+0.10} _{-0.05}	0.005 ^{+0.004} _{-0.002}
L	0.5±0.15	0.020 ^{+0.006} _{-0.007}
M	0.21	0.009
N	0.10	0.004

50 PIN PLASTIC TSOP (400mil)
44 Leads

NEC Cord:S50G5-80-7JF



NOTE

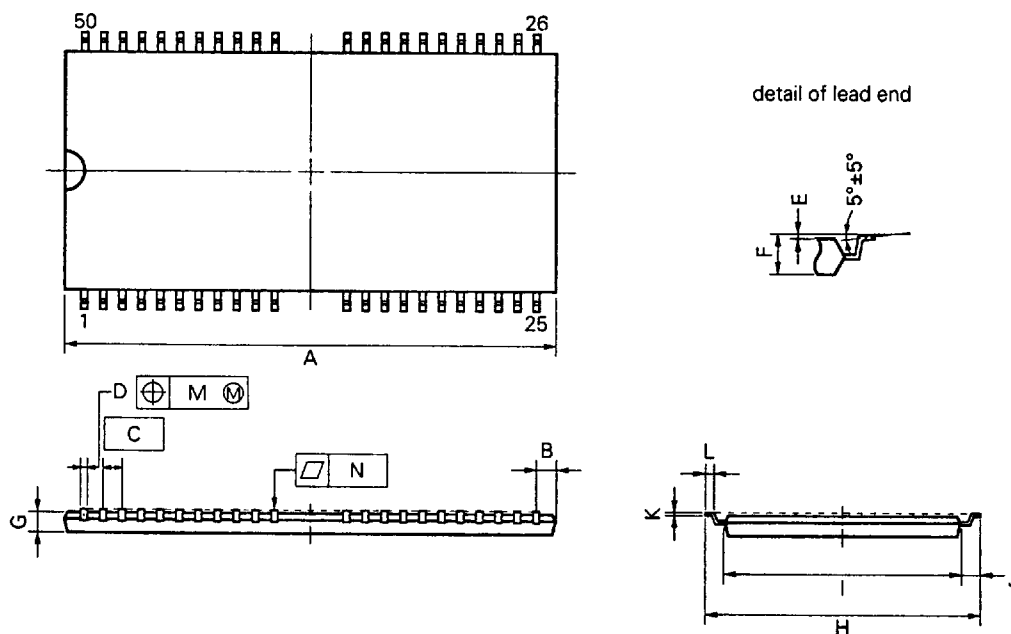
Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

S50G5-80-7JF

ITEM	MILLIMETERS	INCHES
A	21.45 MAX.	0.845 MAX.
B	1.13 MAX.	0.045 MAX.
C	0.8 (T.P.)	0.031 (T.P.)
D	0.30±0.10	0.012 ^{+0.004} _{-0.005}
E	0.05±0.05	0.002±0.002
F	1.1 MAX.	0.044 MAX.
G	0.97	0.038
H	11.76±0.2	0.463±0.008
I	10.16±0.1	0.400±0.004
J	0.8±0.2	0.031 ^{+0.009} _{-0.008}
K	0.125 ^{+0.10} _{-0.05}	0.005 ^{+0.004} _{-0.002}
L	0.5±0.15	0.020 ^{+0.006} _{-0.007}
M	0.13	0.005
N	0.10	0.004

50 PIN PLASTIC TSOP (400mil)
44 Leads Reverse bent

NEC Cord:S50G5-80-7KF



NOTE

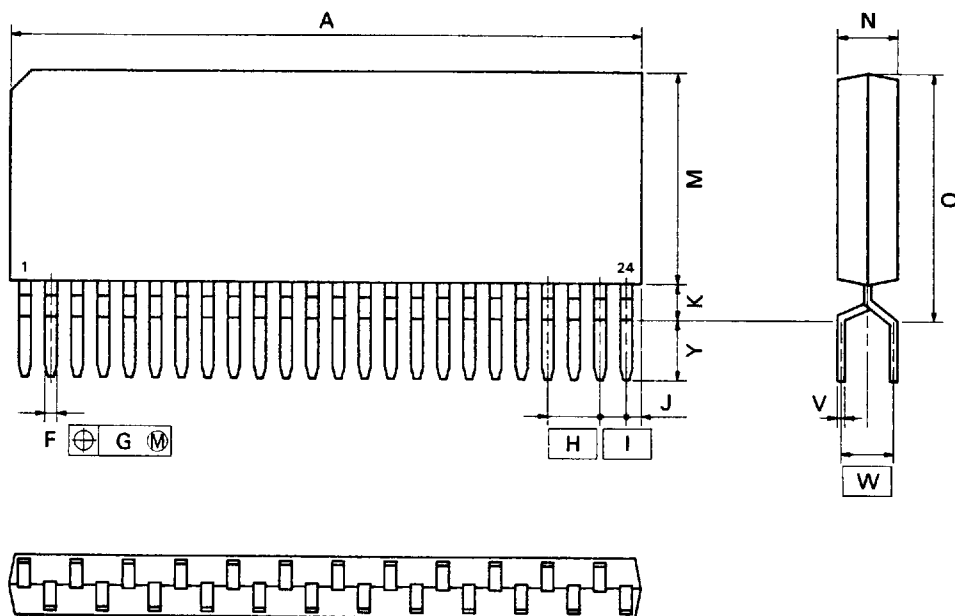
Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

S50G5-80-7KF

ITEM	MILLIMETERS	INCHES
A	21.45 MAX.	0.845 MAX.
B	1.13 MAX.	0.045 MAX.
C	0.8 (T.P.)	0.031 (T.P.)
D	0.30±0.10	0.012 ^{+0.004} _{-0.005}
E	0.05±0.05	0.002±0.002
F	1.1 MAX.	0.044 MAX.
G	0.97	0.038
H	11.76±0.2	0.463±0.008
I	10.16±0.1	0.400±0.004
J	0.8±0.2	0.031 ^{+0.009} _{-0.008}
K	0.125 ^{+0.10} _{-0.05}	0.005 ^{+0.004} _{-0.002}
L	0.5±0.15	0.020 ^{+0.006} _{-0.007}
M	0.13	0.005
N	0.10	0.004

24 PIN PLASTIC ZIP (475mil)

NEC Cord:P24V-100-475A



P24V-100-475A

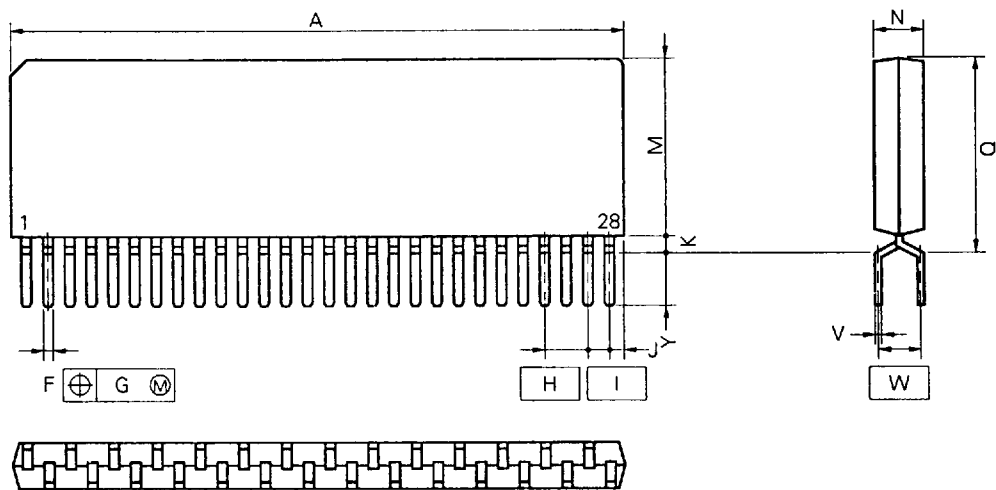
NOTE

Each lead centerline is located within 0.25 mm (0.010 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	31.75 MAX.	1.250 MAX.
F	0.50 ± 0.1	0.020 ± 0.004
G	$\phi 0.25$	$\phi 0.010$
H	2.54	0.100
I	1.27	0.050
J	1.27 MAX.	0.050 MAX.
K	1.0 MIN.	0.039 MIN.
M	10.8 MAX.	0.426 MAX.
N	2.8 ± 0.2	0.110 ± 0.008
Q	12.07 MAX.	0.476 MAX.
V	0.25 ± 0.10	0.010 ± 0.004
W	2.54	0.100
Y	3.3 ± 0.5	0.130 ± 0.02

28 PIN PLASTIC ZIP (475mil)

NEC Cord:P28VF-100-475A

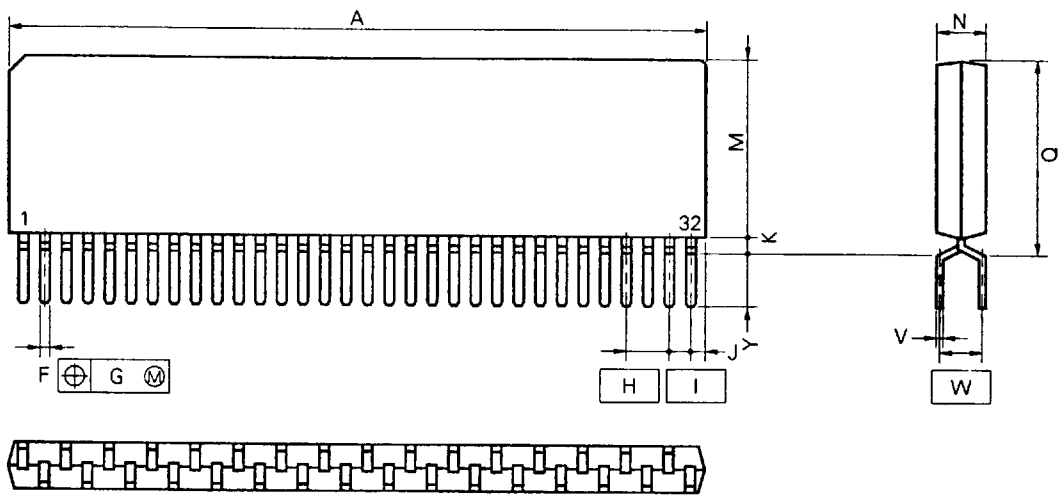


NOTE
Each lead centerline is located within 0.25 mm (0.010 inch) of its true position (T.P.) at maximum material condition.

P28VF-100-475A		
ITEM	MILLIMETERS	INCHES
A	36.83 MAX.	1.450 MAX.
F	0.5±0.10	0.020 ^{+0.004} _{-0.005}
G	0.25	0.010
H	2.54 (T.P.)	0.100 (T.P.)
I	1.27 (T.P.)	0.050 (T.P.)
J	1.27 MAX.	0.050 MAX.
K	0.9 MIN.	0.035 MIN.
M	10.8 MAX.	0.426 MAX.
N	2.8±0.2	0.110 ^{+0.009} _{-0.008}
Q	12.07 MAX.	0.475 MAX.
V	0.25 ^{+0.10} _{-0.05}	0.010 ^{+0.004} _{-0.003}
W	2.54 (T.P.)	0.100 (T.P.)
Y	3.25±0.2	0.128±0.008

32 PIN PLASTIC ZIP (475mil)

NEC Cord:P32VF-100-475A



NOTE
Each lead centerline is located within 0.25 mm (0.010 inch) of its true position (T.P.) at maximum material condition.

P32VF-100-475A		
ITEM	MILLIMETERS	INCHES
A	41.91 MAX.	1.650 MAX
F	0.5±0.10	0.020 ^{+0.004} _{-0.005}
G	0.25	0.010
H	2.54 (T.P.)	0.100 (T.P.)
I	1.27 (T.P.)	0.050 (T.P.)
J	1.27 MAX.	0.050 MAX.
K	0.9 MIN.	0.035 MIN.
M	10.8 MAX.	0.426 MAX.
N	2.8±0.2	0.110 ^{+0.009} _{-0.008}
Q	12.07 MAX.	0.475 MAX.
V	0.25 ^{+0.10} _{-0.05}	0.010 ^{+0.004} _{-0.003}
W	2.54 (T.P.)	0.100 (T.P.)
Y	3.25±0.2	0.128±0.008