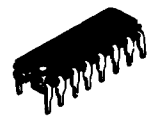
# HM50257 Series

**262144-word × 1-bit Dynamic Random Access Memory**

## ■ FEATURES

- Industry standard 16-pin DIP, 18-pin PLCC, 16-Pin ZIP
- Single 5V (±10%)
- On chip substrate bias generator
- Low Power: 350mW active, 20mW standby
- High speed: Access Time 120ns/150ns/200ns (max.)
- Common I/O capability using early write operation
- Nibble mode capability
- TTL compatible
- 256 refresh cycles . . . . . (4ms)
- 3 Variations of refresh; $\overline{RAS}$ only refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh

HM50257P Series



(DP-16B)

HM50257CP Series

(CP-18)

HM50257ZP Series

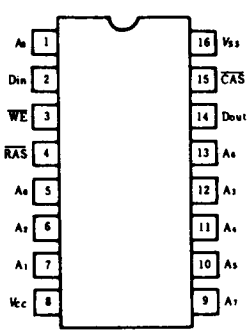
(ZP-16)

## ■ ORDERING INFORMATION

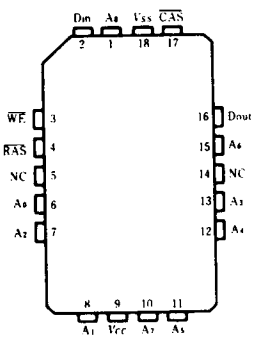
| Type No. | Access Time | Package |
|---|---|---|
| HM50257P-12 | 120ns | 300 mil 16 pin Plastic DIP |
| HM50257P-15 | 150ns | |
| HM50257P-20 | 200ns | |
| HM50257ZP-12 | 120ns | 16 pin Plastic ZIP |
| HM50257ZP-15 | 150ns | |
| HM50257ZP-20 | 200ns | |
| HM50257CP-12 | 120ns | 18 pin PLCC |
| HM50257CP-15 | 150ns | |
| HM50257CP-20 | 200ns | |

## ■ PIN ARRANGEMENT

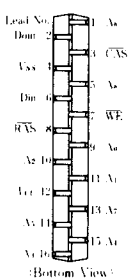
- HM50257P Series
- HM50257CP Series
- HM50257ZP Series




(Top View)

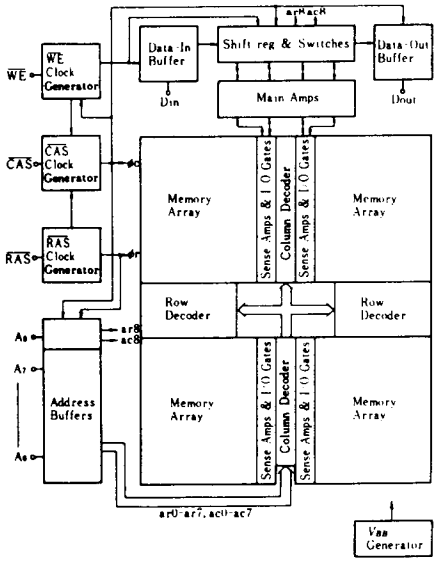



(Top View)




| | |
|---|---|
| $A_0 \sim A_8$ | Address Inputs |
| $\overline{CAS}$ | Column Address Strobe |
| Din | Data In |
| Dout | Data Out |
| $\overline{RAS}$ | Row Address Strobe |
| $\overline{WE}$ | Read/Write Input |
| $V_{CC}$ | Power (+5V) |
| $V_{SS}$ | Ground |
| $A_0 \sim A_7$ | Refresh Address Inputs |

## ■ BLOCK DIAGRAM




## ■ ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to $V_{SS}$ . . . . . -1V to +7V
Operating temperature, Ta (Ambient) . . . . . 0°C to +70°C
Storage temperature . . . . . -55°C to +125°C
Short circuit output current . . . . . 50mA
Power dissipation . . . . . 1W

## ■ RECOMMENDED DC OPERATING CONDITIONS ($Ta$ = 0 to +70°C)

| Parameter | Symbol | min | typ | max | Unit | Note |
|---|---|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 4.5 | 5.0 | 5.5 | V | 1 |
| Input High Voltage | $V_{IH}$ | 2.4 | — | 6.5 | V | 1 |
| Input Low Voltage | $V_{IL}$ | −1.0 | — | 0.8 | V | 1 |

Note 1) All voltages referenced to $V_{SS}$.

## ■ DC ELECTRICAL CHARACTERISTICS ($Ta$ = 0 to +70°C, $V_{CC}$ = 5V ± 10%, $V_{SS}$ = 0V)

| Parameter | Symbol | HM50257-12 | | HM50257-15 | | HM50257-20 | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | min | max | min | max | min | max | | |
| Operating Current ($\overline{RAS}$, $\overline{CAS}$ Cycling: $t_{RC}$ = min) | $I_{CC1}$ | — | 83 | — | 70 | — | 55 | mA | 1 |
| Stand by Current ($\overline{RAS}$ = $V_{IH}$, Dout = High Impedance) | $I_{CC2}$ | — | 4.5 | — | 4.5 | — | 4.5 | mA | |
| Refresh Current ($\overline{RAS}$ only Refresh, $t_{RC}$ = min) | $I_{CC3}$ | — | 62 | — | 53 | — | 42 | mA | |
| Standby Current ($\overline{RAS}$ = $V_{IH}$, Dout Enable) | $I_{CC5}$ | — | 10 | — | 10 | — | 10 | mA | 1 |
| Refresh Current ($\overline{CAS}$ before $\overline{RAS}$ Refresh, $t_{RC}$ = min) | $I_{CC6}$ | — | 69 | — | 58 | — | 45 | mA | |
| Nibble Mode Supply Current ($\overline{RAS}$ = $V_{IL}$, $\overline{CAS}$ Cycling, $t_{NC}$ = min) | $I_{CC8}$ | — | 57 | — | 48 | — | 37 | mA | |
| Input leakage (0 < $V_{IN}$ < 7V) | $I_{LI}$ | −10 | 10 | −10 | 10 | −10 | 10 | μA | |
| Output leakage (0 < $V_{out}$ < 7V, Dout = Disable) | $I_{LO}$ | −10 | 10 | −10 | 10 | −10 | 10 | μA | |
| Output levels High ($I_{out}$ = −5mA) | $V_{OH}$ | 2.4 | $V_{CC}$ | 2.4 | $V_{CC}$ | 2.4 | $V_{CC}$ | V | |
| Output levels Low ($I_{out}$ = 4.2mA) | $V_{OL}$ | 0 | 0.4 | 0 | 0.4 | 0 | 0.4 | V | |

Note) 1. $I_{CC}$ depends on output loading condition when the device is selected. $I_{CC}$ max. is specified at the output open condition.

## ■CAPACITANCE ($V_{CC}=5V\pm10\%$, $Ta=25°C$)

| Parameter | | Symbol | typ | max | Unit | Notes |
|---|---|---|---|---|---|---|
| Input Capacitance | Address, Data-In | $C_{I1}$ | — | 5 | pF | 1 |
| | Clocks | $C_{I2}$ | — | 7 | | 1, 2 |
| Output Capacitance | Data-Out | $C_O$ | — | 7 | | 1, 2 |

Notes) 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}=V_{IH}$ to disable Dout.

## ■ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

($Ta=0$ to $+70°C$, $V_{CC}=5V\pm10\%$, $V_{SS}=0V$) [10, 10, 11]

| Parameter | Symbol | HM50257-12 | | HM50257-15 | | HM50257-20 | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | min | max | min | max | min | max | | |
| Random Read or Write Cycle Time | $t_{RC}$ | 220 | — | 260 | — | 330 | — | ns | |
| Read-Write Cycle Time | $t_{RWC}$ | 265 | — | 310 | — | 390 | — | ns | |
| $\overline{RAS}$ to $\overline{CAS}$ Delay Time | $t_{RCD}$ | 25 | 60 | 25 | 75 | 30 | 100 | ns | 7 |
| Access Time from $\overline{RAS}$ | $t_{RAC}$ | — | 120 | — | 150 | — | 200 | ns | 2, 3 |
| Access Time from $\overline{CAS}$ | $t_{CAC}$ | — | 60 | — | 75 | — | 100 | ns | 3, 4 |
| Output Buffer Turn-off Delay | $t_{OFF}$ | — | 30 | — | 40 | — | 50 | ns | 5 |
| Transition Time (Rise and Fall) | $t_T$ | 3 | 50 | 3 | 50 | 3 | 50 | ns | 6 |
| $\overline{RAS}$ Precharge Time | $t_{RP}$ | 90 | — | 100 | — | 120 | — | ns | |
| $\overline{RAS}$ Pulse Width | $t_{RAS}$ | 120 | 10000 | 150 | 10000 | 200 | 10000 | ns | |
| $\overline{RAS}$ Hold Time | $t_{RSH}$ | 60 | — | 75 | — | 100 | — | ns | |
| $\overline{CAS}$ Hold Time | $t_{CSH}$ | 120 | — | 150 | — | 200 | — | ns | |
| $\overline{CAS}$ Pulse Width | $t_{CAS}$ | 60 | 10000 | 75 | 10000 | 100 | 10000 | ns | |
| $\overline{CAS}$ to $\overline{RAS}$ Precharge Time | $t_{CRP}$ | 10 | — | 10 | — | 10 | — | ns | |
| Row Address Set-up Time | $t_{ASR}$ | 0 | — | 0 | — | 0 | — | ns | |
| Row Address Hold Time | $t_{RAH}$ | 15 | — | 15 | — | 20 | — | ns | |
| Column Address Set-up Time | $t_{ASC}$ | 0 | — | 0 | — | 0 | — | ns | |
| Column Address Hold Time | $t_{CAH}$ | 20 | — | 25 | — | 30 | — | ns | |
| Column Address Hold Time referenced to $\overline{RAS}$ | $t_{AR}$ | 80 | — | 100 | — | 130 | — | ns | |
| Read Command Set-up Time | $t_{RCS}$ | 0 | — | 0 | — | 0 | — | ns | |
| Read Command Hold Time referenced to $\overline{CAS}$ | $t_{RCH}$ | 0 | — | 0 | — | 0 | — | ns | |
| Write Command Set-up Time | $t_{WCS}$ | 0 | — | 0 | — | 0 | — | ns | 8 |
| Write Command Hold Time | $t_{WCH}$ | 40 | — | 45 | — | 55 | — | ns | |
| Write Command Hold Time referenced to $\overline{RAS}$ | $t_{WCR}$ | 100 | — | 120 | — | 155 | — | ns | |
| Rrite Command Pulse Width | $t_{WP}$ | 40 | — | 45 | — | 55 | — | ns | |
| Write Command to $\overline{RAS}$ Lead Time | $t_{RWL}$ | 40 | — | 45 | — | 55 | — | ns | |
| Write Command to $\overline{CAS}$ Lead Time | $t_{CWL}$ | 40 | — | 45 | — | 55 | — | ns | |
| Data-in Set-up Time | $t_{DS}$ | 0 | — | 0 | — | 0 | — | ns | 9 |
| Data-in Hold Time | $t_{DH}$ | 40 | — | 45 | — | 55 | — | ns | 8, 9 |
| Data-in Hold Time referenced to $\overline{RAS}$ | $t_{DHR}$ | 100 | — | 120 | — | 155 | — | ns | |
| $\overline{RAS}$ to $\overline{WE}$ Delay | $t_{RWD}$ | 120 | — | 150 | — | 200 | — | ns | |
| $\overline{CAS}$ to $\overline{WE}$ Delay | $t_{CWD}$ | 60 | — | 75 | — | 100 | — | ns | 8 |
| Read Command Hold Time referenced to $\overline{RAS}$ | $t_{RRH}$ | 10 | — | 10 | — | 10 | — | ns | |
| Refresh Period | $t_{REF}$ | — | 4 | — | 4 | — | 4 | ms | |
| $\overline{CAS}$ Setup Time | $t_{CSR}$ | 10 | — | 10 | — | 10 | — | ns | |
| $\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh) | $t_{CHR}$ | 120 | — | 150 | — | 200 | — | ns | |
| $\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time | $t_{RPC}$ | 0 | — | 0 | — | 0 | — | ns | |
| Nibble Mode Access Time | $t_{NAC}$ | — | 25 | — | 25 | — | 35 | ns | |
| Nibble Mode $\overline{RAS}$ Cycle Time | $t_{NRC}$ | 390 | — | 460 | — | 590 | — | ns | |
| Nibble Mode $\overline{RAS}$ Pulse Width | $t_{NRA}$ | 290 | — | 350 | — | 460 | — | ns | |
| Nibble Mode Cycle Time | $t_{NC}$ | 55 | — | 60 | — | 80 | — | ns | |
| Nibble Mode $\overline{CAS}$ Precharge Time | $t_{NCP}$ | 20 | — | 25 | — | 35 | — | ns | |
| Nibble Mode $\overline{CAS}$ Pulse Width | $t_{NCA}$ | 25 | — | 25 | — | 35 | — | ns | |

(to be continued)

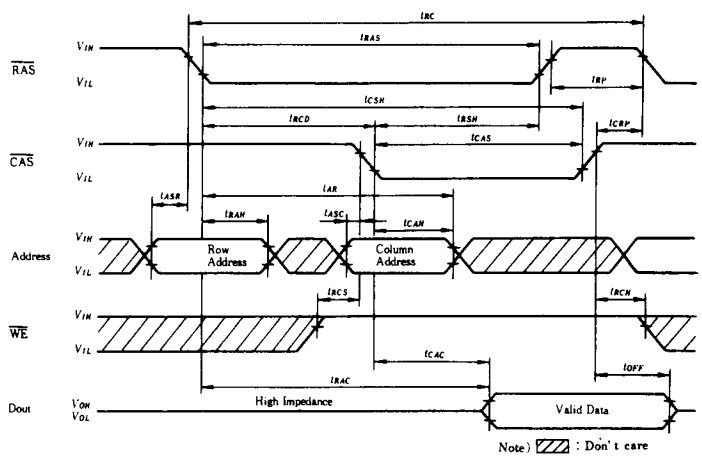
| Parameter | Symbol | HM50257-12 | | HM50257-15 | | HM50257-20 | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | min | max | min | max | min | max | | |
| Nibble Mode RAS Hold Time | $t_{RSH}$ | 40 | | 45 | | 55 | | ns | |
| Nibble Mode CAS to WE Delay | $t_{CWD}$ | 20 | | 25 | | 35 | | ns | |
| Nibble Mode Write Command to CAS Lead Time | $t_{CWL}$ | 20 | | 25 | | 35 | | ns | |
| Nibble Mode Write Command to RAS Lead Time | $t_{RWL}$ | 40 | | 45 | | 55 | | ns | |
| Nibble Mode Write Command Pulse Width | $t_{WP}$ | 20 | | 25 | | 35 | | ns | |
| Nibble Mode Read Write Cycle Time | $t_{RWC}$ | 75 | | 90 | | 120 | | ns | |
| Nibble Mode Read Write CAS Pulse Width | $t_{CRW}$ | 45 | | 55 | | 75 | | ns | |

**Notes**

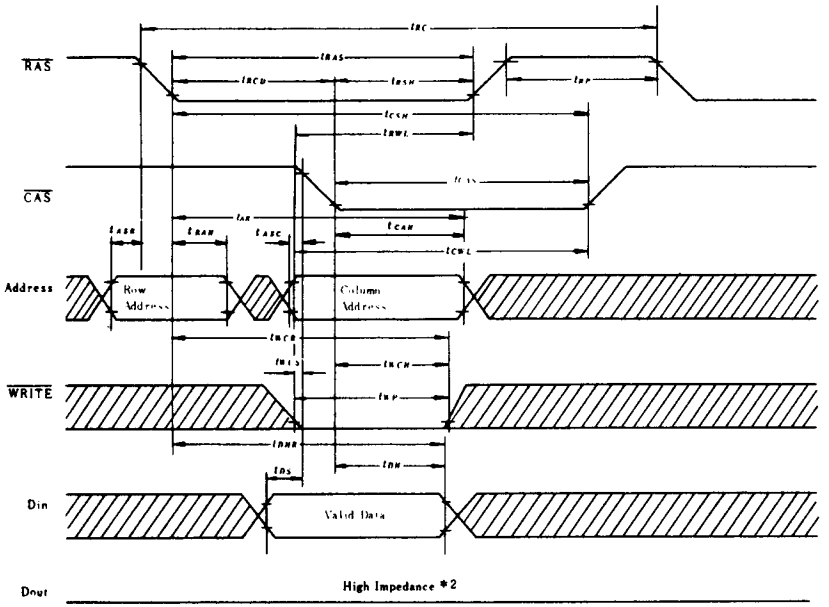
1. AC measurements assume $t_T$ = 5ns.
2. Assumes that $t_{RCD} \leqq t_{RCD}$ (max). If $t_{RCD}$ is greater than the maximum recommended value shown in this table, $t_{RAC}$ exceeds the value shown.
3. Measured with a load circuit equivalent to 2TTL loads and 100pF.
4. Assumes that $t_{RCD} \geqq t_{RCD}$ (max).
5. $t_{OFF}$ (max) defines the time at which the output achieves the open circuit condition and output voltage levels are not referred.
6. $V_{IH}$ (min) and $V_{IL}$ (max) are reference levels for measuring timing of input signals. Also, transition times are measured between $V_{IH}$ and $V_{IL}$.
7. Operation with the $t_{RCD}$ (max) limit insures that $t_{RAC}$ (max) can be met, $t_{RCD}$ (max) is specified as a reference point only; if $t_{RCD}$ is greater than the specified $t_{RCD}$ (max) limit, access time is controlled exclusively by $t_{CAC}$.
8. $t_{WCS}$, $t_{CWD}$ and $t_{RWD}$ are not restrictive operating parameters.
   They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geqq t_{WCS}$ (min), the cycle is an early write cycle and the data output pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geqq t_{CWD}$ (min) and $t_{RWD} \geqq t_{RWD}$ (min), the cycle is a read-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.
9. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.
10. An initial pause of 100μs is required after power-up then excute at least 8 initialization cycles.
11. At least, 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycle are required before using internal refresh counter.

## ■ TIMING WAVEFORMS

### ● READ CYCLE

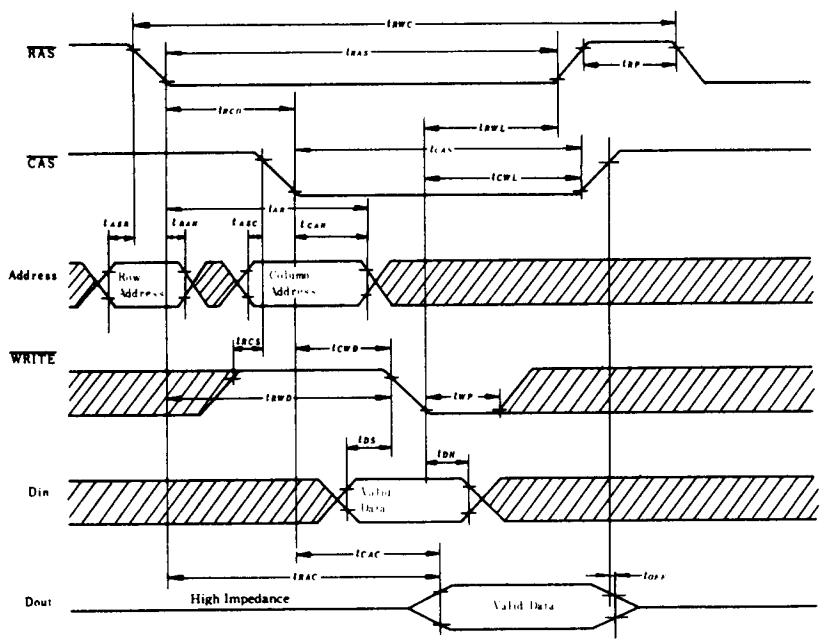


## ● WRITE CYCLE



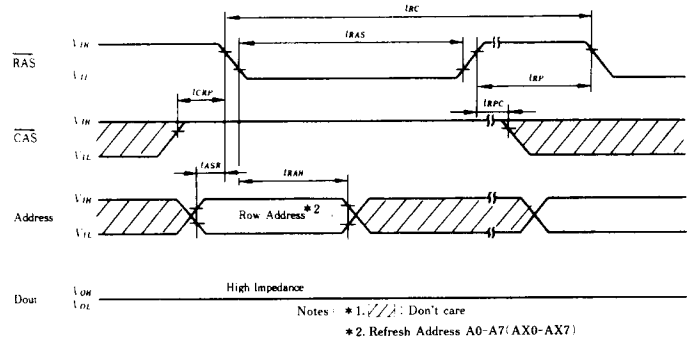

Notes) *1. ▨ : Don't care
*2. $t_{WCS} \geq t_{WCS}$ (min)

## ● READ MODIFY WRITE CYCLE




Notes) *1. ▨ : Don't care
*2. $t_{RWD} \geq t_{RWD}$ (min)
$t_{CWD} \geq t_{CWD}$ (min)

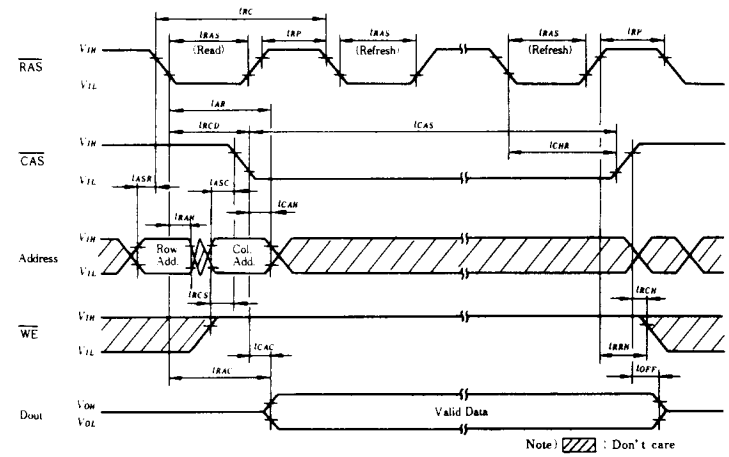
## ● $\overline{RAS}$ ONLY REFRESH CYCLE




Notes: *1. ▨ : Don't care

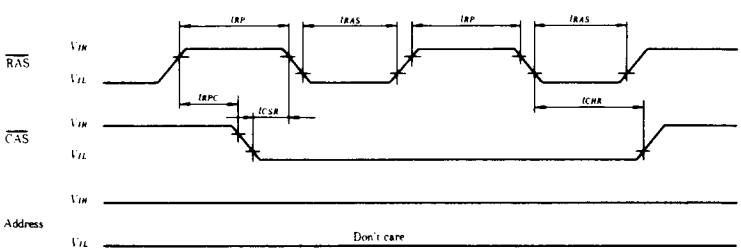
*2. Refresh Address A0-A7(AX0-AX7)

## ● HIDDEN REFRESH CYCLE

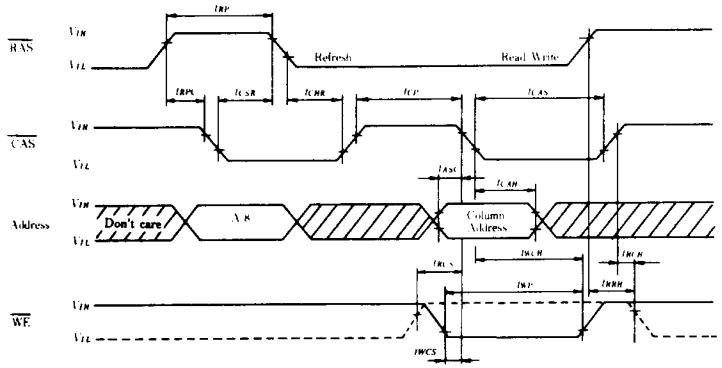



Note) ▨ : Don't care

## ● $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

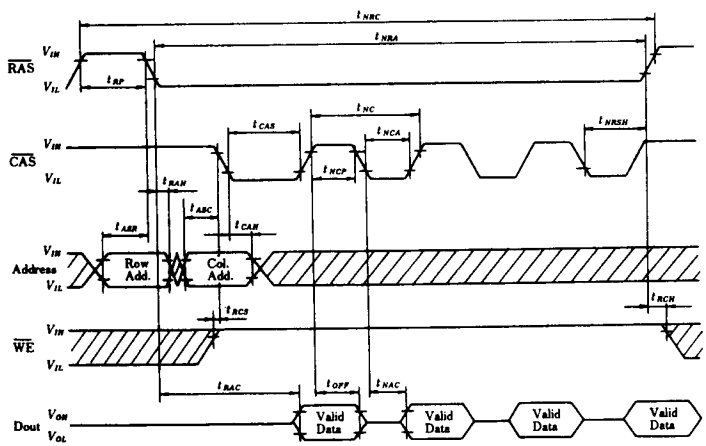


## ● COUNTER TEST




Notes) * 1. ▨ : Don't care
* 2. Dotted Line Means Read Cycle.

## ● NIBBLE MODE READ CYCLE




Note) ▨ : Don't care



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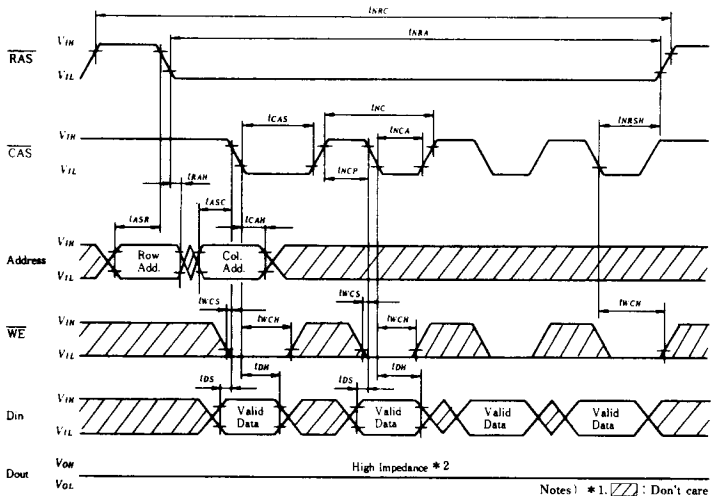
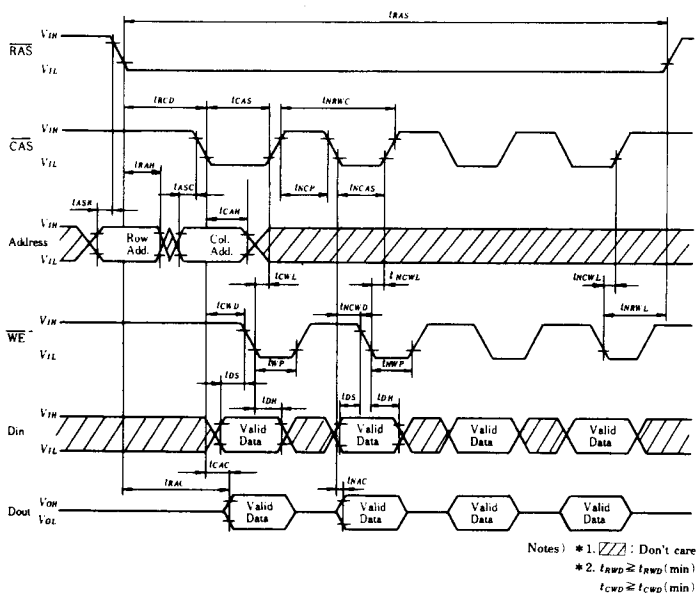
## ● NIBBLE MODE WRITE CYCLE




Notes) * 1. ▨ : Don't care
* 2. $t_{WCS} \geq t_{WCS}$ (min)

## ● NIBBLE MODE READ MODIFY WRITE CYCLE




Notes) * 1. ▨ : Don't care
* 2. $t_{RWD} \geq t_{RWD}$ (min)
$t_{CWD} \geq t_{CWD}$ (min)