

## YSS222

### KPB

#### Karaoke Processor B

#### ■ OUTLINE

YSS222(KPB) is an audio signal processing LSI for the key control function of one channel. The key of -1800 cent to +1200 cent can be managed in each 100 cent.

As A/D, D/A converter and RAM for the key control are built-in, it is the best for the voice key shift of the analog signal equipments such as the tape-recorder, the VTR, and microphones.

The amount of the key shift can be controlled even by the pulse input with the switch and the analog voltage input. Therefore, the microprocessor is unnecessary. It will be possible to develop and to make products in a shorter time at a lower cost.

#### ■ FEATURES

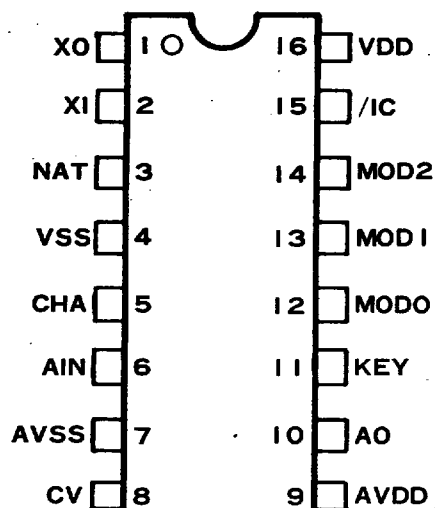
- Key control of -1800 cent to +1200 cent by 100 cent.
- 14-bit floating A/D and D/A converter are built-in to cope with analog signal.
- Sampling frequency of the internal signal processing is 16kHz.
- Sampling frequency of A/D and D/A converter is 32kHz.
- RAM for the key control processing is built-in.
- Three selective modes for specifying the amount of the key shift.
  1. Analog voltage mode: Specification by analog voltage.
  2. Switch pulse mode: Specification by pulse input from switch.
  3. Microprocessor pulse mode: Specification by pulse input from microprocessor.
- Master clock is 768kHz(48fs).
- 5V single power supply and Si-gate CMOS process.
- 16-pin DIP(YSS222-D) or 24-pin SOP(YSS222-M).

YAMAHA CORPORATION

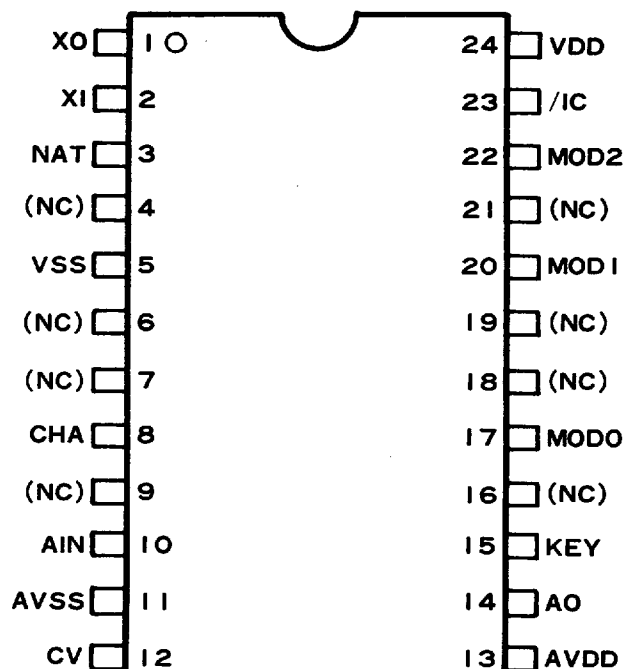
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| YSS222 CATALOG             |
| CATALOG No. : LSI-4SS222A2 |
| 1996. 5                    |

## PIN CONFIGURATION



<16DIP Top View>



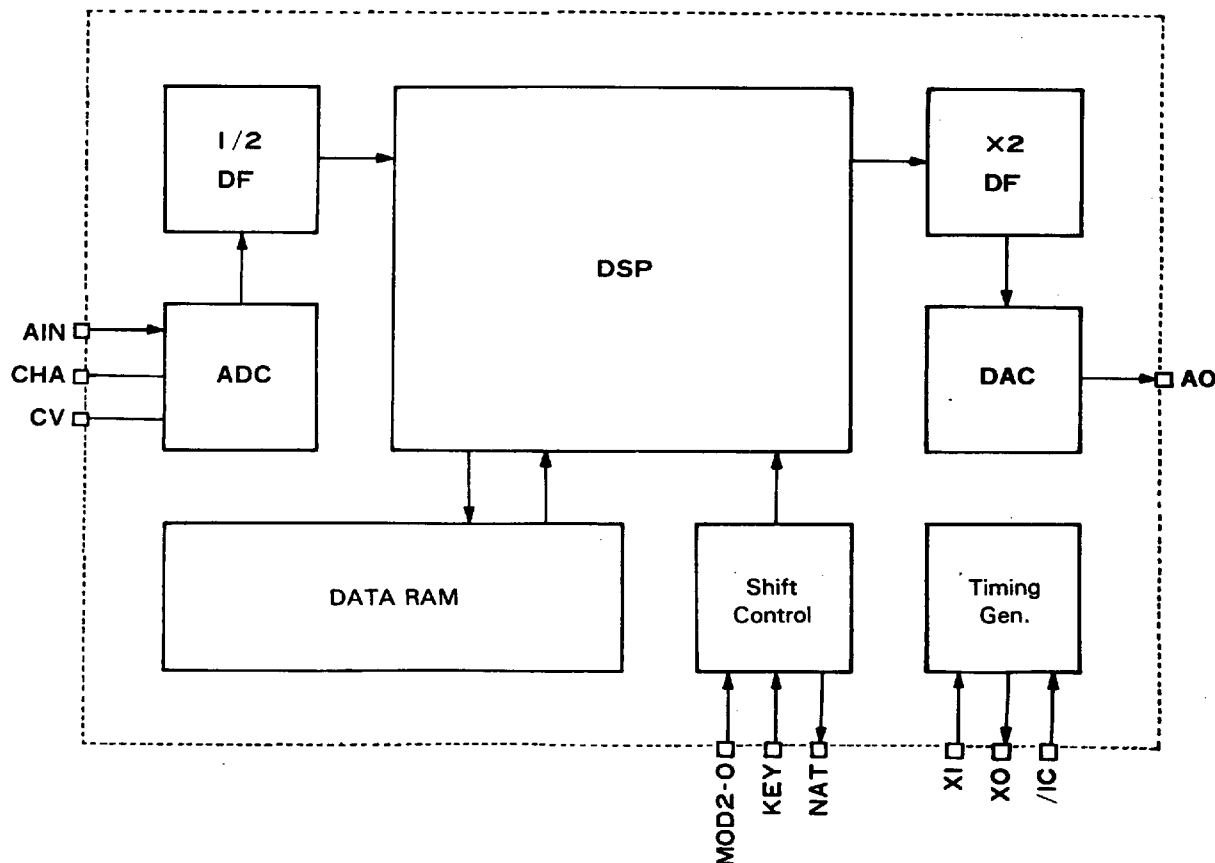
<24SOP Top View>

## PIN DESCRIPTION

| No. |     | Name | I/O | Function                                                        |
|-----|-----|------|-----|-----------------------------------------------------------------|
| 16D | 24S |      |     |                                                                 |
| 1   | 1   | XO   | O   | Oscillator Connection Terminal                                  |
| 2   | 2   | XI   | I   | Oscillator Connecting Terminal or External Clock Input (768kHz) |
| 3   | 3   | NAT  | O   | Key Shift Status Output ('H'=Non-Shift state)                   |
| 4   | 5   | VSS  | —   | Ground (Digital Block)                                          |
| 5   | 8   | CHA  | —A  | Sample/Hold Capacitor Connecting Terminal for AIN signal        |
| 6   | 10  | AIN  | IA  | Analog Audio Signal ADC Input                                   |
| 7   | 11  | AVSS | —A  | Ground (Analog Block)                                           |
| 8   | 12  | CV   | —A  | Center Voltage terminal of Internal ADC                         |
| 9   | 13  | AVDD | —A  | +5V Power Supply (Analog Block)                                 |
| 10  | 14  | AO   | OA  | Analog Audio Signal DAC Output                                  |
| 11  | 15  | KEY  | IA  | Key Shift Control Input                                         |
| 12  | 17  | MOD0 | I   | Control Mode Select 0                                           |
| 13  | 20  | MOD1 | I   | Control Mode Select 1                                           |
| 14  | 22  | MOD2 | I   | Control Mode Select 2                                           |
| 15  | 23  | /IC  | Is  | Initial Clear Input                                             |
| 16  | 24  | VDD  | —   | +5V Power Supply (Digital Block)                                |

(Note) Is; Schmitt-Trigger Input Terminal, A; Analog Terminal

## ■ BLOCK DIAGRAM



## ■ FUNCTION DESCRIPTION

### 1. Clocks      XI, XO

Using XI and XO terminals, the oscillation circuit is composed.

The oscillation frequency is 768kHz(48fs).

It is also possible to input an external clock to the XI terminal.

### 2. Audio Signal I/O      AIN, CHA, CV, AO

An analog audio signal is input from AIN terminal. The signal is A/D converted at 32kHz, is decimated to 16kHz with 1/2 under sampling filter, and is digital-processed.

Connect to CHA terminal the sample/hold capacitor for A/D conversion of AIN signal.

CV terminal indicates a center voltage of internal ADC. With a stabilization capacitor connected, bias the AIN signal by this voltage.

After digital key shift processing, audio signal is over-sampled to 32kHz with 2 times over-sampling filter and after D/A conversion, it is output from AO terminal.

With a sample/hold capacitor connected to AO terminal, execute the signal by the buffer with a high impedance input.

### 3. Key control KEY, MOD2-0, NAT

The method of specifying the amount of the key shift is selected with MOD2-MOD0 terminals. The KEY terminal is an input terminal to control the amount of the key shift. However, the input method is different depending on the specified mode.

The NAT terminal becomes 'H' when key is 'Non-shift' (It is displayed in every mode description as <NAT>).

When the key has changed, (All modes contain  $\pm 0.0$  cent), NAT the terminal becomes 'L'.

| MOD2 | MOD1 | MOD0 | Mode                      | Key Shift Range [cent]      |
|------|------|------|---------------------------|-----------------------------|
| H    | H    | H    | Microprocessor Pulse Mode | -1800 ~ +1200 (by 100 cent) |
| H    | H    | L    | Switch Pulse Mode 1       | -1200 ~ +1200 (by 100 cent) |
| H    | L    | H    | Switch Pulse Mode 2       | -600 ~ +600 (by 100 cent)   |
| H    | L    | L    | Switch Pulse Mode 3       | -400 ~ +400 (by 100 cent)   |
| L    | H    | H    | Analog Voltage Mode 1     | -1800 ~ +1200 (by 100 cent) |
| L    | H    | L    | Analog Voltage Mode 2     | -1600 ~ +1200 (by 200 cent) |

#### (1) Analog voltage mode

The KEY terminal voltage is divided into 32 levels between VDD-VSS, and keys are provided according to the KEY terminal voltage.

As for the analog voltage mode, there are two kinds and the shift resolution is different.

| KEY Terminal Voltage [V] |             | Key Shift [cent] |         | KEY Terminal Voltage [V] |             | Key Shift [cent] |        |
|--------------------------|-------------|------------------|---------|--------------------------|-------------|------------------|--------|
| * VDD                    | VDD=5.0     | Mode 1           | Mode 2  | * VDD                    | VDD=5.0     | Mode 1           | Mode 2 |
| 32 ~ 31/32               | 5.00 ~ 4.84 | +1200            | +1200   | 16 ~ 15/32               | 2.50 ~ 2.34 | -400             | -400   |
| 31 ~ 30/32               | 4.84 ~ 4.69 | +1100            |         | 15 ~ 14/32               | 2.34 ~ 2.19 | -500             |        |
| 30 ~ 29/32               | 4.69 ~ 4.53 | +1000            | +1000   | 14 ~ 13/32               | 2.19 ~ 2.03 | -600             | -600   |
| 29 ~ 28/32               | 4.53 ~ 4.38 | +900             |         | 13 ~ 12/32               | 2.03 ~ 1.88 | -700             |        |
| 28 ~ 27/32               | 4.38 ~ 4.22 | +800             | +800    | 12 ~ 11/32               | 1.88 ~ 1.72 | -800             | -800   |
| 27 ~ 26/32               | 4.22 ~ 4.06 | +700             |         | 11 ~ 10/32               | 1.72 ~ 1.56 | -900             |        |
| 26 ~ 25/32               | 4.06 ~ 3.91 | +600             | +600    | 10 ~ 9/32                | 1.56 ~ 1.41 | -1000            | -1000  |
| 25 ~ 24/32               | 3.91 ~ 3.75 | +500             |         | 9 ~ 8/32                 | 1.41 ~ 1.25 | -1100            |        |
| 24 ~ 23/32               | 3.75 ~ 3.59 | +400             | +400    | 8 ~ 7/32                 | 1.25 ~ 1.09 | -1200            | -1200  |
| 23 ~ 22/32               | 3.59 ~ 3.44 | +300             |         | 7 ~ 6/32                 | 1.09 ~ 0.94 | -1300            |        |
| 22 ~ 21/32               | 3.44 ~ 3.28 | +200             | +200    | 6 ~ 5/32                 | 0.94 ~ 0.78 | -1400            | -1400  |
| 21 ~ 20/32               | 3.28 ~ 3.13 | +100             |         | 5 ~ 4/32                 | 0.78 ~ 0.63 | -1500            |        |
| 20 ~ 19/32               | 3.13 ~ 2.97 | $\pm 0$          | $\pm 0$ | 4 ~ 3/32                 | 0.63 ~ 0.47 | -1600            | -1600  |
| 19 ~ 18/32               | 2.97 ~ 2.81 | -100             |         | 3 ~ 2/32                 | 0.47 ~ 0.31 | -1700            |        |
| 18 ~ 17/32               | 2.81 ~ 2.66 | -200             | -200    | 2 ~ 1/32                 | 0.31 ~ 0.16 | -1800            | <NAT>  |
| 17 ~ 16/32               | 2.66 ~ 2.50 | -300             |         | 1 ~ 0/32                 | 0.16 ~ 0.00 | <NAT>            |        |

(Note) <NAT>: The key becomes non-shift.

## (2) Switch pulse mode

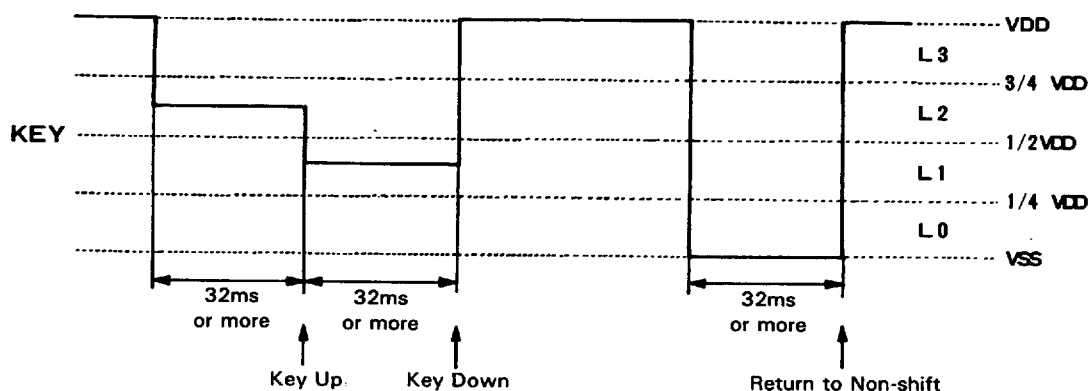
The key changes 100 cent by every pulse to KEY terminal according to the voltage level of the pulse.

The width of the pulse is required to be 32ms or more, and the pulse shorter than 32ms is disregarded.

As for the switch pulse mode, there are three kinds and the variable range of the key is different. The pulse which specifies more than the maximum variable range is disregarded.

| KEY Terminal Voltage [V]        | Operation                 | Maximum Variable Range |        |        |
|---------------------------------|---------------------------|------------------------|--------|--------|
|                                 |                           | Mode 1                 | Mode 2 | Mode 3 |
| L3= VDD ( VDD ~ 3/4 VDD)        | No Change                 |                        |        |        |
| L2= 5/8 VDD (3/4 VDD ~ 2/4 VDD) | Key Shift Up (100 cent)   | +6                     | +3     | +2     |
| L1= 3/8 VDD (2/4 VDD ~ 1/4 VDD) | Key Shift Down (100 cent) | -6                     | -      | -2     |
| L0= VSS (1/4 VDD ~ VSS)         | Return to Non-shift <NAT> |                        |        |        |

## [Example]



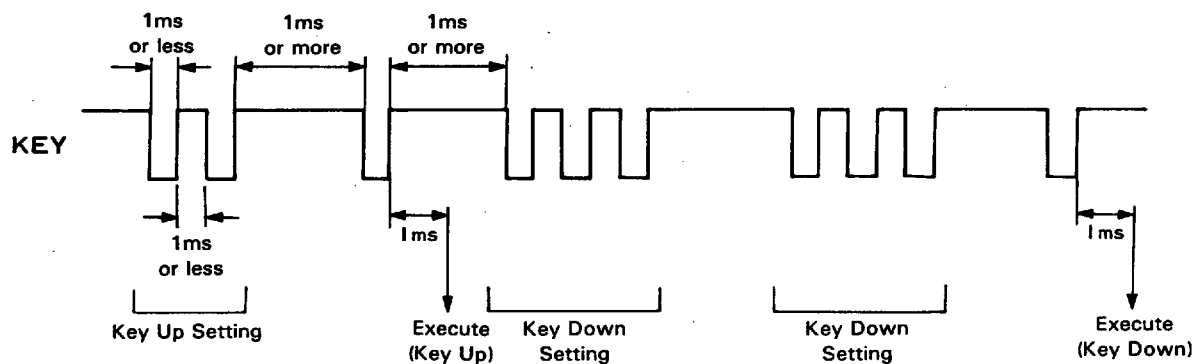
## (3) Microprocessor pulse mode

The amount of the key shift is specified according to the number of the pulse input to KEY terminal.

Each code is identified by the number of the pulse inputs at intervals of 1ms or less, and the delimitation between codes by a pulse interval of 1ms or more. Set the width of the pulse as 1ms or less.

In this mode, unless 'one pulse' code is input to KEY terminal, actual key shift will not be executed.

| Pulse Code  | Operation                      |
|-------------|--------------------------------|
| One Pulse   | Execute                        |
| Two Pulse   | Setting of Key Up (100 cent)   |
| Three Pulse | Setting of Key Down (100 cent) |
| Four Pulse  | Setting of Non shift <NAT>     |

**[Example]****4. Reset /IC**

It is necessary to reset this LSI when the power is turned on.

## ■ ELECTRICAL CHARACTERISTICS

### 1. Absolute Maximum Ratings

| Parameter             | Symbol | Rating         | Unit |
|-----------------------|--------|----------------|------|
| Power Supply Voltage  | VDD    | -0.5 ~ 7.0     | V    |
| Input Voltage         | VI     | -0.5 ~ VDD+0.5 | V    |
| Output Current        | IO     | -20 ~ 20       | mA   |
| Operating Temperature | Top    | 0 ~ 70         | °C   |
| Storage Temperature   | Tstg   | -50 ~ 125      | °C   |

### 2. Recommended Operating Conditions

| Parameter             | Symbol | Min. | Typ. | Max. | Unit |
|-----------------------|--------|------|------|------|------|
| Power Supply Voltage  | VDD    | 4.5  | 5.0  | 5.5  | V    |
| Operating Temperature | Top    | 0    | 25   | 70   | °C   |

### 3. DC Characteristics

| Parameter              | Symbol | Condition      | Min.    | Typ. | Max.   | Unit |
|------------------------|--------|----------------|---------|------|--------|------|
| Power Supply Current   | IDD    | VDD=5.0V       |         | 9    |        | mA   |
| Input Voltage H Level  | VIL    | *1             |         |      | 0.3VDD | V    |
| Input Voltage L Level  | VIH    | *1             | 0.7VDD  |      |        | V    |
| Input Leakage Current  | ILI    | *2             |         |      | 10     | μA   |
| Input Capacitance      | CI     | *1             |         |      | 8      | pF   |
| Output Voltage L Level | VOL    | IOL=1.6mA, *3  |         |      | 0.4    | V    |
| Output Voltage H Level | VOH    | IOH=-0.4mA, *3 | VDD-0.4 |      |        | V    |
| Output Capacitance     | CO     | *3             |         |      | 10     | pF   |

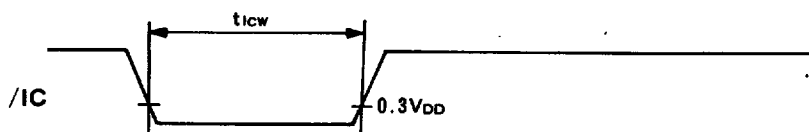
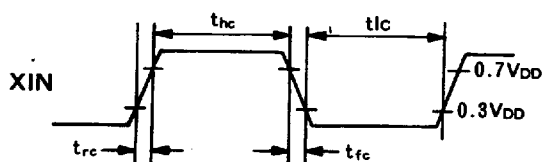
\*1) Applicable to XI, MOD0, MOD1, MOD2, /IC terminals.

\*2) Applicable to input terminals except analog terminals and pulled up terminals.

\*3) Applicable to all output terminals except analog terminals.

## 4. AC Characteristics

| Parameter           | Symbol           | Min. | Typ. | Max. | Unit |
|---------------------|------------------|------|------|------|------|
| XIN Clock Frequency | fc               | 690  | 768  | 845  | kHz  |
| H Level Time        | t <sub>hc</sub>  | 390  |      |      | ns   |
| L Level Time        | t <sub>lc</sub>  | 390  |      |      | ns   |
| Rise Time           | t <sub>rc</sub>  |      | 50   | 200  | ns   |
| Fall Time           | t <sub>fc</sub>  |      | 50   | 200  | ns   |
| /IC Pulse Width     | t <sub>icw</sub> | 13   |      |      | μs   |

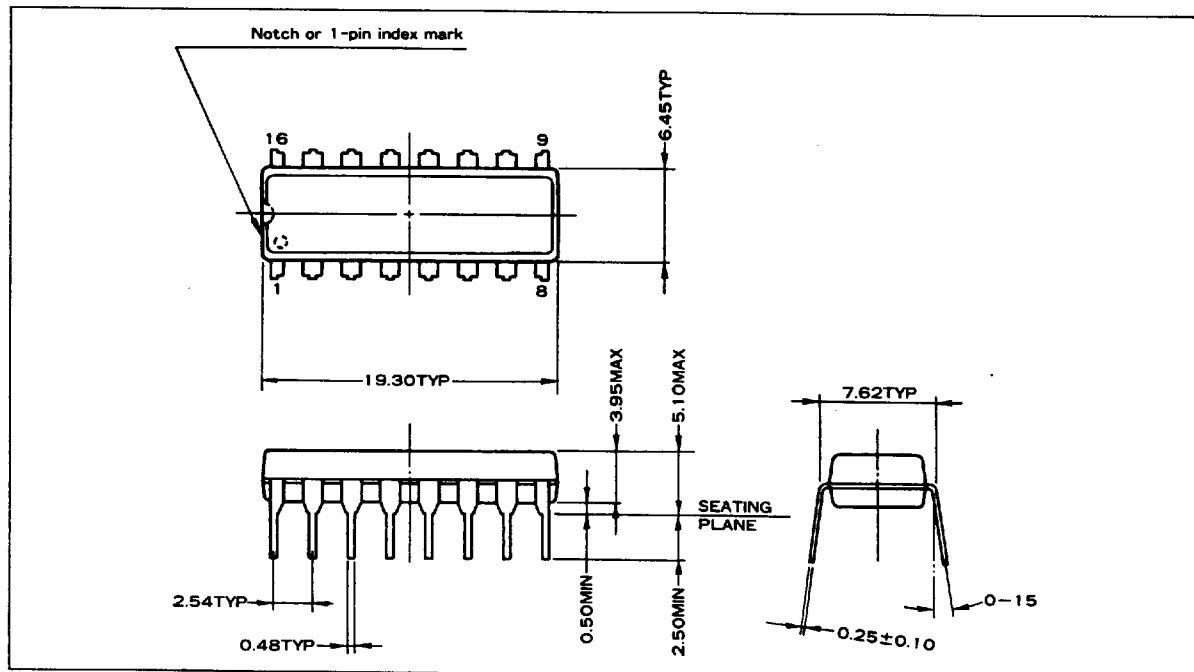
5. Analog Characteristics ( $V_{DD}=5.0V$ ,  $T_{op}=25^{\circ}C$ )

| Parameter                 | Symbol | Condition                        | Min.         | Typ.        | Max.         | Unit |
|---------------------------|--------|----------------------------------|--------------|-------------|--------------|------|
| Analog Input Voltage (1)  | VIA1   | AIN Terminal                     | $0.05V_{DD}$ |             | $0.95V_{DD}$ | V    |
| Analog Input Voltage (2)  | VIA2   | KEY Terminal                     | 0            |             | $V_{DD}$     | V    |
| Analog Output Voltage     | VOA    | AO Terminal                      | $0.02V_{DD}$ |             | $0.98V_{DD}$ | V    |
| CV Center Voltage         | VC     | CV Terminal                      |              | $0.5V_{DD}$ |              | V    |
| Total Harmonic Distortion | THD+N  | 1kHz, 0dB, *1<br>1kHz, -30dB, *1 |              |             | 1.0<br>1.5   | %    |
| Signal to Noise Ratio     | S/N    | S=0dB, *1                        | 75           | 80          |              | dB   |

\*1) 0dB=4.5V<sub>pp</sub>, A/D → D/A through

## ■ EXTERNAL DIMENSIONS

### ● YSS222-D



### ● YSS222-M

