TOSHIBA BI-CMOS INTEGRATED CIRCUIT SILICON MONOLITHIC

TB62600FG

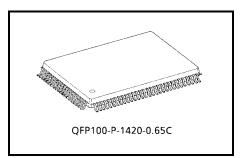
64BIT SHIFT REGISTER / LATCH DRIVER

The TB62600FG is specifically designed for 64bit Thermal Head drivers. And this IC is monolithic integrated circuits designed to be used together with Bi–CMOS (DMOS) integrated circuit. The devices consist of a 64bit shift register, dual 64bit latches, and 64 output DMOS structures.

The suffix (G) appended to the part number represents a Lead(Pb)-Free product.

FEATURE

- Built-in selection circuit : parallel-in parallel-out (8 × 8) or serial-in parallel-out (1 × 64)
- CMOS compatible inputs
- Open-drain DMOS outputs
- Low steady-state power consumption
- Built-in mono stable multi-viblator for head protection
- Package : QFP100-P-1420C

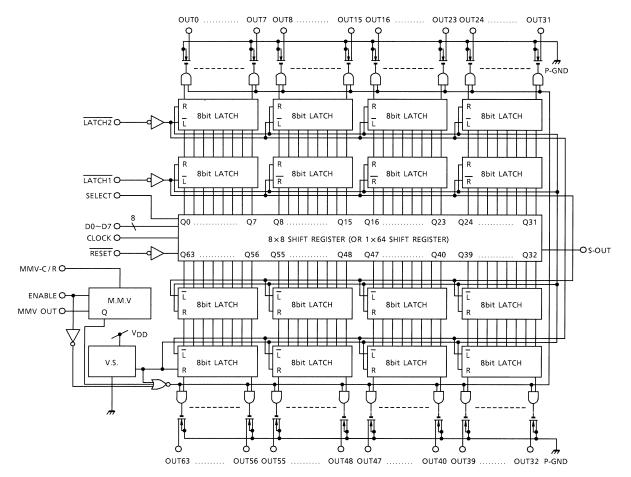


Weight: 1.6 g (typ.)

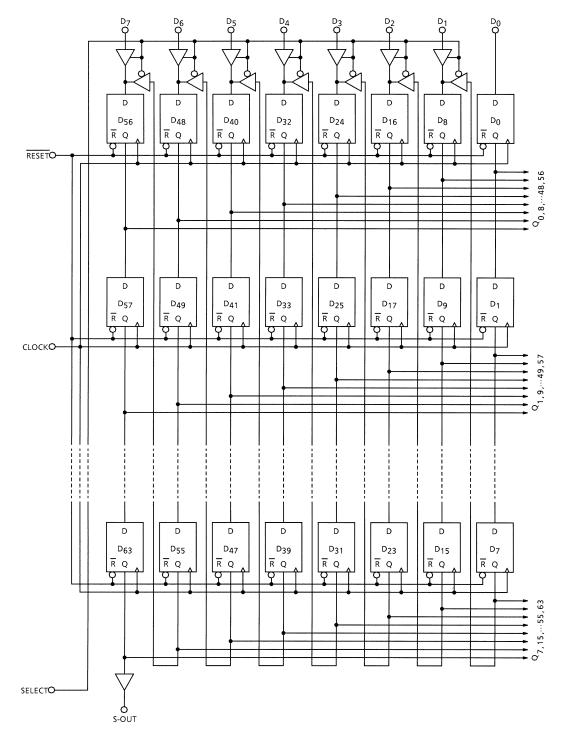
PIN CONNECTION (TOP VIEW)

	VDD	L-GND	RESET	CLOCK	S-OUT	D7	D6	D5	D4	D3	D2	D1	DO	NC	LATCH1	LATCH2	ENABLE	SELECT	L-GND	DD VDD	
1	100		98	97	96	95	94	93	92	91	90	89	88	87	86	85	84	83		81	1
NC [33	90	5/	90	35	54	33	92	51	90	09	00	07	80	05	04	05	02] NC
NC [2		\sim																	79] мму-оцт
NC [3	()																78] MMV-C/R
P-GND	4		\sim																	77	P-GND
	5																			76	
	6																			75] <u>outi</u>
OUT61	7																			74] <u>OUT2</u>
	8																			73] outs
	9																			72] OUT4
	10																			71] <u>outs</u>
OUT57	11																			70] <u>out</u> 6
	12																			69	
P-GND	13																			68	P-GND
ουτ55	14																			67	
OUT54	15																			66	
OUT53	16																			65	
OUT52	17																			64	
OUT51	18																			63	0UT12
OUT50 [19																			62] OUT13
OUT49 [20																			61	0UT14
OUT48	21																			60	0UT15
P-GND	22																			59	P-GND
OUT47	23																			58	0UT16
OUT46	24																			57	0UT17
OUT45	25																			56] OUT18
OUT44	26																			55] OUT19
OUT43	27																			54	0UT20
OUT42	28																			53	0UT21
OUT41	29																			52	0UT22
OUT40	30																				0UT23
	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	J
	P-GND	OUT39	0UT38	0UT37	0UT36	0UT35	0UT34	0UT33	0UT32	P-GND	P-GND	OUT31	0UT30	0UT29	0UT28	0UT27	0UT26	0UT25	0UT24	P-GND	
	4	10	10	19	19	19	19	Ы	19	Ę	Ę	10	19	19	10	19	19	19	19	đ	1

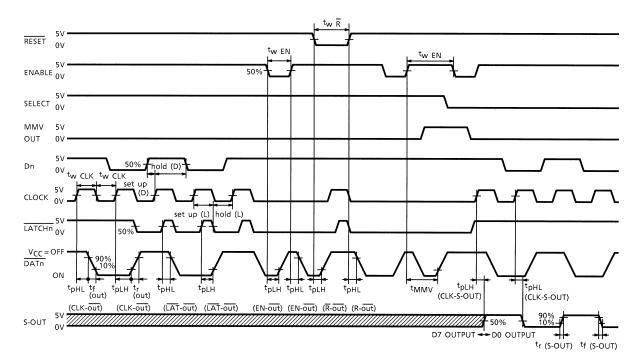
BLOCK DIAGRAM



BLOCK DIAGRAM (8 × 8, 1 × 64 shift register)



TIMING WAVEFORM



TERMINAL DESCRIPTION

PIN NAME	PIN No.	FUNCTION
CLOCK	97	Input Terminals for Shift register Clock.
ENABLE	84	"L" : All Outputs "On". Pull-Down Input Terminal.
RESET	98	"L" : Reset shift register and latch. Pull-Down Input Terminal.
D0~D7	88~95	Input Terminals for Output Data. "H" : Output On, "L" : Output Off.
MMV-C/R	78	CR Connection Terminal for CR Timer (MMV)
MMV-OUT	79	Output Terminal for CR Timer (MMV)
OUT0 ~ 63	_	Output Terminals. These are Open Drain Outputs.
SELECT	83	Input Terminal for Input Mode Data. "H" : 8bit Parallel Input Mode, "L" : 1bit Serial Input Mode.
S-OUT	96	Output Terminal for Serial Data "D63".
LATCH1 / LATCH2	86 / 85	Input Terminal for Latch. "H" : Data Throught, "L" : Data Latch.
V _{DD}	81, 100	Supply Voltage Terminal for Control Logic.
L-GND	82, 99	Ground Terminal for Control Logic
P-GND	_	Ground Terminal for Drivers. 10 Terminals.

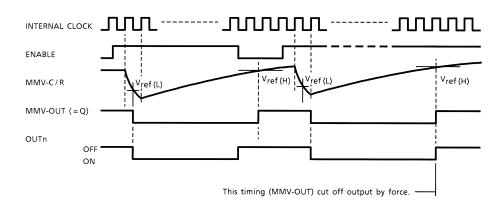
MMV OPERATION

MMV Output of Q becomes "L" when the MMV / E voltage becomes less than V_{ref} (L) after the first rising edge of Internal Clock.

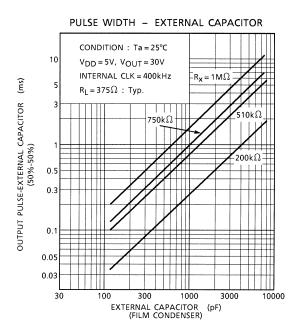
And becomes "H" when the MMV / E voltage above V_{ref} (H) after re-changing of external capacitance connect to MMV / E. The external capacitance and resistor connect to MMV / E control MMV Output "ON" period. So Output Load is protected from burn-out. It's required enough discharging time (decided by Time period of

Internal Clock) of external capacitance.

(Refer to figure below)



 PULSE WIDTH OF MMV See Below



ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

CHARACT	ERISTIC	SYMBOL	RATING	UNIT		
Supply Voltage	ly Voltage		ply Voltage		-0.3~7.0	V
Output Drain-Sourc	e Voltage	V _{DS}	-0.4~30	V		
Output Current		I _{DS}	130	mA / ch		
Input Current		I _{IN}	±5	mA		
Input Voltage		V _{IN}	-0.3~V _{DD} ± 0.3	V		
Power Dissipation	Free Air	PD	1.0	w		
	(Note 1) PCB	FD	1.3	vv		
Operating Temperat	ure	T _{opr}	-40~85	°C		
Storage Temperatur	e	T _{stg}	-55~150	°C		

Note 1: 60 × 60 × 1.6 mm Cu 24% Glass Epoxy PCB

RECOMMENDED OPERATING CONDITIONS (Ta = $-40 \sim 85^{\circ}$ C, V_{SS} = 0 V)

CHARACTERISTIC		SYMBOL	CON	MIN	TYP.	MAX	UNIT		
Supply Voltage	V _{DD}			_			5.5	V	
Input Voltage	"H" LEVEL	V _{IH}	_		0.7 V _{DD}	-	V _{DD}	v	
	"L" LEVEL	VIL		0	-	0.3 V _{DD}			
Output Drain-So	Output Drain-Source Voltage			-	_	24	V		
			Duty = 100%		_	_	44		
Output Current	upply Voltage upply Voltage upput Voltage "H" LEVEL "L" LEVEL utput Drain–Source Voltage utput Current xternal Resistor xternal Capacitance	ent		Duty = 80%	All Output "L" Level	_	_	49	mA / ch
			Duty = 50%		_	_	62		
External Resistor		R _{EXT}		200	_	1000	kΩ		
External Capacitance		C _{EXT}		100	_	4000	pF		
Power Dissipation	ı	PD		_	_	_	0.67	mW	

ELECTRICAL CHARACTERISTICS (Ta = $-10 \sim 80^{\circ}$ C, V_{DD} = 4.5 \sim 5.5 V, V_{SS} = 0 V, "H" = V_{IH}, "L" =V_{IL})

CHARACTERISTIC		SYMBOL	TEST CIR- CUIT	TEST C	ONDITION	MIN	TYP.	MAX	UNIT
		V _{DS1} — I _{OUT} = 40 mA, Ta = 25°C		_	0.16	0.32			
Output Voltage	"L" Level	V _{DS1}	_	I _{OUT} = 40 mA	_	_	0.48	V	
	L Level	V _{DS2}	_	I _{OUT} = 100 mA	∖, Ta = 25°C	_	0.40	0.80	V
		V _{DS2}	_	I _{OUT} = 100 mA	١	_	_	1.20	
Output Current	"H" Level	I _{OH}	_	S-OUT	V _{OH} = 4.6 V Ta =25°C	_	0.2	0.5	
	"L" Level	I _{OL}	_	MMV-OUT	V _{OH} = 0.4 V Ta=25°C	_	0.2	0.5	mA
Output Resistor	Output Resistor		_	Ta = 25°C		_	4.00	8.00	Ω
Output Leakage Current		I _{OZ1}	—	V _{OUT} = 30V, EN = "L", 1bit		_	_	10	μA
		I _{OZ2}	_	V _{OUT} = 30V, E	_	_	100		
Input Current		I _{IN}	—	V _{IN} = V _{DD} or V	_	_	±1	μA	
	"H" Level	V _{IH}	_	—		0.7 V _{DD}	_	_	v
Input Voltage	"L" Level	V _{IL}	_		0	_	0.3 VDD		
Voltage Supervis	er Operating Voltage	V _{VS}	_		2.0	_	4.0	V	
Supply Current		I _{DD}	_		_	_	300	μA	
Operating Supply Current		I _{DD1}	_	$ f_{CLK} = 5MHz, Duty = 50\% \\ Data = 1 / 2 f_{CLK}, OUTPUT off \\ LATCH = "L", LATCH - Data \\ = "L" \\ f_{CLK} = 1MHz, Duty = 50\% \\ Data=1 / 64 f_{CLK} \\ All OUTPUT open \\ LATCH = "H", 1bit ON $		_	_	5.0	mA
		I _{DD2}	_			_	_	6.0	
Input Pull-Up Resistor		RV _{DD}	_	V _{DD} = 5.0 V, T	a = 25°C	150	300	600	kO
Input Pull-Down	Resistor	RV _{SS}	_	V _{DD} = 5.0 V, T	a = 25°C	150	300	600	kΩ
Internal Clock Fre	equency	f _{int}	_	V _{DD} = 5.0 V, T	a = 25°C	400	800	_	kHz

RECOMMENDED TIMING CONDITIONS (Ta = -40~85°C, V_{DD} = 4.5~5.5 V, V_{SS} = 0 V)

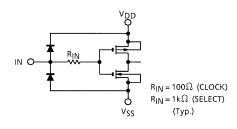
CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN	TYP.	МАХ	UNIT
Clock Pulse Width	^t w CLK	_	50	_	_	ns
Enable Pulse Width	t _{w EN}	—	0.5	_	_	μs
Latch Pulse Width	t _w T	_	50	_	_	ns
Clear Pulse Width	t _{w CLR}	—	80	_	_	ns
Data Set up Time	t _{setup}	—	37	50	—	ns
Data Hold Time	t _{hold}	_	50	—	_	ns

SWITCHING CHARACTERISTICS (Ta = 25°C, V_{DD} = 5 V, V_{OUT} = 26 V, R_1 = 650 Ω , C_L = 15 pF)

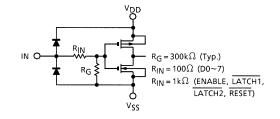
CHARACTER	STIC	SYMBOL	TEST CONDITION	MIN	TYP.	MAX	UNIT
	CLK-Outn		MMV-C / R = "L"	_	_	1000	
CLK-Outin $R - Outin$ $LAT1 - Outin$ $LAT1 - Outin$ $LAT1 - Outin$ $LAT2 - Outin$ $LAT2 - Outin$ $EN - Outin$	R - Outn		MMV-C / R = "L"	_	_	1000	
	_	_	1000	ns			
	LAT2 - Outn	pen	MMV-C / R = "L"	_	_	1000	
	EN- Outn		R = 750 kΩ, C = 2600 pF,Ta = 25°C	_	_	2500	
	CLK-Outn		MMV-C / R = "L"	_	_	1000	
(Low-to-High) Propagation Delay Time (High-to-Low) Set Up Time Hold Time Clock Pulse Width Latch Pulse Width Reset Pulse Width Enable Pulse Width Output Rise Time Output Fall Time	LAT1 - Outn		MMV-C / R = "L"	_	_	1000	1
	LAT2 - Outn	t _{pHL}	MMV-C / R = "L"	_	_	1000	ns
	EN- Out _n			_	_	2500	
Set Up Time	CLK-LATn	t _{setup} (L)	_	_	70	120	
Set op Time	CLK-S-IN	t _{setup} (D)	_	_	_	30	ns
Hold Time	CLK-LATn	t _{hold (L)}	-	—	_	0	115
	CLK-S-IN	t _{hold} (D)	-	—	_	20	
Clock Pulse Width		t _{w CLK}	—	—	-	50	ns
Latch Pulse Width		t _{w LATn}	-	—	_	50	ns
Reset Pulse Width		t _w R	—	—	-	50	ns
Enable Pulse Width		t _{w EN}	—	_	_	400	ns
Output Rise Time		t _{or}	OUTn	—	200	500	ns
Output Fall Time		t _{of}	OUTn	_	200	500	ns
Maximum Clock Frequenc	у	f _{MAX}	Duty = 50%	10	15	—	
Voltage Superviser Operat	ting Pulse Width	t _{w VS}	V _{DD (H)} = 5 V, V _{DD (L)} = 2 V	—	200	—	
MMV Reset Time		t _{MM∨}	R = 750 kΩ, C = 2600 pF,Ta = 25°C	1	3	5	

EQUIVALENT OF INPUTS AND OUTPUT CIRCUIT

1. CLOCK, SELECT

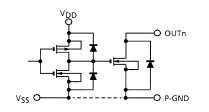


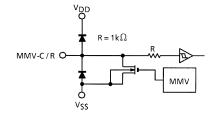
2. ENABLE, LATCH1, LATCH2, RESET, D0~7



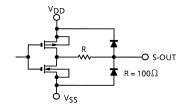








5. S-OUT, MMV-OUT



PRECAUTIONS for USING

This IC does not integrate protection circuits such as overcurrent and overvoltage protectors.

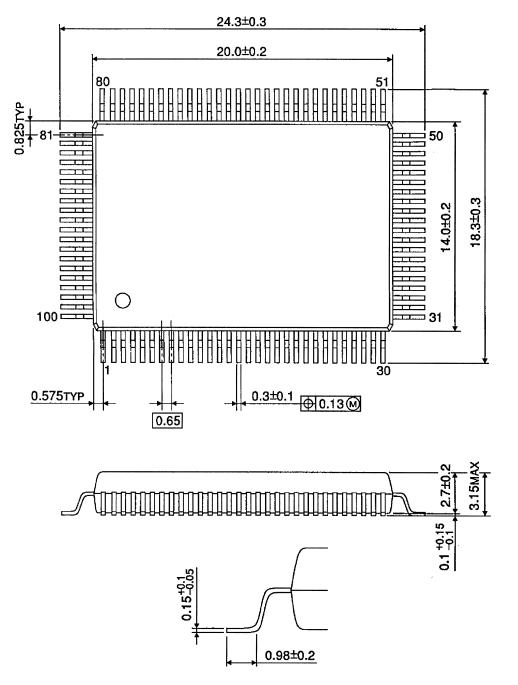
Thus, if excess current or voltage is applied to the IC, the IC may be damaged. Please design the IC so that excess current or voltage will not be applied to the IC.

Utmost care is necessary in the design of the output line, V_{CC} (V_{DD}) and GND (L–GND, P–GND) line since IC may be destroyed due to short–circuit between outputs, air contamination fault, or fault by improper grounding.

PACKAGE DIMENSIONS

QFP100-P-1420-0.65C

Unit: mm



Weight: 1.6 g (typ.)

Notes on Contents

1. Block Diagrams

Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

2. Equivalent Circuits

The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

3. Timing Charts

(4)

Timing charts may be simplified for explanatory purposes.

IC Usage Considerations

Notes on Handling of ICs

- The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings. Exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.
- (2) Use an appropriate power supply fuse to ensure that a large current does not continuously flow in case of over current and/or IC failure. The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow and the breakdown can lead smoke or ignition. To minimize the effects of the flow of a large current in case of breakdown, appropriate settings, such as fuse capacity, fusing time and insertion circuit location, are required.
- (3) If your design includes an inductive load such as a motor coil, incorporate a protection circuit into the design to prevent device malfunction or breakdown caused by the current resulting from the inrush current at power ON or the negative current resulting from the back electromotive force at power OFF. IC breakdown may cause injury, smoke or ignition. Use a stable power supply with ICs with built-in protection functions. If the power supply is unstable, the protection function may not operate, causing IC breakdown. IC breakdown may cause injury,

 Smoke or ignition.

 Do not insert devices in the wrong orientation or incorrectly.

Make sure that the positive and negative terminals of power supplies are connected properly.
Otherwise, the current or power consumption may exceed the absolute maximum rating, and exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.
In addition, do not use any device that is applied the current with inserting in the wrong orientation or incorrectly even just one time.

(5) Carefully select external components (such as inputs and negative feedback capacitors) and load components (such as speakers), for example, power amp and regulator. If there is a large amount of leakage current such as input or negative feedback condenser, the IC output DC voltage will increase. If this output voltage is connected to a speaker with low input withstand voltage, overcurrent or IC failure can cause smoke or ignition. (The over current can cause smoke or ignition from the IC itself.) In particular, please pay attention when using a Bridge Tied

Load (BTL) connection type IC that inputs output DC voltage to a speaker directly.

Points to Remember on Handling of ICs

(1) Heat Radiation Design

In using an IC with large current flow such as power amp, regulator or driver, please design the device so that heat is appropriately radiated, not to exceed the specified junction temperature (Tj) at any time and condition. These ICs generate heat even during normal use. An inadequate IC heat radiation design can lead to decrease in IC life, deterioration of IC characteristics or IC breakdown. In addition, please design the device taking into considerate the effect of IC heat radiation with peripheral components.

(2) Back-EMF

When a motor rotates in the reverse direction, stops or slows down abruptly, a current flow back to the motor's power supply due to the effect of back-EMF. If the current sink capability of the power supply is small, the device's motor power supply and output pins might be exposed to conditions beyond maximum ratings. To avoid this problem, take the effect of back-EMF into consideration in system design.

About solderability, following conditions were confirmed

- Solderability
 - (1) Use of Sn-37Pb solder Bath
 - solder bath temperature = 230°C
 - · dipping time = 5 seconds
 - $\cdot \,$ the number of times = once
 - use of R-type flux
 - (2) Use of Sn-3.0Ag-0.5Cu solder Bath
 - \cdot solder bath temperature = 245°C
 - · dipping time = 5 seconds
 - \cdot the number of times = once
 - use of R-type flux

RESTRICTIONS ON PRODUCT USE

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