SSI 73M3522
Bell 212A/V.22 Modem Filter

July, 1989

DESCRIPTION

The SSI 73M3522 is a 16 pin CMOS integrated circuit that provides the channel filtering and equalization functions required for Bell 212A and CCITT V.22 modem applications. Employing switched capacitor filter techniques, the 73M3522 includes channel separation filters optimized for 1200 and 2400 Hz operation, while maintaining the bandshape necessary to reject 550 and 1800 Hz guard tones typical for V.22 standard modems. Fixed compromise equalization and group delay correction is distributed between the two channels as prescribed by V.22 recommendations. Dual multiplexers provide channel steering action for answer/originate control using a single pin.

The 73M3522 is designed to provide the front end for a Bell 212A or V.22 modem design. Optimized for PSTN lines, the 73M3522 offers an economical solution to the filter requirements of medium speed modem designs.

FEATURES

- **Performs Bell 212A/V.22 channel filter functions**
- **High performance/low cost filter for medium speed modems**
- **Compromise equalization**
- **Single pin originate/answer steering logic**
- **Selectable clock divider-2.304 MHz or 3.5795 MHz color burst frequency**
- **± 5V operation at 50 mW typical power consumption**
- **CMOS technology and I/O compatibility**
- **16 pin DIP configuration**
- **CMOS latch-up protected**

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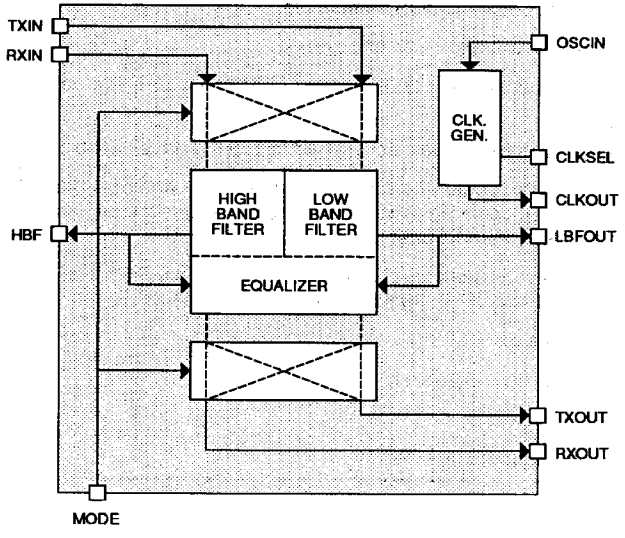
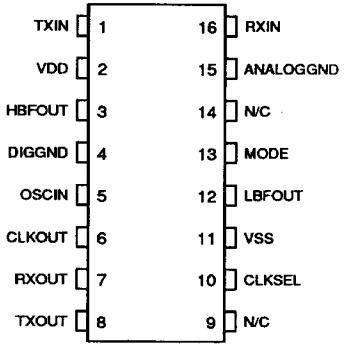
BLOCK DIAGRAM



PIN DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

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SSI 73M3522
Bell 212A/V.22
Modem Filter

FUNCTIONAL DESCRIPTION

GENERAL

The SSI 73M3522 is designed to act as a low cost filter for use in Bell 212A or V.22 modem designs. The device consists of high and low band filters, split compromise equalizers for the two channels, and dual multiplexer logic for originate/answer channel steering. The unbuffered filter outputs are brought out to pins LBF and HBF before the signals have been processed by the equalizer section, and may be used for test purposes or in applications where the equalizer must be bypassed. Output impedance of these pins is 100 KΩ, requiring buffering if significant loads are to be driven. A clock generator provides the switched capacitor clock sampling frequency of 52.36 KHz from a 2.304 MHz buffered input signal. Tying pins 10 and 11 together changes the internal scaling rate to allow use of a 3.5795 MHz input, which can be generated from a standard color burst crystal. Filter response is essentially flat for a passband centered around the 1200 and 2300 Hz center frequencies, while notch filters located at 550 and 1800 Hz insure excellent rejection of CCITT guard tones.

DESIGN CONSIDERATIONS

The SSI 73M3522 uses SCF sampled data techniques. To avoid signal aliasing problems the input signal should not contain significant energy within 3 KHz of any multiple of the 52.36 KHz sampling clock. An anti-aliasing filter may be needed to meet this requirement.

When the alternate clock input is selected, a rate multiplier is inserted in the normal clock divider circuit. This shifts the SCF clock frequency to 52.30 KHz and the CLKOUT pin output to 104.6 KHz. In addition, a low level modulation tone at approximately 23 KHz will be generated with a typical amplitude of less than 600 μV RMS. Normal applications will not be affected by these changes.

PIN DESCRIPTIONS

NAME	I/O	DESCRIPTION
ANALOGGND	I	Analog ground pin - separate from digital ground.
CLKOUT	O	104.5 KHz SCF clock output, CMOS compatible.
DIGGND	I	Digital ground pin - separate from analog ground.
HBFOUT	O	High band filter output before equalization. Limited to 100 KΩ drive capability.
LBFOUT	O	Low band filter output before equalizer. Limited to 100 KΩ drive capability.
MODE	I	Channel steering control. Logic 1 selects the answer mode, with high-band transmit and low-band receive signal routing. A logic 0 selects the originate mode with the opposite channel orientation.
OSCIN	I	Accepts a CMOS level frequency reference at 2.304 or 3.5795 MHz as selected to generate the SCF 52.36 KHz clock used internally.
RXIN	I	Receive signal filter input.
RXOUT	O	Receive signal output from equalizer.
TXIN	I	Transmit signal filter input.
TXOUT	O	Transmit signal output from equalizer.

PIN DESCRIPTIONS (Continued)

NAME	I/O	DESCRIPTION
VDD	I	+5V -5%, +25% power input.
VSS	I	-5V +5%, -25% power input.
CLKSEL	I	Clock select pin. Connecting pins 10 and 11 changes the internal divider ratio to allow use of a standard 3.5795 MHz color burst crystal reference to generate the 52.36 KHz SCF clock. The 2.304 MHz clock input is selected when pin 10 is left open (has internal pull-up).

ELECTRICAL SPECIFICATIONS

DIGITAL SIGNALS (pins 5,6,10,13)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
VIH	High level input voltage		3.75			V
IIH	High level input current				10	µA
VIL	Low level input voltage				0.8	V
IIL	Low level input current				-10	µA

CLOCK INPUT (pin 5)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Input clock frequency	See note				
Input clock duty cycle		20		80	%

Note: 2.304 MHz or 3.5795 MHz ±0.01%

ANALOG SIGNALS (pins 1,2,3,4,7,8,11,12,15,16)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
VDD	Supply voltage		4.75		6.25	V
VSS	Supply voltage		-4.75		-6.25	V
IDD	Supply current	VDD = 5.0V			10	mA
ISS	Supply current	VSS = -5.0V			-10	mA

ANALOG SIGNALS (Continued)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
Zin	Input impedance		10			KΩ
Zout	Output impedance	pins 3, 12		100		KΩ
Zout	Output impedance	pins 7, 8			1	KΩ
	Output noise	C-message			950	µV RMS
	Channel separation		50			dB
	Input signal level				VDD -2.0	V P-P
	Supply imbalance	VDD + VSS			0.5	V
	Operating temperature range		0		70	°C
	Storage temperature range		-55		125	°C

TYPICAL PERFORMANCE

(TA = 25°C, VDD = 5.0V, VSS = -5.0V)

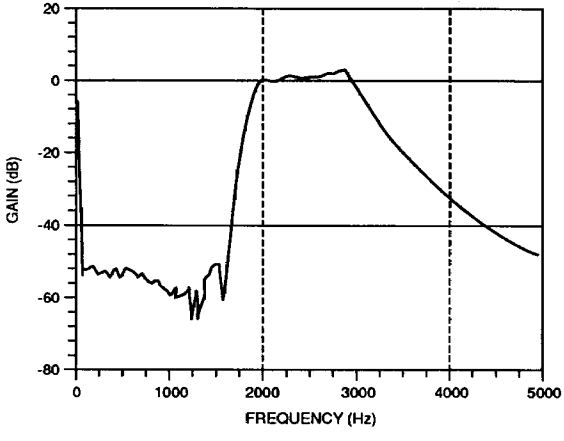


FIGURE 1: High Band Amplitude Response (dB)

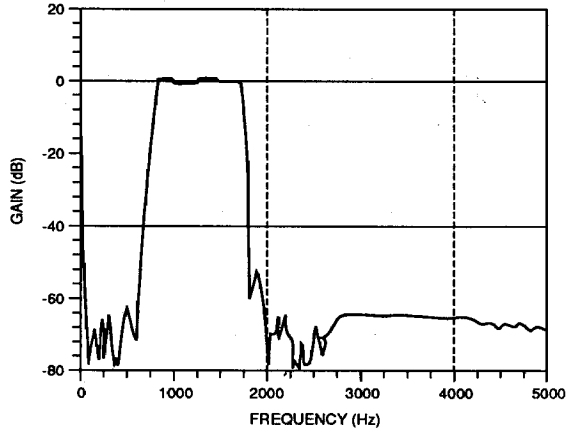


FIGURE 2: Low Band Amplitude Response (dB)

TYPICAL FREQUENCY RESPONSE

(TA = 25°C, VDD = 5.0V, VSS = -5.0V)

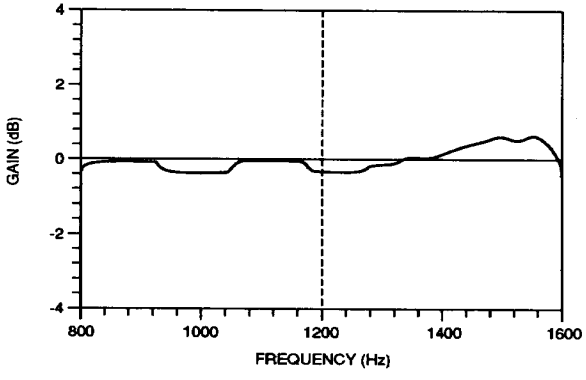


FIGURE 3: Low Band Amplitude Response (dB)

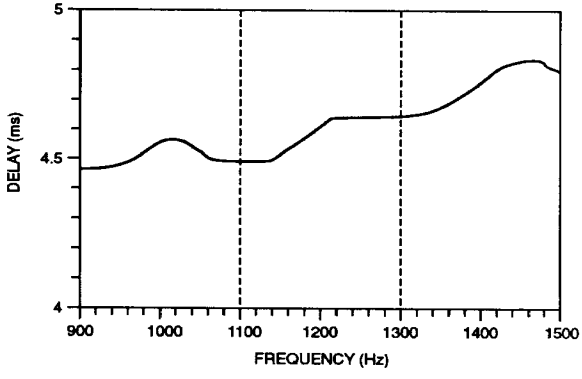


FIGURE 4: Low Band Group Delay (ms)

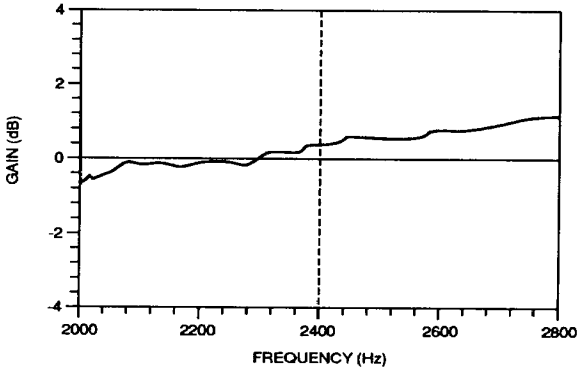


FIGURE 5: High Band Amplitude Response (dB)

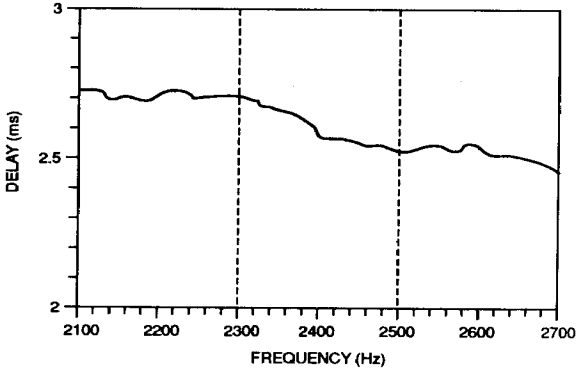
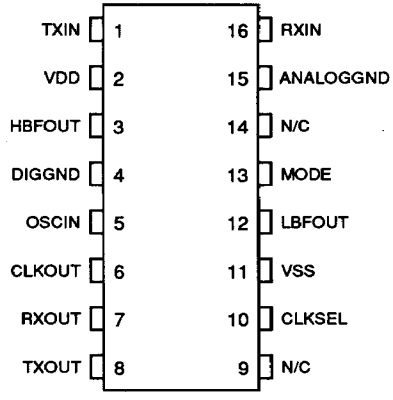


FIGURE 6: High Band Group Delay (ms)

PACKAGE PIN DESIGNATIONS
(TOP VIEW)



16-pin DIP

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 73M3522 16-pin DIP	SSI 73M3522-CP	73M3522-CP