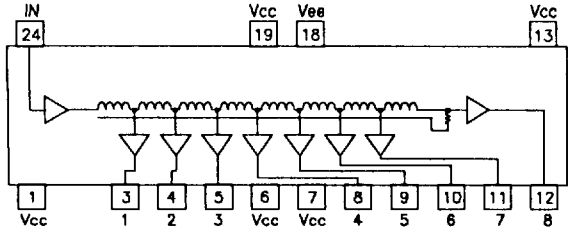
8 Tap 100K ECL Buffered Delay Modules



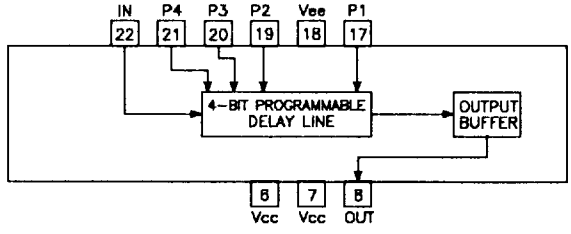
GENERAL: For Operating Specifications and Test Conditions, see Tables VI and VIII on page 7 of this catalog. Delays specified for the Leading Edge.

Minimum Input Pulse Width, **DDECL** ..... 30% of total delay
Temperature Coefficient of Delay ..... 300ppm/°C typical
Supply Current, I_{EE}, **DDECL** ..... 85 mA typ., 115 mA max.

Electrical Specifications at 25°C

Part Number	Tap 1 (ns)	Tap 2 (ns)	Tap 3 (ns)	Tap 4 (ns)	Tap 5 (ns)	Tap 6 (ns)	Tap 7 (ns)	Total - Tap 8 (ns)	Tap-to-Tap (ns)
DDECL-16	2 ± .5	4 ± .5	6 ± 0.75	8 ± 0.75	10 ± 1.0	12 ± 1.0	14 ± 1.0	16 ± 1.00	2.0 ± 0.5
DDECL-20	2.5 ± .5	5 ± .5	7.5 ± 0.75	10 ± 1.0	12.5 ± 1.0	15 ± 1.0	17.5 ± 1.0	20 ± 1.00	2.5 ± 0.8
DDECL-24	3 ± .5	6 ± 0.75	9 ± 1.0	12 ± 1.0	15 ± 1.0	18 ± 1.0	21 ± 1.5	24 ± 1.50	3.0 ± 0.8
DDECL-32	4 ± .5	8 ± 1.0	12 ± 1.0	16 ± 1.0	20 ± 1.0	24 ± 1.5	28 ± 1.5	32 ± 1.50	4.0 ± 1.0
DDECL-40	5 ± .5	10 ± 1.0	15 ± 1.5	20 ± 1.5	25 ± 1.5	30 ± 1.5	35 ± 1.5	40 ± 1.50	5.0 ± 1.0
DDECL-48	6 ± 1.0	12 ± 1.0	18 ± 1.5	24 ± 1.5	30 ± 1.5	36 ± 1.5	42 ± 1.5	48 ± 1.50	6.0 ± 1.0
DDECL-56	7 ± 1.0	14 ± 1.0	21 ± 1.5	28 ± 1.5	35 ± 1.5	42 ± 2.0	49 ± 2.0	56 ± 2.00	7.0 ± 1.5
DDECL-64	8 ± 1.0	16 ± 1.5	24 ± 1.5	32 ± 1.5	40 ± 2.0	48 ± 2.0	56 ± 2.0	64 ± 2.50	8.0 ± 1.5
DDECL-80	10 ± 1.5	20 ± 2.0	30 ± 2.0	40 ± 2.0	50 ± 2.0	60 ± 2.5	70 ± 2.5	80 ± 3.00	10.0 ± 1.5
DDECL-96	12 ± 1.5	24 ± 2.0	36 ± 2.0	48 ± 2.0	60 ± 2.5	72 ± 3.0	84 ± 3.5	96 ± 4.50	12.0 ± 2.0

4-Bit Programmable 100K ECL Delay Modules



GENERAL: For Operating Specifications and Test Conditions, see Tables VI and VIII on page 7 of this catalog. Delays specified for the Leading Edge.

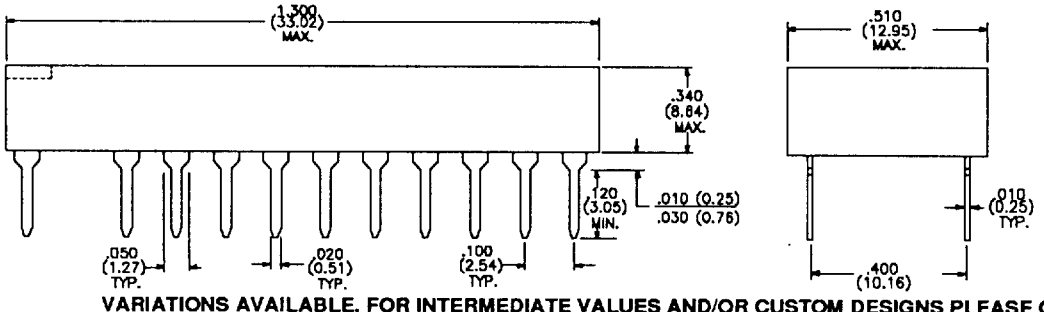
INPUT LOADING: Input, Pin 22, internally connected to 16 ea. 100K inputs terminated by Thevenin equivalent of 100 Ohms to -2V.

Minimum Input Pulse Width, **PPECL** ..... 30% of total delay
Temperature Coefficient ..... 300ppm/°C typical
Supply Current, I_{EE}, **PPECL** ..... 85 mA typ., 115 mA max.

CUMULATIVE TOLERANCES: Maximum Deviation Tolerances for Programmed Delays Referenced to Initial Delay, Setting "0000." Tables display values of delay with respect to input, whose tolerance is the cumulative error of the initial delay (± 1.0) and the Maximum Deviation. For example, the setting "1111" delay of PPECL2-1 is 15.0 ± 1.0 ref. to "0000," and 17.0 ± 1.5 ref. to the input.

Electrical Specifications at 25°C

4 Bit 100K ECL Part Number	Delay per Step (ns)	Output Delay (ns) per Program Setting (P4*P3*P2*P1)																Max. Deviation ref. to 0000 (ns)
		0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111	
PPECL2-0.2	0.2 ± .10	2.0 ± 0.5	2.2	2.4	2.6	2.8	3.0	3.2	3.4	3.6	3.8	4.0	4.2	4.4	4.6	4.8	5.0	± 0.3
PPECL2-0.25	0.25 ± .10	2.0 ± 0.5	2.25	2.50	2.75	3.00	3.25	3.50	3.75	4.00	4.25	4.50	4.75	5.00	5.25	5.50	5.75	± 0.5
PPECL2-0.5	0.5 ± .25	2.0 ± 0.5	2.5	3.0	3.5	4.0	4.5	5.0	5.5	6.0	6.5	7.0	7.5	8.0	8.5	9.0	9.5	± 0.7
PPECL2-1	1.0 ± 0.5	2.0 ± 0.5	3.0	4.0	5.0	6.0	7.0	8.0	9.0	10.0	11.0	12.0	13.0	14.0	15.0	16.0	17.0	± 1.0
PPECL2-1.5	1.5 ± 0.5	2.0 ± 0.5	3.5	5.0	6.5	8.0	9.5	11.0	12.5	13.0	14.5	16.0	17.5	19.0	20.5	22.0	23.5	± 1.5
PPECL2-2	2.0 ± 0.6	2.0 ± 0.5	4.0	6.0	8.0	10.0	12.0	14.0	16.0	18.0	20.0	22.0	24.0	26.0	28.0	30.0	32.0	± 1.5
PPECL2-2.5	2.5 ± 0.6	2.0 ± 0.5	4.5	7.0	9.5	12.0	14.5	17.0	19.5	22.0	24.5	27.0	29.5	32.0	34.5	37.0	39.5	± 1.5



Physical Dimensions
inches (mm)

Per Schematics above, unused pins are removed from the 24 Pin outline.

VARIATIONS AVAILABLE. FOR INTERMEDIATE VALUES AND/OR CUSTOM DESIGNS PLEASE CONSULT THE FACTORY.

Specifications subject to change without notice.

DDECL-6/93

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