

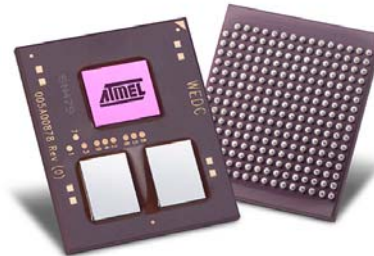
PC755 Microprocessor + 1MByte L2-Cache Multi-Chip Module Fact Sheet

Main Features

- PC755B RISC microprocessor
- 8 Mbit of Synchronous Pipelined Burst SRAM configured as 128Kx72 (L2-Cache)
- Extended temperature modules 2.0V (Core)/3.3V (I/O) for industrial and military applications

Multi-Chip Module Benefits

- 60% space savings
- Reduced ball count from 560 down to 255; reduced PWB density, reduced PWB cost
- Eliminates high-speed memory board design
- Suitable for hi-rel applications
- Reliability data available upon request
- Reduced part count
- Scalable and expandable
- Footprint compatible with PCX745BVZFUxxxLE
- Upgradeable to PC7410M16MGxxxLE



Performance Features

- Core Frequency: 300 MHz, 350 MHz
- L2 Cache Frequency: 150 MHz, 175 MHz
- 60x Bus Frequency: 66 MHz

	Discrete Approach	PC755BM8MGxxx	Space Savings
Area	$625\text{mm}^2 + 2 \times 352\text{mm}^2 = 1329\text{mm}^2$	525mm^2	60%
I/O Count	360 BGA + 200 TQFP = 560	255	54%



• **Packaging**

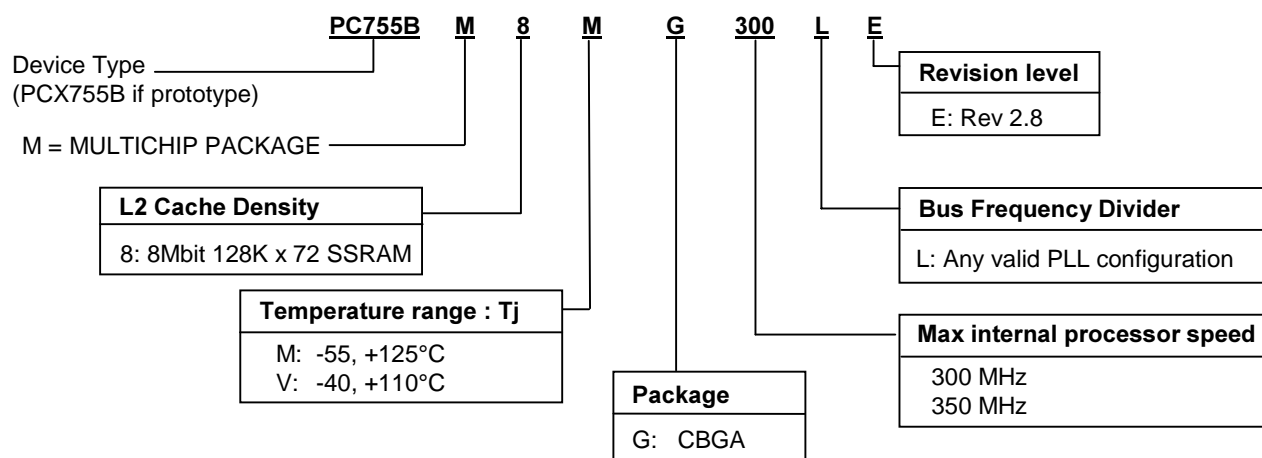
- 25x21mm, 255-pin Ceramic BGA
- 21mm x 25mm CI-CGA (optional/developmental)
- 525mm² Multilayer ceramic interposer, Al₂O₃
- High reliability flip-chip die attach: C4 process on 755 & SSRAM
- JEDEC level 2 underfill optimized for ceramic bond
- Same technology used reliability in automotive industry for over 30 years
- Lowest possible inductance chip interconnect technology
- Highest possible chip density for reduced interposer dimension

• **Ball attach**

- Ball diameter/height: 0.80mm before reflow
- 1.27mm pitch
- 255 balls in 16x16 array (minus one – for optical)
- Module height: 3.90 mm max

• **Screening**

- Full Military temperature range: T_j = -55°C to +125°C
- Industrial temperature range: T_j = -40°C to +110°C



For availability of the different versions, please contact your Atmel sales office or visit our web site at <http://www.atmel.com>

You may also contact the PowerPC technical hotline at std.hotline@gfo.atmel.com



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