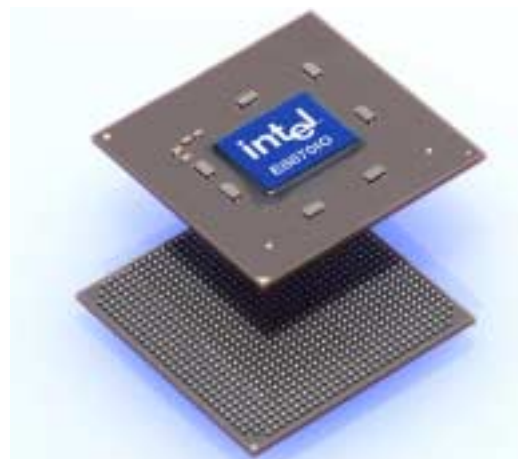# intel®

Intel® E8870IO Server I/O Hub (SIOH) Datasheet

Product Features

- Scalability Port (SP):
  — Two SPs with 3.2 GB/s peak bandwidth per direction per SP.
  — Bi-directional SPs for a total bandwidth of 12.8 GB/s.
- Four Hub Interface 2.0 Ports:
  — For connecting to Intel® 82870P2 PCI/ PCI-X 64-bit Hub 2 (P64H2).
  — 16-bit, 533 MHz interface.
  — 1 GB/s peak data rate.
- One Hub Interface 1.5 Port:
  — For connecting to Intel® 82801DB. Legacy I/O Controller Hub 4 (ICH4).
  — 8-bit, 266 MHz interface.
  — 266 MB/s peak data rate.
- Supports peer-to-peer write traffic between Hub Interface Ports.
- Dedicated read cache for each Hub Interface Port:
  — 32 128-byte cache lines.
  — Dedicated prefetch engines for Hub Interface 2.0 ports.
- Supports caching of frequently used and prefetched data residing in main memory.
- 64-line write cache.

- Aggressive prefetching algorithm optimized for PCI-X functionality supported by the 82870P2 component:
  — Utilizing enhanced features such as read-streaming, and prefetch horizon.
- Supports multiple unordered inbound traffic streams:
  — Two unordered streams per Hub Interface 2.0 port.
  — One stream for the Hub Interface 1.5 port.
- System Management Bus (SMBus) 2.0 slave interface for server management with Packet Error Checking.
- Reliability, Availability, and Serviceability (RAS):
  — Sideband access to configuration registers via SMBus SMBus or JTAG.
  — End-to-end ECC for all interfaces.
  — Fault detection and logging.
  — Signal connectivity testing via. boundary scan.
- Packaging:
  — 42.5 mm x 42.5 mm
  — 1012-pin organic LAN grid array (OLGA) package-2B.

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August 2002

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Introduction 1

1.1 Overview

The Intel® E8870 chipset delivers new levels of availability, features, and performance for servers. It provides flexible common modular architecture support for the Intel® Itanium® 2 processor family. The E8870 chipset up to four processors in a single node configuration, and up to eight processors in a multi-node configuration using the Scalability Port Switch (SPS) component, delivering stability to platforms through reuse and common architecture support.

The component names used throughout this document refer to the component markings listed in Table 1-1.

Table 1-1. Chipset Component Markings

Component Name	Product Marking
SNC	E8870
SIOH	E8870IO
SPS	E8870SP
DMH	E8870DH
P64H2	82870P2
ICH4	82801DB
FWH	82802AC

1.2 Server I/O Hub Architectural Overview

The Intel® E8870IO Server I/O Hub (SIOH) component provides connectivity between the I/O bridge components and the other components in the E8870 chipset. The SIOH is capable of interfacing to a total of five I/O bridges via Hub Interface ports. The E8870 chipset may include up to two SIOH components, depending on the configuration.

The example in Figure 1-1 illustrates a typical eight-way configuration. A four-way single node configuration would consist of one SIOH and one SNC component. The SIOH is capable of interfacing up to four P64H2 I/O bridge devices via the 16-bit Hub Interface 2.0 compliant ports. The 8-bit Hub Interface 1.5 compliant port is used to connect an ICH4 bridge device, providing legacy I/O functionality.

Note: One ICH4 is used in both single and multi-node configurations.

Figure 1-1. Typical Intel® E8870 Chipset-Based Eight-Way Itanium® 2 Server System Configuration
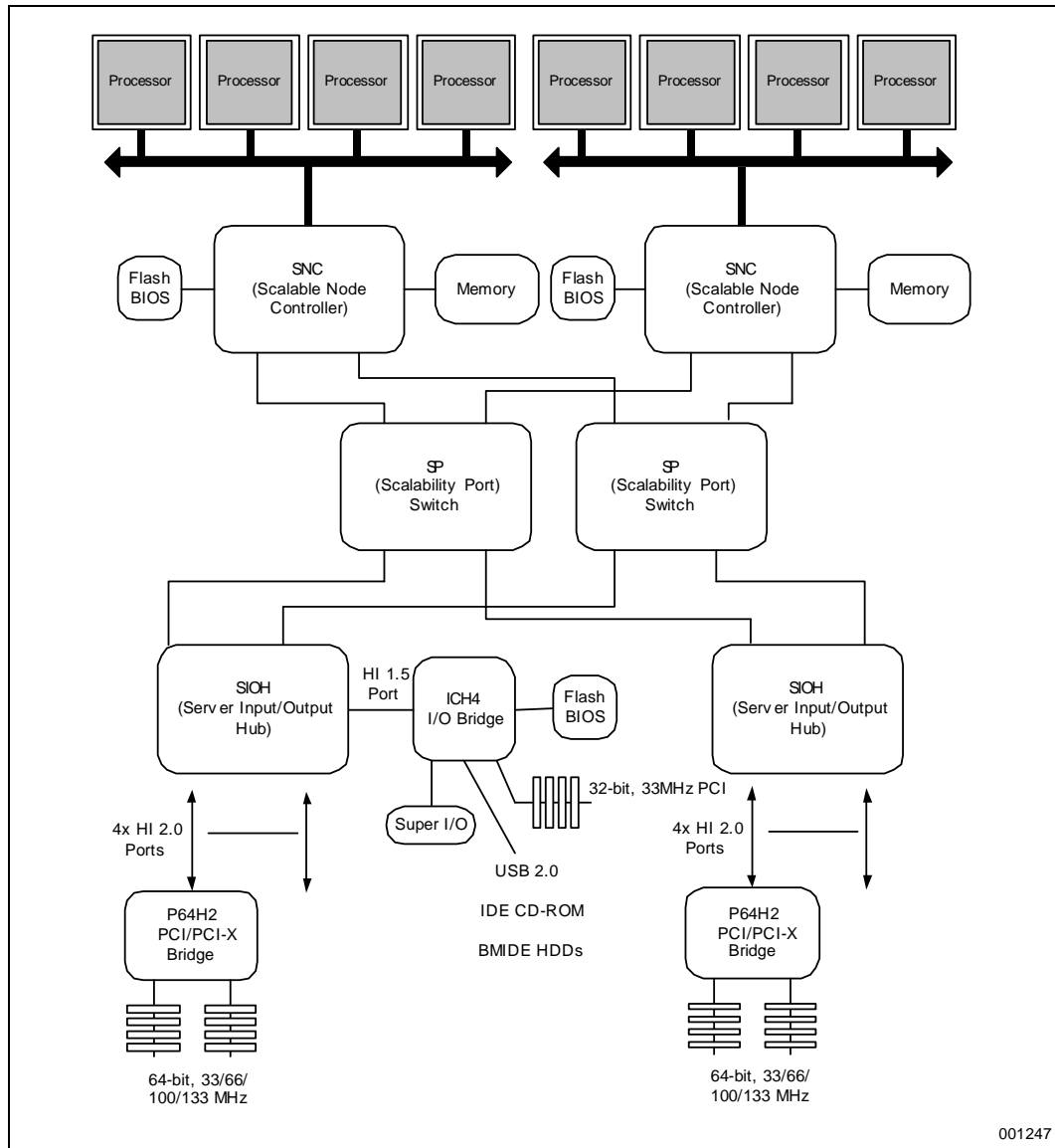
1.3 Interfaces

The SIOH component functions as a hub between multiple I/O ports (Hub Interfaces) and the other host bridge components. The SIOH connects the multiple I/O ports to the memory subsystem, the host processors, and other SIOH components. This section provides an overview of the SIOH functionality as three high-level functional blocks:

- Hub Interface
- Internal Interconnect
- Scalability Port Interface

Refer to Figure 1-2 and Figure 1-3.

Figure 1-2. SIOH Interfaces

Scalability Port

Scalability Port

Write Cache

Traffic Routing

Read Cache

Read Cache

Read Cache

Read Cache

Read Cache

SIOH

Hub Interface Rev. 1.5 Compliant

Hub Interface (8-bit)

Hub Interface (16-bit)

Hub Interface (16-bit)

Hub Interface (16-bit)

Hub Interface (16-bit)

Hub Interface Rev. 2.0 Compliant

001125
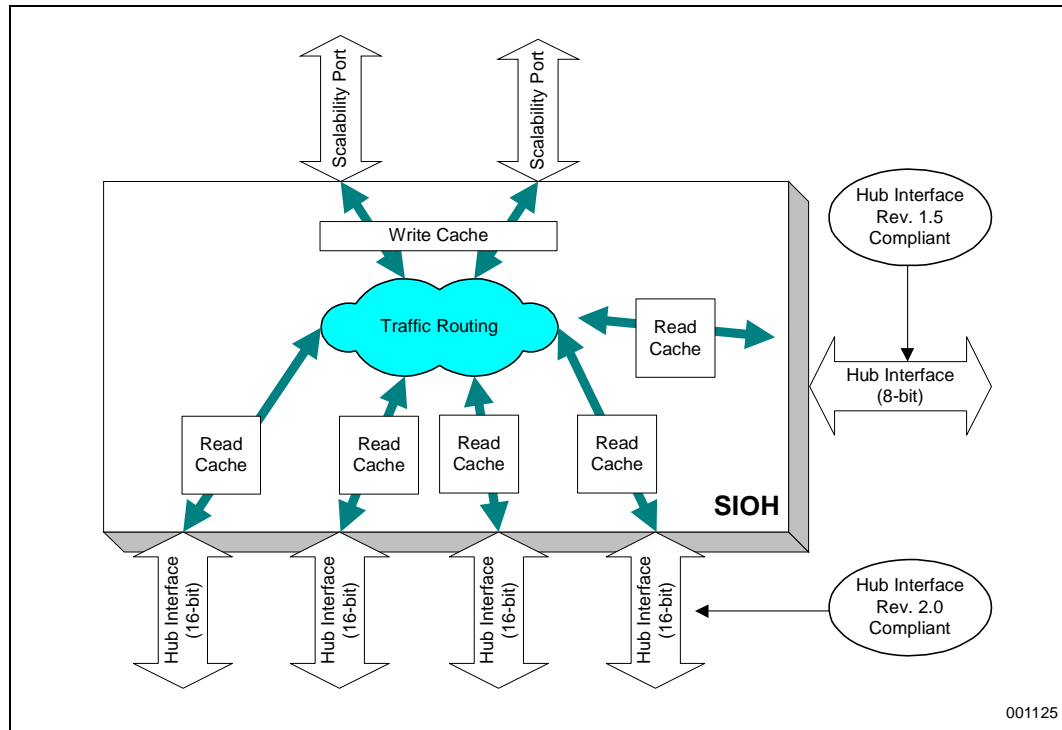
The SIOH is responsible for routing traffic between the different Hub Interfaces and Scalability Ports.

Figure 1-3. SIOH Functional Blocks

Scalability Port

Scalability Port

Scalability Port Interface

Config Registers

Internal Interconnect

Hub Interface

Hub Interface

Hub Interface

Hub Interface

Hub Interface

Hub Interface Rev. 1.5 Compliant

Hub Interface (8-bit)

Hub Interface 16-bit

Hub Interface 16-bit

Hub Interface 16-bit

Hub Interface 16-bit

Hub Interface Rev. 2.0 Compliant

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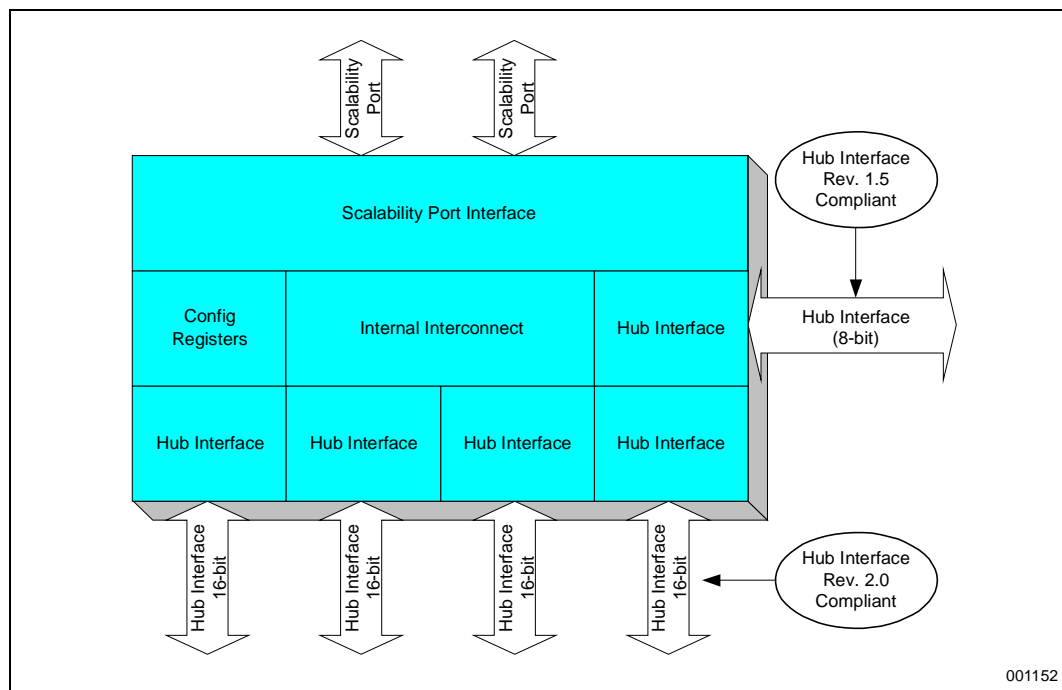
1.4   Scalability Port Interface

The Scalability Port (SP) interface is responsible for accepting and sending packets between the SIOH and either the SPS or SNC components. The SIOH SP interface consists of two SP ports. The SP is a cache-coherent interface optimized for scalable multi-node systems that maintain coherency between all processors and their caches.

The SP uses a point-to-point bus topology using source-synchronous data transfer. In order to reduce pin counts, the SP uses Simultaneous Bi-directional (SBD) signalling technology. SBD technology eliminates any arbitration delays since data can be transmitted in both directions simultaneously. The SP interface includes a 40-bit data interface (32-bits of data and 8-bits of ECC) operating at 800MHz, resulting in 3.2 GB/s in each direction per SP.

1.5   Hub Interface

The Hub Interface is responsible for accepting and sending Hub Interface packets between the SIOH and an I/O bridge. The I/O bridges supported are P64H2 (Hub Interface-to-PCI bridge), ICH4 (Hub Interface-to-Compatibility bridge).

For the SIOH, there are four Hub Interface 2.0 ports and one 8-bit Hub Interface 1.5 port.

All Hub Interface ports support parallel termination. Parallel termination is required for the routing distances required for E8870 chipset-based platforms.

Hub Interface uses a point-to-point bus topology using source-synchronous data transfer. Hub Interface uses impedance matching techniques (RCOMP) for optimal signal integrity. It dynamically adjusts the driver impedance to match the impedance of the traces on the board throughout thermal variations. Impedance adjustment is accomplished using a dedicated pin (HLxRCOMP) connected to an external resistor that equals the impedance of the Hub Interface traces.

For optimal scalability, the Hub Interface cluster is replicated for each Hub Interface port.

1.6   SMBus Interface

The SIOH supports a SMBus 2.0 compatible slave interface to provide register visibility for a server management subsystem. This low cost port is a two-pin (SDA, SCL) serial interface useful for communicating with a baseboard management controller. The interface supports 100 kHz.

The interface allows for a multi-master subsystem, which means more than one device can initiate data transfers at the same time. To support this feature, the SMBus bus arbitration relies on the wired-AND connection of all SMBus interfaces. Two masters can drive the bus simultaneously provided they are driving identical data. The first master drives SDA high, while another master drives SDA low loses the arbitration. The SCL signal consists of a synchronized combination of clocks generated by the masters using the wired-AND connection to the SCL signal.

The SMBus serial operation uses an open-drain wired-AND bus structure that allows multiple devices to drive the bus lines and to communicate status about events such as arbitration, wait states, error conditions and so on. For example, when the slave is unable to accept or drive data at the rate that the master is requesting, the slave can hold the clock line low between the high states to insert a wait interval. The master's clock can only be altered by a slower slave peripheral keeping the clock line low or by another master during arbitration.

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1.7   JTAG Tap Port

The SIOH supports the IEEE 1149.1 (JTAG) Test Access Port (TAP) for test and debug. The TAP interface is a serial interface comprised of five signals: TDI, TDO, TMS, TCK, and TRST#. The JTAG interface will operate from 4 to 25 MHz.

1.8   Terminology

Differential	Input buffer logic that requires a voltage reference or the signal complement.
Direct Connect/Single Node	Up to 4-way Itanium® 2 processor/E8870 chipset platform configuration that consists of one SIOH and SNC that are directly connected by Scalability Ports.
Dirty Node	The SNC or SIOH that owns a modified cache line.
FWH	Firmware Hub. This is the chipset Flash Memory component that typically provides the BIOS firmware code.
Hinted Peer-to-Peer	A transaction initiated by one of the P64H2 PCI/PCI-X buses destined for a target on the other PCI/PCI-X bus on the same P64H2.
Home Node	The SNC that controls the memory on which a particular cache line resides.
HVCMOS	3.3V CMOS I/O buffer logic.
Inbound Transactions	Transactions initiated on Hub Interface destined for the Scalability Port interface.
iGTL	Inverted GTL buffer logic.
IOxAPIC	I/O Advanced Programmable Interrupt Controller. Intel authored an interrupt specification that covers various methods for interrupting a host processor. Each I/O bridge contains an IOxAPIC controller for issuing these interrupts on behalf of their child devices.
Local Peer-to-Peer	A transaction initiated by one of the P64H2 PCI buses destined for a target on another Hub Interface port on the same SIOH.
LVHSTL	Low Voltage High Speed Tranceiver Logic
LVPECL	Low Voltage Positive Emitter Coupled Logic
Outbound Transactions	Transactions initiated on a Scalability Port destined for Hub Interface.
Phit	Physical unit of data transfer consisting of 40 bits of protocol level information.
PHP	PCI Hot-Plug.
Remote Peer-to-Peer	A transaction initiated by one of the P64H2 PCI buses destined for a target on another Hub Interface port on a different SIOH.

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SAPIC	Streamlined Advanced Programmable Interrupt Controller. Implemented in Itanium® 2 processor-based platforms, this interrupt mechanism uses inbound writes to specific addresses to interrupt the host processor.
SAR	I/O APIC Controller and Hot Plug Controller Range.
SBD	Simultaneous Bi-Directional.
SIOH	Server I/O Hub. This component is used for server platform configurations requiring high bandwidth and high connectivity I/O bus connectivity.
SNC	Scalable Node Controller. Includes the processor, memory, and Scalability Port interfaces.
SP	Scalability Port.
SPCMOS	Low speed SP I/O buffer logic.
SPS	Scalability Port Switch. The crossbar/central snoop filter that connects the SNCs and SIOHs.

1.9 Reference Documents

- *Intel® E8870 Scalable Node Controller (SNC) Datasheet*
- *Intel® E8870DH DDR Memory Hub (DMH) Datasheet*
- *Intel® E8870SP Scalability Port Switch (SPS) Datasheet*
- *Intel® 82870P2 64-bit Hub 2 (P64H2) Datasheet*
- *Intel® 82801DB I/O Controller Hub4 (ICH4) Datasheet*
- *SMBus Specification, Revision 2.0*
- *PCI Local Bus Specification, Revision 2.2*
- *PCI-X Local Bus Specification, Revision 1.0*

1.10 Revision History

Revision Number	Description	Date
-001	Initial release of the document.	August 2002

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Signal Description 2

2.1 Conventions

The terms *assertion* and *deassertion* are used extensively when describing signals, to avoid confusion when working with a mix of active-high and active-low signals. The term *assert*, or *assertion*, indicates that the signal is active, independent of whether the active level is represented by a high or low voltage. The term *deassert*, or *deassertion*, indicates that the signal is inactive.

Signal names may or may not have a "#" appended to them. The "#" symbol at the end of a signal name indicates that the active, or asserted state occurs when the signal is at a low voltage level. When "#" is not present after the signal name the signal is asserted when at the high voltage level.

The exception to the "#" symbol convention lies in the Hub Interface 1.5 signal description. Active is not applicable to HI 1.5. The reader is cautioned against attaching any meaning to the "#" symbol in HI 1.5 mode.

When discussing data values used inside the component, the logical value is used; i.e. a data value described as "1101b" would appear as "1101b" on an active-high bus and as "0010b" on an active-low bus. When discussing the assertion of a value on the actual pin, the physical value is used; i.e. asserting an active-low signal produces a "0" value on the pin.

The following notations are used to describe the signal types:

- I: Input pin
- O: Output pin
- I/O: Bi-directional (input/output) pin
- ASYNC: Asynchronous pin

2.2 Scalability Port (SP) Interface

The SP is the interface between the SIOH to the SPS and SNC components of the E8870 chipset (refer to Table 2-1).

Table 2-1. Scalability Port (SP) Signals

Signal Name	Type	Clock Domain	Description
SP{0/1}ZUPD[1:0]	I Analog	N/A	**Impedance Update:** Used to adjust the impedance of I/O drivers.
SP{0/1}SYNC	I/O CMOS1.5	ASYNC	**Reset Synchronization:** Provides synchronization between ports for impedance control and reference voltage adjustment. This signal is also used by the SP reset logic to determine when SP comes out of reset. SP{0/1}SYNC is released when ports at both ends of the link are ready.
SP{0/1}PRES	I CMOS1.5	N/A	**SP Present:** Signals the SP of an impending hot-plug event.

Table 2-1. Scalability Port (SP) Signals (Continued)

Signal Name	Type	Clock Domain	Description
SP{0/1}AVREFH[3:0]	I Analog	N/A	**Strand A Voltage Reference High:** 3/4 VCC reference.
SP{0/1}AVREFL[3:0]	I Analog	N/A	**Strand A Voltage Reference Low:** 1/4 VCC reference.
SP{0/1}ASTBP[1:0]	I/O SBD	400 MHz	**Strand A P Strobes:** Positive phase data strobes for Strand A to transfer data at the 2x rate (800 MHz).
SP{0/1}ASTBN[1:0]	I/O SBD	400 MHz	**Strand A N Strobes:** Negative phase data strobes for Strand A to transfer data at the 2x rate (800 MHz).
SP{0/1}AD[15:0]	I/O SBD	800 MHz	**Strand A Data Bus:** 16-bits of the data portion of a PHIT on Strand A. These bits are SSO encoded. SP{0/1}ASSO determines if these are out of an inverter or not.
SP{0/1}AEP[2:0]	I/O SBD	800 MHz	**Strand A Parity/ECC:** Two of these signals carry the ECC information for the data flits (AEP[1:0]). There are four bits of ECC for each data PHIT. The header flits are not ECC protected. The third signal is for parity (AEP[2]). Each PHIT is always protected by two bits of parity.
SP{0/1}ALLC	I/O SBD	800 MHz	**Strand A Link Layer Control:** For each PHIT these signals carry two of the four bits of link layer control information.
SP{0/1}ASSO	I/O SBD	800 MHz	**Strand A SSO Encode:** This signal is asserted to indicate that the data bits over Strand A are inverted.
SP{0/1}BVREFH[3:0]	I SBD	N/A	**Strand B Voltage Reference High:** 3/4 VCC reference.
SP{0/1}BVREFL[3:0]	I SBD	N/A	**Strand B Voltage Reference Low:** 1/4 VCC reference.
SP{0/1}BSTBP[1:0]	I/O SBD	400 MHz	**Strand B P Strobes:** Positive phase data strobes for Strand B to transfer data at the 2x rate (800 MHz).
SP{0/1}BSTBN[1:0]	I/O SBD	400 MHz	**Strand B N Strobes:** Negative phase data strobes for Strand B to transfer data at the 2x rate (800 MHz).
SP{0/1}BD[15:0]	I/O SBD	800 MHz	**Strand B Data Bus:** 16-bits of the data portion of a PHIT on Strand B. These bits are SSO encoded. SP{0/1}BSSO determines if these are out of an inverter or not.
SP{0/1}BEP[2:0]	I/O SBD	800 MHz	**Strand B Parity/ECC:** Two of these signals carry the ECC information for the data flits (BEP[1:0]). There are 4-bits of ECC for each data PHIT. The header flits are not ECC protected. The third signal is for parity (BEP[2]). Each PHIT is always protected by two bits of parity.
SP{0/1}BLLC	I/O SBD	800 MHz	**Strand B Link Layer Control:** For each PHIT these signals carry two of the four bits of link layer control information.
SP{0/1}BSSO	I/O SBD	800 MHz	**Strand B SSO Encode:** This signal is asserted to indicate that the data bits over Strand B are inverted.
SP{0/1}GPIO[1:0]	I/O CMOS 1.5 OD	ASYNC	**General Purpose I/O Signals:** These pins are asynchronous open drain I/O signals. To filter glitches on the inputs, the value of the input only changes when the same value has been sampled over four consecutive 200 MHz clock cycles. Similarly, to ensure accurate sampling of these signals by other devices, the output value will be asserted for a minimum of 6 consecutive 200 MHz cycles.
Vccsp	Analog	N/A	VCC for the SP.

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The Hub Interface 2.0 connects the SIOH to a maximum of four P64H2 PCI/PCI-X bridge components (refer to Table 2-2).

Table 2-2. Hub Interface 2.0 Signals

Signal Name	Type	Clock Domain	Description
HL{4/3/2/1}PD[17:0]	I/O iGTL	533 MHz	**Packet data signals:** PD[16] is connected to PD[20] on P64H2, and PD[17] is connected to PD[21] on P64H2.
HL{4/3/2/1}PSTRBF HL{4/3/2/1}PUSTRBF	I/O iGTL	533 MHz	**Hub Interface Strobe First:** HL{n}PSTRBF strobes are used for HL{n}PD[7:0] & HL{n}PD[16]. HL{n}PUSTRBF strobes are used for HL{n}PD[15:8] & HL{n}PD[17].
HL{4/3/2/1}PSTRBS HL{4/3/2/1}PUSTRBS	I/O iGTL	533 MHz	**Hub Interface Strobe Second:** HL{n}PSTRBS strobes are used for HL{n}PD[7:0] & HL{n}PD[16]. HL{n}PUSTRBS are the strobes used for HL{n}PD[15:8] & HL{n}PD[17].
HL{4/3/2/1}RQOUT	O iGTL	66 MHz	**Hub Interface Request Out:** This must be connected to HI[16] of the P64H2.
HL{4/3/2/1}RQIN	I iGTL	66 MHz	**Hub Interface Request In:** This must be connected to HI[17] of the P64H2.
HL{4/3/2/1}STOP	I/O iGTL	66 MHz	**Hub Interface Stop:** This must be connected to HI[18] of the P64H2.
HL{4/3/2/1}VSWING	I/O Analog	N/A	Hub Interface voltage swing.
HL{4/3/2/1}RCOMP	I/O iGTL	N/A	**Hub Interface Compensation:** Connects to the external RCOMP resistor and used for impedance matching.
HL{4/3/2/1}VREF	I Analog	N/A	Hub Interface voltage reference.

2.3 Hub Interface 1.5

The Hub Interface 1.5 connects the SIOH to the legacy I/O ICH4 component (refer to Table 2-3).

Table 2-3. Hub Interface 1.5 Signals

Signal Name	Type	Clock Domain	Description
HL0PD[7:0]#	I/O iGTL	266 MHz	Packet data pins.
HL0PSTRBS	I/O iGTL	266 MHz	Second PD Interface Strobe.
HL0PSTRBF	I/O iGTL	266 MHz	First PD Interface Strobe.
HL0RQOUT#	O iGTL	66 MHz	**Hub Interface Request Out:** This must be connected to HI[8] on ICH4.
HL0RQIN#	I iGTL	66 MHz	**Hub Interface Request In:** This must be connected to HI[9] on ICH4.
HL0STOP#	I/O iGTL	66 MHz	**Hub Interface Stop Signal:** This must be connected to HI[10] on ICH4.
HL0PAR#	I/O iGTL	66 MHz	**Hub Interface Parity Signal:** This must be connected to HI[11] on ICH4.

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Table 2-3. Hub Interface 1.5 Signals (Continued)

Signal Name	Type	Clock Domain	Description
HL0VREF[1:0]	I Analog	N/A	Hub Interface Voltage Reference.
HL0RCOMP	I/O iGTL	N/A	**Hub Interface Compensation:** Connects to the external RCOMP resistor and used for impedance matching.
HL0VSWING	I/O Analog	N/A	Hub Interface Voltage Swing.

2.4 Reset and Miscellaneous Signals

Table 2-4. Reset and Miscellaneous Signals

Signal Name	Type	Clock Domain	Description
RESETI#	I CMOS1.5	200 MHz	**Reset Input:** Reset input driven by the system.
RESET66#	O CMOS1.5	200 MHz	**Reset 66:** Reset signal output for the downstream I/O components. Synchronized to the SIOH reset input (RESETI#) signal.
PWRGOOD	I CMOS1.5	ASYNC	**Power Good:** Clears the SIOH. This signal is held low until all power supplies are within specification. This signal is followed by RESETI# Deassertion.
INT_OUT#	O CMOS 1.5 OD	ASYNC	**Interrupt Output:** SIOH interrupt output pin for SP Hot-Plug and performance. This pin is asynchronous and is driven for a minimum of six consecutive SYSCLKs before transitioning.
EV[3:0]#	I/O CMOS1.5 OD	ASYNC	**Event In/Out:** Open-drain event pins connected to the performance monitors. As inputs they are used in signal conditioning the PerfMon's trigger selection. As an output they indicate that the target condition has been met for a particular monitor. To filter glitches on the inputs, the value of the input only changes when the same value has been sampled over four consecutive 200 MHz clock cycles. Similarly, to ensure accurate sampling of these signals by other devices, these output value will be asserted for a minimum of twelve consecutive 200 MHz cycles.
ERR[2:0]#	I/O CMOS1.5 OD	ASYNC	**Error Out:** Open-drain error indicator pins to indicate the severity level of an error that has occurred internally or observed by this chip.
BUSID[2:0]	I CMOS1.5	N/A	**Bus Number Identification:** Static inputs to set the PCI equivalent of bus ID.
NODEID[4:0]	I CMOS1.5	N/A	**Device Node Identification:** Static inputs to set the PCI equivalent of device ID. NODEID[3:0] specifies the SMBus slave address for the component.

2.5 Clock Signals

The SIOH requires a 200 MHz LVHSTL clock source. The SIOH also generates 66 MHz and 33 MHz output clocks that can be used as source clocks by the downstream I/O components (refer to Table 2-5).

Table 2-5. Input and Output Clock Signals

Signal Name	Type	Clock Domain	Description
SYSCLK/SYSCLK#	I Differential	200 MHz	**System Clock:** Input clock source (and complement) to the SIOH.
DET	I CMOS1.5	N/A	**PLL Determinism Pin:** DET pin is strapped high to enable determinism in the E8870 chipset. If high, CLK33 and CLK66 references are reset on First Hard Reset Deassertion.
FBCLK66	I CMOS 3.3	66 MHz	**66 MHz Feedback Clock:** External 66 MHz PLL feedback input.
VREFFBCLK66	I Analog	66 MHz	**Voltage Reference for FBCLK66:** Reference voltage for the 66 MHz PLL feedback.
CLK66	O CMOS 3.3	66 MHz	**Clock 66:** 66 MHz clock for all I/O subsystem common clock signals.
CLK33	O CMOS 3.3	33 MHz	**Clock 33:** Can be used as 33 MHz clock for ICH4 PCI bus.
LVHSTLODTEN	I CMOS1.5	200 MHz	**LVHSTL On Die Termination Enable:** Enables the on die termination resistors for the LVHSTL input buffers used on clock inputs.
VccaCore	Analog	N/A	VCC for Core clock.
VssaCore	Analog	N/A	VSS for Core clock.
VCCASP	Analog	N/A	VCC for SP clock.
VSSASP	Analog	N/A	VSS for SP clock.
VCCAHL	Analog	N/A	VCC for HI clock.
VSSAHL	Analog	N/A	VSS for HI clock.
VCCACom	Analog	N/A	VCC for Common clock.
VSSACom	Analog	N/A	VSS for Common clock.
Vcc33	Analog	N/A	3.3 VCC for all HVCMOS drivers.

2.6　JTAG and SMBus Signals

Table 2-6. JTAG and SMBus Signals

Signal Name	Type	Clock Domain	Description
TCK	I JTAG	TCK	**JTAG Test Clock:** Clock input used to drive Test Access Port (TAP) state machine during test. TCK = 20 MHz max.
TDI	I JTAG	TCK	**JTAG Test Data In:** Data input for test mode, used to serially shift data and instructions into the TAP.
TDO	O JTAG	TCK	**JTAG Test Data Out:** Data output for test mode, used to serially shift data out of the TAP.
TMS	I JTAG	TCK	**JTAG Test Mode Select:** This signal is used to control the state of the TAP controller.
TRST#	I JTAG	ASYNC	**JTAG Test Reset:** This signal resets the TAP controller logic.
SCL	I/O SMBus OD	SCL	**SMBus Clock:** Provides synchronous operation of the SMBus.
SDA	I/O SMBus OD	SCL	**SMBus Addr/Data:** Used for data transfer and arbitration on the SMBus.

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Configuration Registers 3

The SIOH is viewed by the system as a single PCI device with seven different functions. While the standard PCI header is defined in the *PCI Local Bus Specification,* Revision 2.2, the remaining configuration registers typically reside above 40h.

3.1 Register Access Mechanisms

The SIOH configuration registers can be accessed from the following sources:

- Configuration Read/Write from Scalability Port (SP)
- System Management Bus (SMBus)
- JTAG

3.1.1 Scalability Port Initiated Register Access

SIOH will accept only one configuration access from the SPs at a time. Subsequent accesses experience back pressure until the previous configuration access is finished.

3.1.2 JTAG Initiated Register Access

The SIOH provides a JTAG configuration access mechanism that allows a user to access any register in the chipset. This is accomplished by using a mechanism similar to the PCI CF8/CFC data structure. The flow to read and write configuration space via JTAG is shown in Table 3-1 and Table 3-2.

Table 3-1. JTAG Read to Configuration Space

Field of Serial Chain	Bit#	Phase 1	Phase 2	Phase 3[1]
Data [31:0]	63:32			Read the data.
Register Number	31:24	Write with address to read.		
Device	23:19			
Function	18:16			
Bus Number	15:8			
Error	7			Read for proper termination.
Reserved	6:5			
Busy	4	Set to 1	Poll until cleared.	
Enable Access	3	Set to 1		
Byte Enable Command	2:0	Set command: • 100 - read dword Address must be dword aligned.		

1. Software could choose to merge Phase 2 and Phase 3 into one operation.

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Table 3-2. JTAG Write to Configuration Space

Field of Serial Chain	Bit#	Phase 1	Phase 2	Phase 3[1]
Data [31:0]	63:32	Write with data and address to write.		
Register Number	31:24			
Device	23:19			
Function	18:16			
Bus Number	15:8			
Error	7			Read for proper termination.
Reserved	6:5			
Busy	4	Set to 1	Poll until cleared.	
Enable Access	3	Set to 1		
Byte Enable Command	2:0	Set command: • 001 - write byte. • 010 - write word Address must be word aligned. • 011 - write dword Address must be dword aligned.		

1. Software could choose to merge Phase 2 and Phase 3 into one operation.

The bus, function, device, and register numbers are similar to the CF8 structure. This mechanism may be used in run-time and in the middle of any other traffic.

Note: The JTAG port on the SIOH can only be used to access its own configuration registers.

3.1.3 SMBus Operation

The SIOH allows a server management subsystem to read and write its configuration registers. This is accomplished through an "out-of-band", slave-only SMBus 2.0 port.

The SIOH claims address 11X0_XXX where XXXX specifies NODEID[3:0] pin strappings (sampled upon the deassertion of RESETI#).

Note: It is possible for software to change the default Node ID by programming the CBC register. This reprogramming will *not* affect the SMBus address assignment.

3.2 Device Mapping

The device number for each device connected to an SP is captured from pins upon the rising edge of hard reset. In the CBC register, Bus[2:0] is captured from the BUSID[2:0] pins. Bus[7:3] are assigned by software. Bus[7:0] are intended for truly large systems where the total # of devices on the cross-bar network may exceed the 32 device limit on a given PCI bus. Software must set Bus[7:0] to FF for the SIOH when using an SP switch.

Note: The compatibility bus must be programmed to Bus 0. Therefore, the SIOH Bus ID should never get assigned to 0 by software.

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In the CBC register, Node ID[4:0] are also captured from external pins on the Node ID[4:0] pins. Those bits are compared with the device number field in the PCI configuration access. The device number can be any value between 0 and 31. Software must set Node ID[4:3] to 11 in the E8870 chipset.

The SIOH has a PCI bus range per Hub Interface. Each Hub Interface is assigned a bus number (BUSNO[x]) and is accessed with Type 0 configuration cycles. Bus range BUSNO[x] +1 to BUSNO[x+1] of SIOH encompasses all PCI buses behind Hub Interface[x] and is accessed with Type 1 configuration cycles.

Table 3-3 describes how configuration cycles are routed by the SIOH.

Table 3-3. Outbound Configuration Cycle Routing

Configuration Cycle	Route
Bus[7:0] == Bus[7:0] (in CBC) AND Device[4:0] == Node ID[4:0]	Configuration cycle targets this SIOH so service it locally and return the completion to source.
Bus[7:0] == BUSNO[x][1]	Forward Type 0 configuration cycle to Hub Interface x.
BUSNO[x] < Bus[7:0] < BUSNO[x+1][1]	Forward Type 1 configuration cycle to Hub Interface x.
None of the above.	Master Abort.

1. This test is performed only if the first row tests false.

Even if a Hub Interface is unpopulated, it must be assigned to a bus number. Any configuration cycles to this bus number will Master Abort.

Table 3-4 maps the function assignments for the SIOH.

Table 3-4. SIOH Function Mapping

Function Number	SIOH Description
0	Hub Interface Port 0 registers (8-bit compatibility port).
1	Hub Interface Port 1 registers.
2	Hub Interface Port 2 registers.
3	Hub Interface Port 3 registers.
4	Hub Interface Port 4 registers.
5	General SIOH registers.
6	RAS registers.

3.3   Register Attributes

The Default column in the following register definitions (refer to Table 3-5) indicates the register will be set to this value after a hard reset. (Refer to Chapter 6, "Reset" for the definition of a hard reset.) Start-up BIOS software is responsible for setting all register values that is dependent on the particular platform. Each of the following registers uses the following conventions for the bit attribute column.

Table 3-5. Register Attributes Definitions

Attribute	Abbreviation	Description
Read Only	RO	The bit is set by the hardware only and software can only read the bit. Writes to the register have no effect. A hard reset will set the bit to its default value.
Read/Write	RW	The bit can be read and written by software. A hard reset will set the bit to its default value.
Read/Write Once	RWO	The bit can be read by software. It can also be written by software but the hardware prevents writing it more than once without a prior hard reset. This protection applies on a bit-by-bit basis, e.g. if the RWO field is two bytes and only one byte is written, then the written byte cannot be rewritten (unless reset). However, the unwritten byte can still be written once.
Read/Clear	RC	The bit can be either read or cleared by software. In order to clear an RC bit, the software must write a one to it. Writing a zero to an RC bit will have no effect. A hard reset will set the bit to its default value.
Sticky	RWS, RCS, ROS	The bit is "sticky" or unchanged by a hard reset. Read/Write, Read/Clear, and Read Only bits may be sticky. Refer to Chapter 6, "Reset" for the definition of a hard reset. These bits are only reset with PWRGOOD.
Reserved	RV	This bit is reserved for future expansion and must not be written. The *PCI Local Bus Specification,* Revision 2.3 requires that reserved bits must be preserved. Any software that modifies a register that contains a reserved bit is responsible for reading the register, modifying the desired bits, and writing back the result.

3.4   Vendor ID Register (VID)

These registers latch Syndrome and ECC information for the first non-fatal error detected inside the SPL cluster. Not all errors have logs.

Device: Node_ID
Function: 0, 1, 2, 3, 4, 5, 6
Offset: 00h

Bit	Attr	Default	Description
15:0	RO	8086h	**Vendor Identification Number**: This is the standard 16-bit value assigned to Intel.

3.5 Device ID Register (DID)

The Device ID (DID) register identifies the SIOH component and adheres to the *PCI Local Bus Specification,* Revision 2.2. Since this register is part of the standard PCI header, there is a DID register per PCI function.

Device: **Node_ID**
Function: **0, 1, 2, 3, 4, 5, 6**
Offset: **02h**

Bit	Attr	Default	Description
15:0	RO	F0 - 0510h F1 - 0511h F2 - 0512h F3 - 0513h F4 - 0514h F5 - 0515h F6 - 0516h	**Device Identification Number**: This value is the device ID for the SIOH component. In order for proper driver functionality, each SIOH function has a different value for the DID register. (Fn = function n).

3.6 PCI Command Registers (PCICMD)

The PCI Command (PCICMD) registers follow a subset of the *PCI Local Bus Specification,* Revision 2.2. These registers provide the basic control for the SIOH to initiate and respond to Hub Interface cycles and maintain compatibility with PCI configuration space. Since these registers are part of the standard PCI header, there is a PCICMD register per PCI function.

Device: **Node_ID**
Function: **0, 1, 2, 3, 4**
Offset: **04h**

Bit	Attr	Default	Description
15:9	RV	0	*Reserved.*
8	RO	0	**SERR# Enable:** The SIOH never issues a DO_SERR special cycle.
7	RV	0	*Reserved.*
6	RW	0	**Parity Error Response (IERRE):** Controls the SIOH response when a parity error (on function 0) or multi-bit ECC error is detected on the Hub Interface. This bit only controls the detection in PCISTS[15] and PCISTS[8]. The SIOH reports all parity errors on the Hub Interface. Refer to Section 3.47, "First Error Status Registers (FERRST)" for details on parity error reporting.
5:4	RV	0	*Reserved.*
3	RO	0	**Special Cycle Enable:** Controls the ability to forward PCI-type (legacy) special cycles. Devices on the Hub Interface are not capable of accepting legacy special cycles. This bit does not apply to Hub Interface specific special cycles.
2	RO	1	**Bus Master Enable:** Controls the ability for the SIOH to initiate Hub Interface cycles. The SIOH can always issue Hub Interface bus cycles.
1	RO	1	**Memory Access Enable:** Controls the ability for the SIOH to respond to memory transactions initiated on the Hub Interface. The SIOH can always accept memory transactions.
0	RO	0	**I/O Access Enable:** Controls the ability for the SIOH to respond to I/O transactions initiated on the Hub Interface. The E8870 chipset does not support inbound I/O cycles.

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3.7 PCI Status Registers (PCISTS)

The PCI Status (PCISTS) registers follow a subset of the *PCI Local Bus Specification,* Revision 2.2. These registers provide the basic status of this device in response to Hub Interface cycles and maintain compatibility with PCI configuration space. Since these registers are part of the standard PCI header, there is a PCISTS register per PCI function.

Device: Node_ID
Function: 0, 1, 2, 3, 4
Offset: 06h

Bit	Attr	Default	Description
15	RC	0	**Detected Integrity Error:** This bit indicates different conditions for SIOH function 0 versus functions 1 - 4. For function 0, this bit indicates that a parity error was observed on the Hub Interface. This bit is not affected by the state of PCICMD[6]. For functions 1 -4, this bit indicates that a multi-bit ECC error was detected on the Hub Interface. If PCICMD[6] is enabled, single-bit errors will also set this bit.
14	RO	0	**Signalled System Error:** This bit indicates if a system error special cycle (DO_SERR) is initiated by the SIOH component. This bit should never be asserted since the SIOH never initiates DO_SERR.
13	RC	0	**Received Master Abort Status:** This bit indicates if the SIOH receives a Master Abort completion cycle or an unimplemented Special Cycle command.
12	RC	0	**Received Target Abort Status:** This bit indicates if the SIOH receives a Target Abort completion cycle in response to an SIOH-initiated Hub Interface cycle.
11	RC	0	**Signalled Target Abort Status:** The SIOH sets this bit when it issues a Target Abort completion cycle to the Hub Interface agent.
10:9	RV	0	*Reserved.*
8	RC	0	**Master Data Integrity Error:** This bit indicates that a *data* parity or multi-bit ECC error was detected on the Hub Interface. This bit is set when all of the following conditions are met: • The SIOH detected a data parity (function 0) or multi-bit ECC error on data (functions 1 - 4) for an outbound read completion. • PCICMD[6] is set to 1.
7:0	RV	00h	*Reserved.*

3.8 Revision ID Register (RID)

The Revision ID (RID) register tracks the specific revision of this component. Since this register is part of the standard PCI header, there is one RID register per PCI function.

Device: Node_ID
Function: 0, 1, 2, 3, 4, 5, 6
Offset: 08h

Bit	Attr	Default	Description
7:0	RO	XXh	**Revision Identification Number:** 20H = C0 stepping of the SIOH 21H = C1 stepping of the SIOH

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3.9 Class Code Registers (CCR)

The Class Code (CCR) registers identify the SIOH component as a host bridge. These registers adhere to the *PCI Local Bus Specification,* Revision 2.2. Since these registers are part of the standard PCI header, there is a CCR register per PCI function.

Device: **Node_ID**
Function: **0, 1, 2, 3, 4, 5, 6**
Offset: **09h**

Bit	Attr	Default	Description
23:16	RO	06h	**Base Class Code:** This code indicates that the SIOH is a bridge device.
15:8	RO	00h	**Sub-Class Code:** This code indicates that the SIOH bridge is part of a host bridge.
7:0	RO	00h	**Register-Level Programming Interface:** This field identifies a specific programming interface that device independent software can use to interact with the device. There are no such interfaces defined for host bridges.

3.10 Header Type Registers (HDR)

The SIOH follows the standard PCI Configuration space header format and maintains seven functions. The Header-Type Registers (HDR) adhere to the *PCI Local Bus Specification,* Revision 2.2. Since these registers are part of the standard PCI header, there is an HDR register per PCI function.

Device: **Node_ID**
Function: **0, 1, 2, 3, 4, 5, 6**
Offset: **0Eh**

Bit	Attr	Default	Description
7	RO	1	**Multi-Function Device:** This bit indicates if the SIOH is a multi-function device. The SIOH is a multi-function device.
6:0	RO	00h	**Configuration Layout:** This field identifies the format of the standard PCI configuration header space. A value of zero indicates that it follows the standard PCI model.

3.11 Subsystem Vendor ID Register (SVID)

The Subsystem Vendor ID (SVID) register identifies the SIOH component and adheres to the *PCI Local Bus Specification,* Revision 2.2. Since this register is part of the standard PCI header, there is a SVID register per PCI function.

Device: **Node_ID**
Function: **0, 1, 2, 3, 4, 5, 6**
Offset: **2Ch**

Bit	Attr	Default	Description
15:0	RWO	8086h	**Subsystem Vendor Identification Number:** This value is the subsystem vendor ID for the SIOH component. The value can only be assigned once after reset.

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3.12 Subsystem ID Register (SID)

The Subsystem ID (SID) register adheres to the *PCI Local Bus Specification,* Revision 2.2. Since this register is part of the standard PCI header, there is a SID register per PCI function.

Device: **Node_ID**
Function: **0, 1, 2, 3, 4, 5, 6**
Offset: **2Eh**

Bit	Attr	Default	Description
15:0	RWO	8086h	**Subsystem Identification Number:** This value is the subsystem ID for the SIOH component. The value can only be assigned once after reset.

3.13 Hub Interface Control Registers (HLCTL)

These registers specify certain behavior for each Hub Interface. There is one register per interface.

Device: **Node_ID**
Function: **0, 1, 2, 3, 4**
Offset: **40h**

Bit	Attr	Default	Description
15:11	RV	0	*Reserved.*
10:9	RW	0	**Inactivity Timer:** These bits program the upper two bits of the Hub Interface cluster's inactivity timer. This 10-bit timer counts 200 MHz clocks and is used to determine when inbound read stream structures are active or inactive. 00 - 1.28 us 01 - 2.56 us 10 - 3.84 us 11 - 5.12 us
8	RO	See Description	**Hub Interface Presence:** Device detection is done via Hub Interface REQ# line. For function 0, presence is determined with a successful reset handshake. 0 = No device is connected on this Hub Interface 1 = A device is connected on this Hub Interface The default state of this bit depends on whether a component is present on the other end of the Hub Interface. If this interface detects that no component is present, the default state of this bit will be zero. If a component is present, the bit defaults to one.
7:6	RW	0	**Outstanding Completion-Required Requests:** This bit enables the number of outbound requests that require a completion the SIOH will attempt to the Hub Interface target. Such transactions include outbound read requests, outbound I/O reads and writes, and outbound configuration reads and writes. The SIOH can support up to four. The P64H2 can support four, and the ICH4 can support one. Programming this field correctly optimizes the Hub Interface bandwidth by matching the capabilities of the interfacing component. 00 - Only one outbound delayed request attempted on this Hub Interface port at a time. 01 - Two outbound delayed requests can be attempted simultaneously on this Hub Interface port. 10 - *Reserved* 11 - Four outbound delayed requests can be attempted simultaneously on this Hub Interface port. Each Hub Interface cluster can always accept four outbound delayed requests from the SP cluster. This register only specifies how many of those four the SIOH will attempt before waiting for the completion to return from the I/O bridge.

Device: Node_ID
Function: 0, 1, 2, 3, 4
Offset: 40h (Continued)

Bit	Attr	Default	Description
5	RW	0	**Read Streaming Disable:** This bit disables the SIOH ability to use the Hub Interface 2.0 read streaming feature.
			For function 0, Read Streaming is not a supported feature and this bit is always read as zero.
4	RW	0	**ECC/Parity Check Enable:** This bit enables the ECC checking/correction logic for the Hub Interface 2.0 ports and the parity checking logic for function 0. When this bit is cleared, any ECC or parity errors detected on the Hub Interface are not reported or corrected and do not affect the routing of the packet (e.g. dropping errors on header).
			This bit should be enabled after the ECC/parity generation logic is enabled on the Hub Interface component.
			This bit does not affect the SIOH's ECC/Parity generation logic.
3	RW	0	**Serial PipeID Enable:** The SIOH issues outbound read requests with different PipeIDs. Setting this bit forces the SIOH to issue all outbound reads and writes with the same PipeID of 0.
2	RWS	See Description	**Disable Hub Interface:** When set, this bit tri-states the corresponding Hub Interface outputs and masks the Hub Interface's inputs. Any internal transactions that are routed to the disabled interfaces will be master-aborted.
			The default state of this bit depends on whether a component is present on the other end of the Hub Interface (see HLCTL[8]). If this interface detects that a component is present, the default state of this bit will be zero. If no component is present, the bit defaults to one. Hardware does not protect against enabling an interface that does not have an interfacing component.
1	RW	0	**Read Cache Disable:** This bit disables the read cache for the Hub Interface.
			If the read caches are disabled, prefetching should also be disabled. Otherwise, the SIOH will prefetch data it will never deliver from the cache. If the read caches are disabled and the port interfaces a P64H2, restreaming also needs to be disabled in the P64H2.
0	RW	0	**Prefetch Disable:** This bit disables read prefetching for the Hub Interface port. If disabled, inbound reads initiated on the Hub Interface port will request only the line requested and no more.

3.14   Hub Interface Command Control Registers (HLCMD)

The Hub Interface Command/Control (HLCMD) registers specify the basic functionality of the SIOH on each Hub Interface.

Device: Node_ID
Function: 0, 1, 2, 3, 4
Offset: 44h

Bit	Attr	Default	Description
31:29	RO	0	**HUB_SUB_FIRST:** This field stores the lowest subordinate Hub Interface hub number. This information is compared with the Hub ID to determine whether a completion packet should be forwarded further down the Hub Interface hierarchy.
			This field is not applicable for components other than a Hub Interface-to-Hub Interface bridge.
28	RV	0	*Reserved.*

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Device: Node_ID
Function: 0, 1, 2, 3, 4
Offset: 44h (Continued)

Bit	Attr	Default	Description
27:25	RO	0	**HUB_SUB_LAST:** This field stores the highest subordinate Hub Interface hub number. This information is compared with the Hub ID to determine whether a completion packet should be forwarded further down the Hub Interface hierarchy. *This field is not applicable for components other than a Hub Interface-to-Hub Interface bridge.*
24	RV	0	*Reserved.*
23:21	RO	0	**HUB_ID:** This field identifies the Hub Interface ID number for the SIOH. The SIOH uses this field to determine when to accept a Hub Interface request packet and send any corresponding completion packets. *This field is not applicable for components other than a Hub Interface-to-Hub Interface bridge.*
20	RV	0	*Reserved.*
19:16	RW	0	**HL_TIMESLICE:** This field sets the Hub Interface arbiter timeslice value with four base-clock granularity. A value of zero means that the timer immediately expires and the SIOH will allow the agent interfacing Hub Interface access to the bus every other transaction.
15:14	RO	0	**HL_WIDTH:** This field sets the Hub Interface data bus width. A value of 01 indicates a 16-bit data bus and 00 indicates an 8-bit data bus. This field only applies for function 0. For functions 1 - 4 of the SIOH (Hub Interface 2.0 ports) this field is reserved and always returns 00.
13	RO	1 (0)	**HL_RATE_VALID:** This bit is sampled by software and indicates when the Hub Interface bus rate is valid. This bit is cleared when the Hub Interface bus rate is being changed. This field only applies for function 0. For functions 1 - 4 of the SIOH (Hub Interface 2.0 ports) this field is reserved and always returns 0.
12:10	RO	010 (000)	**HL_RATE:** This field indicates the Hub Interface data rate. Function 0 supports a 4x data rate encoded with 010. This field only applies for function 0. For functions 1 - 4 of the SIOH (Hub Interface 2.0 ports) this field is reserved and always returns 000.
9:4	RV	00h	*Reserved.*
3:1	RW	111	**MAX_DATA:** This field is programmed with the longest data stream the SIOH is permitted to send on the Hub Interface. MAX_DATA applies to both write request cycles and read completion cycles. 000 = 32-bytes 001 = 64-bytes 01X = 128-bytes 1XX = 256-bytes If software attempts to program HLCMD[3:1] to 000 for functions 1 to 4, any subsequent reads will return 001 indicating 64-bytes.
0	RV	0	*Reserved.*

3.15   Hub Interface Recoverable Error Control Registers (RECHUB)

These registers latch control information for the first non-fatal error detected inside the Hub Interface cluster. Not all errors have logs.

This is the bit mapping for Hub Interface *Requests* (RECHUB[31] = 0).

Device: Node_ID
Function: 0, 1, 2, 3, 4
Offset: 4Ch

Bit	Attr	Default	Description
127:120	ROS (RV)	0	**Hub Interface header ECC (Upper):** This ECC code covers Header [127:64]. For function 0, this field is reserved.
119:112	ROS	0	**Hub Interface header ECC (Lower):** This ECC code covers Header [63:0]. For function 0, this field is reserved except for the following bits: 114:112, which records the parity bits when AF=1 and EA = 1 (3D-word header). 113:112, which records the parity bits when AF=1 and EA = 0 (2 D-word header). 112, which records the parity bit when AF = 0 and EA = 0 (1 D-word header).
111:99	ROS	0	**Prefetch Horizon[1].**
98	ROS	0	**Reserved Field of the packet.**
97:96	ROS	0	**Elen[1]:** Extended Length.
95:64	ROS	0	**Addr[63:32][1]:** Address bits 63:32 of the address. The SIOH does not support all upper address bits. If the SIOH detects an inbound illegal address error because one or more of these bits are set, then Addr[63] will be set and Addr[62:32] will be zero.
63:34	ROS	0	**Addr[31:2][2]:** Address bits 31:2 of the address.
33	ROS	0	**EH:** Extended Header.
32	ROS	0	**EA/CT:** Extended Address/Configuration type.
31	ROS	0	**Rq/Cp:** Request/completion field.
30	ROS	0	**R/W:** Read/Write field.
29	ROS	0	**CR:** Completion required field.
28	ROS	0	**AF:** Address format.
27	ROS	0	**LK:** Lock cycle.
26:21	ROS	0	**TD Routing:** Transaction Description routing field.
20	ROS	0	**Reserved Field on the packet.**
19:16	ROS	0	**TD Attribute:** Transaction Descriptor Attribute.
15:14	ROS	0	**Space:** Address space.
13:8	ROS	0	**Data Length:** D-word data length.
7:0	ROS	0	**Byte Enables:** 7:4 is the Last D-word Byte Enables and 3:0 is the First Byte Enables. **Special Cycle Encoding**: When Space field indicates a Special Cycle.

1. For Special Cycles, RECHUB[111:64] does not use this encoding and should be padded with zeroes by the initiator.
2. For Special Cycles, RECHUB[63:31] might have data if required by the Special Cycle. Otherwise, it should be padded with zeroes by the initiator.

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This is the bit mapping for Hub Interface *Completions* (RECHUB[31] = 1).

Device: **Node_ID**
Function: **0, 1, 2, 3, 4**
Offset: **4Ch**

Bit	Attr	Default	Description
127:120	ROS (RV)	0	**Hub interface header ECC (Upper):** This ECC code covers Header[128:64]. For function 0, this field is reserved.
119:112	ROS	0	**Hub interface Header ECC (Lower):** This ECC code covers Header[63:0]. For function 0, this field is reserved except for bit 112, which records the parity bit.
111:32	ROS	0	**Reserved Field on the packet.**
31	ROS	0	**Rq/Cp:** Request/completion field.
30	ROS	0	**R/W:** Read/Write field.
29:28	ROS	0	**Reserved Field of the packet.**
27	ROS	0	**LK:** Lock cycle.
26:21	ROS	0	**TD Routing:** Transaction Description routing field.
20	ROS	0	**Reserved Field on the packet.**
19:16	ROS	0	**TD Attribute:** Transaction Descriptor Attribute.
15:14	ROS	0	**Space:** Address space.
13:8	ROS	0	**Data Length:** D-word data length.
7:0	ROS	0	**Completion Status:** Indicates the status of the request.

3.16 Hub Interface Recoverable Error Data Registers (REDHUB)

This register latches data information for the first non-fatal error detected inside the Hub Interface cluster. Not all errors have logs.

Device: **Node_ID**
Function: **0, 1, 2, 3, 4**
Offset: **5Ch**

Bit	Attr	Default	Description
95:72	RV	0	*Reserved.*
71:64	ROS	0	**ECC/Parity Field:** For inbound functions 1 - 4, there are eight bits of ECC per 64 bits of data. For function 0, there is one parity bit per 32 bits of data.
63:0	ROS	0	**Data Field.**

3.17 Hub Interface Non-Recoverable Error Control Register (NRECHUB)

This register latches data information for the first non-fatal error detected inside the Hub Interface cluster. Not all errors have logs.

Device: Node_ID
Function: 0, 1, 2, 3, 4
Offset: 68h

Bit	Attr	Default	Description
127:0	ROS	0	**Hub Interface Header or Internal Request/Response Header:** See the RECHUB register for contents.

3.18 Hub Interface ECC Mask Register (HECCMSK)

This register is used to force an ECC error (parity for function 0) affecting only data packets flowing into the SIOH (inbound writes and outbound read completions). After this register is written with a masking function, all subsequent *inbound* Hub Interface data packets will generate a masked version of the ECC code. To disable testing, the mask value is left at 0h (the default). The mask is bit-wise XOR with the received ECC.

Note: Even if ECC checking is disabled with the HLCTL register, this mask is still applied.

For function 0 (HI1.5), only parity is supported and only HECCMSK[0] applies. This bit acts as a mask for the parity bit affecting only data packets flowing into the SIOH (inbound writes and outbound read completions). The mask is bit-wise XOR with the received parity bit.

Device: Node_ID
Function: 0, 1, 2, 3, 4
Offset: 84H

Bit	Attr	Default	Description
7:0	RW	00h	**ECC/Parity Mask:** For 64 bits of data. For function 0, bit 0 acts as a mask for the parity bit.

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3.19 Hub Interface Performance Monitor Response and Control Registers (HL_PMR[1:0])

The Performance Monitor Response (PMR) registers control operation of their associated counter, and provide overflow or max compare status information.

Device: Node_ID
Function: 1, 2, 3, 4
Offset: 8Ch (HL_PMR[0]), 90h (HL_PMR[1])

Bit	Attr	Default	Description
31:25	RV	0	*Reserved.*
24	RW	0	**Event Register Select:** The PME_LO & PME_HI registers select events based on the Hub Interface header fields. The PME_RSC register selects resource specific events that are mutually exclusive of the Hub Interface header events. One or the other of the event sets can be selected. 0 = Hub Interface events (PME_LO, PME_HI). 1 = Hub Interface resources (PME_RSC).
23:22	RW	0	**Compare Mode:** This field defines how the PMCMP (compare) register is to be used. 00 - Compare mode disabled (PMCMP register not used). 01 - Max compare only: The PMCMP register value is compared with the counter value. If the counter value is greater, the Count Compare Status (bit 13) of the "Event Status" field of this register will be set. 10 - Max compare with update of PMCMP at end of sample: The PMCMP register value is compared with the counter value, and if the counter value is greater, the PMCMP register is updated with the counter value. Note, the Event Status field is not affected in this mode. 11 - Address compare mode where the PMCMP register is compared with the address field. Counter 0 of a counter pair will compare on an address greater than the register, and counter 1 will compare on an address equal to or lesser than the register (inverse of greater than). When both comparisons are valid, an address range comparison qualification is generated. This mode will cause the address range comparison to be AND'ed with the event qualification specified in the selected PME register of each counter. The Event Status field is not affected in this mode. The address comparison range is A[38:7].
21:19	RW	0	**Reset Event Select:** Counter and event status will reset and counting will continue. 000 - No reset condition. 001 - Partner event status: When the partner counter causes an event status condition to be activated, either by a counter overflow or max comparison, then this counter will reset and continue counting. 010 - Partner PME register event: When the partner counter detects a match condition that meets its selected PME register qualifications, then this counter will reset and continue counting. 011 - *Reserved* 100 - EV0 pin 101 - EV1 pin 110 - EV2 pin 111 - EV3 pin

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Device: Node_ID
Function: 1, 2, 3, 4
Offset: 8Ch (HL_PMR[0]), 90h (HL_PMR[1]) (Continued)

Bit	Attr	Default	Description
18:16	RW	0	**Count Event Select:** This field determines the counter enable source. 000 - PME register event. 001 - Partner event status (max compare or overflow). 010 - All clocks when enabled. 011 - *Reserved* 100 - EV0 pin 101 - EV1 pin 110 - EV2 pin 111 - EV3 pin
15:14	RW	0	**Count Mode:** 00 - Count event selected by **Count Event Select** field. 01 - Count clocks after event selected by **Count Event Select** field. 10 - Count transaction length of event selected by **Count Event Select** field. 11 - *Reserved*
13:12	RW	0	**Event Status:** This status bit captures an overflow or count compare event. The Event Status Output field can be programmed to allow this bit to be driven to an external EV pin. x1 - Overflow -The PMD counter overflow status. 1x - Count compare - PMD counter greater than PMCMP register when in compare mode. This bit is sticky in that once an event is reported the status remains even though the original condition is no longer valid. This bit can be cleared by software or by starting a sample. Event status is always visible in the PERFCON register, except if "Event Status Output" field is in cascade mode. If in address compare mode (compare mode = 11), the count compare bit is not activated.
11:9	RW	0	**Event Status Output:** This field selects which pin to report event status, or an address compare if in address compare mode (compare mode = 11). 000 - Event status reported only in PERFCON register. 001 - Event status (overflow) reported to partner only. Used for cascading event counters. 100 - Event status or address comparison in PERFCON and on EV0 pin. 101 - Event status or address comparison in PERFCON and on EV1 pin. 110 - Event status or address comparison in PERFCON and on EV2 pin. 111 - Event status or address comparison in PERFCON and on EV3 pin.

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Device: Node_ID
Function: 1, 2, 3, 4
Offset: 8Ch (HL_PMR[0]), 90h (HL_PMR[1]) (Continued)

Bit	Attr	Default	Description
8:5	RW	0	**CD_Src:** Counter disable source. These bits control which input disables the counter. Note, if the **enable source** is inactive, counting is also disabled. 1xxx - EV3 pin x1xx - EV2 pin xx1x - EV1 pin xxx1 - EV0 pin
4:2	RW	0	**CE_Src:** Counter enable source. These bits identify which input enables the counter. Default value disables counting. 000 - Disabled. 001 - PERFCON **local_count_enable** field. 010 - Partner event status (max compare, overflow, or cascade). 011 - *Reserved* 100 - EV0 pin 101 - EV1 pin 110 - EV2 pin 111 - EV3 pin
1	RW	0	**Clear Overflow:** This bit clears the overflow bit in the associated PMD counter. The counters continue counting. This bit is cleared by hardware when the operation is complete.
0	RW	0	**Reset:** Setting this bit to a one sets all registers associated with this counter to the default state. It does not change this PMR register since any desired value can be loaded while setting the Reset bit. This Reset bit will clear itself after the reset is completed. For diagnostic purposes, the contents of the other registers can be read to verify operation of this bit. There is also a reset bit in the PERFCON register that clears all counter registers including the PMR.

3.20 Hub Interface Performance Monitor Event Registers – Low (HL_PME_LO[1:0])

Selections in these registers correspond to fields within the Hub Interface packet header. Each field selection is AND'ed with all other fields in these registers and the HL_PME_HI registers. These registers are selected for match decoding via the Event Register Select field in the PMR registers.

Device: Node_ID
Function: 1, 2, 3, 4
Offset: 94h (HL_PME_LO[0]), 98h (HL_PME_LO[1])

Bit	Attr	Default	Description
31	RW	0	**Incoming/Outgoing:** 0 = Incoming (from PCI bus).
30:29	RW	0	**Request/Completion Packet:** 00 - Request packet 01 - Completion packet 1x - Either

Device: Node_ID
Function: 1, 2, 3, 4
Offset: 94h (HL_PME_LO[0]), 98h (HL_PME_LO[1]) (Continued)

Bit	Attr	Default	Description
28:27	RW	0	**Write/Read:** 00 - Read 01 - Write 1x - Either read or write
26:25	RW	0	**Completion Required:** (Request packet only) 00 - No completion required 01 - Completion required 1x - Either
24:23	RW	0	**Lock:** 00 - No lock 01 - Lock 1x - Either
22:20	RW	0	**TD Attributes:** 0xx - Any attribute 100 - Asynchronous and snoop required 101 - Isochronous and snoop required 110 - Asynchronous and no snoop required 111 - Isochronous and no snoop required
19:18	RW	0	**Configuration Type:** (If Config Cycle Space selected) 00 - Type 0 01 - Type 1 1x - either type
17:16	RW	0	**Prefetch:** Extended header bit set in packet header and horizon field non-zero 00 - Non prefetch 01 - Prefetch 1x - Either
15:12	RW	0	**Space:** (OR'ed group) xxx1- Memory xx1x - IO x1xx - Configuration 1xxx - Special Cycles
11:8	RW	0	**Data Length:** 0xxx - Any length 1000 - 8-bytes or less 1001 - 16 bytes 1010 - 32-bytes 1011 - 64-bytes 1100 - 128-bytes 1101 - 256-bytes 1110 - 512-bytes 1111 - 1K bytes
7:0	RW	0	**Completion Status** (for Completion Packet) **or Special Cycle Encoding** (for Request Packet): 00h - Any completion status or special cycle.

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3.21 Hub Interface Performance Monitor Event Registers – High (HL_PME_HI[1:0])

These registers are an extension of the HL_PME_LO register. Each field selection is AND'ed with all other fields in these registers and the HL_PME_LO registers. Note that inbound retry events are AND'ed with all other match conditions. These registers are selected for match decoding via the Event Register Select field in the PMR registers.

Device: Node_ID
Function: 1, 2, 3, 4
Offset: 9Ch (HL_PME_HI[0]), A0h (HL_PME_HI[1])

Bit	Attr	Default	Description
31:14	RV	0	*Reserved.*
13:12	RW	0	**Retry:** For inbound transactions this field is AND'ed with match from all other fields, and for outbound transactions this field OR'ed with match from all other fields. Inbound vs. outbound transaction selected in bit 31 of HL_PME_LO register. 00 - All transactions selected, both retried and non-retried. x1 - Complete retry (entire inbound or outbound packet retried). 1x - Partial retry (part of packet retried - only for outbound transactions).
11:0	RW	0	**Routing and Mask:** "xxxxxxmmmmmm" - where x is the routing value field and m is the bit mask for each individual bit in the routing field ('1' is mask,'0' is select).

3.22 Hub Interface Performance Monitor Resource Event Registers (HL_PME_RSC[1:0])

These registers contain resource selections that are mutually exclusive to the event selections. These selections are not qualified by the event selections. Each individual field selection is OR'ed with the other fields to generate the counter match condition. This register is selected via the Event Register Select Field in the PMR registers.

Device: Node_ID
Function: 1, 2, 3, 4
Offset: A4h (HL_PME_RSC[0]), A8h (HL_PME_RSC[1])

Bit	Attr	Default	Description
31:2	RV	0	*Reserved.*
1:0	RW	0	**Read Cache:** 00 - Disable count 01 - Hit 10 - Miss 11 - Invalidate

3.23 Hub Interface Performance Monitor Data Registers (HL_PMD[1:0])

These registers are the counter value. The overflow bit can be cleared via the PMR registers without perturbing the value of the counter. This counter is reset at the beginning of a sample period unless it has been preloaded since a prior sample.

Device: Node_ID
Function: 1, 2, 3, 4
Offset: ACh (HL_PMD[0]), B0h (HL_PMD[1])

Bit	Attr	Default	Description
31	RW	0	**Overflow.**
30:0	RW	0	**Current counter value.**

3.24 Hub Interface Performance Monitor Compare Register (HL_PMCMP[1:0])

The compare register can be used three ways as selected in the "Compare Mode" field of the PMR register. First, when PMD is incremented, the value of PMD is compared to the value of PMCMP. If PMD is greater than PMCMP, this status is reflected in the PERFCON register and/or on EV pins as selected in the "Event Status Output" field of the PMR register. Secondly, update the PMCMP register with the value of PMD if the PMD register exceeds the contents of PMCMP.

The third mode is an address comparison mode. PMD0 compares on addresses greater than the PMCMP0 register, and PMD1 compares on addresses less than or equal to PMCMP1. The "AND" of these two comparisons is the address range comparison and it qualifies the other match event conditions for both counters. Note that the contents of PMCMP are compared to A[38:7].

Device: Node_ID
Function: 1, 2, 3, 4
Offset: B4h (HL_PMCMP[0]), B8h (HL_PMCMP[1])

Bit	Attr	Default	Description
31:0	RW	FFFF_FFFFh	**Counter compare value.**

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3.25   SIOH Control Registers (IOCTL)

The SIOH Control Registers specify the basic functionality of the SIOH feature set.

Device: **Node_ID**
Function: 5
Offset: 40h

Bit	Attr	Default	Description
15	RW	0	**MDA Enable:** This bit specifies whether or not a monochrome adapter card resides on the platform. If enabled, then any inbound writes that target B_000 to B_7FFF in legacy DOS space will get automatically routed to the compatibility bus. The monochrome adapter card (if one exists) must reside on the compatibility bus.
14:12	RV	0	*Reserved.*
11	RW	0	**Multi-Node Enable:** The SIOH has slightly different behavior when in a single-node configuration: 0 = Single node configuration. 1 = Multi-node configuration. In a single-node configuration, PCLR commands are never issued and Lock/PHOLD handling is different.
10	RW	1	**Compatibility Bus Enable:** This bit identifies if this SIOH interfaces the compatibility bus (ICH4 component). All reads or writes to the compatibility space will be routed to the 8-bit Hub Interface 1.5 port (Hub Interface port 0) if this bit is set (see Section 4.1.4, "Compatibility Bus"). 0 = The compatibility bus does not interface this SIOH component. 1 = The compatibility bus interfaces this SIOH component (on Hub Interface port 0).
9:7	RW	000	**VGA Port:** This bit field identifies which Hub Interface port interfaces the VGA device for the system. All reads or writes to the legacy VGA space will be routed to the Hub Interface port specified with this field (see Section 4.1.5, "VGA Space"). 000 = Hub Interface Port 0 (compatibility port) 001 = Hub Interface Port 1 010 = Hub Interface Port 2 011 = Hub Interface Port 3 100 = Hub Interface Port 4 101 = On Remote SIOH (forward inbound VGA accesses to SP with VGA attribute) 11x = Not on *any* SIOH (forward inbound VGA accesses to SP with DRAM attribute)
6	RW	0	**Write Cache Flush:** Setting this bit causes the SIOH to evict all write cache lines which are in Modified state. When the SIOH evicts all the Modified lines, this bit is cleared by the hardware. Software can poll this bit after setting it to know when the flush operation is complete.
5	RV	0	*Reserved.*
4	RW	0	**ICH Destination ID Copy Disable**: For interrupts issued by the ICH4, the SIOH copies address bits [19:15] to address bits [8:4]. Setting this bit disables that functionality.
3	RV	0	*Reserved.*
2	RW	0	**Default SP:** 0 = SP0 is selected as the default SP. 1 = SP1 is selected as the default SP.
1:0	RV	00	*Reserved.*

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3.26 System Reset Register (SYRE)

This register allows system software to reset the SIOH component.

Device: Node_ID
Function: 5
Offset: 42h

Bit	Attr	Default	Description
7:2	RV	0	*Reserved.*
1	RW	0	**Boot Flag Reset**: The rising edge of this bit will reset the boot flag register (BOFL) back to the default value.
0	RW	0	**SIOH Reset:** The rising edge on this bit will reset the entire SIOH. A reset sequence is initiated. This bit is used to reset the SIOH and asserts RESET66# during an SP Hot-Plug event.

3.27 Memory-Mapped I/O Base Low Address Register (MMIOBL)

The MMIOBL register with the MMIOLL register specifies one of the two address ranges allocated for Hub Interface-destined transactions. MMIOBL and MMIOLL are intended to specify a memory-mapped I/O window below the 4 GB boundary. The transaction address is compared against the base field for proper disposition. (Refer to Table 4-1 for how this register is decoded.)

For comparison purposes, address bits 23:0 are ignored and 43:32 must be zero.

Device: Node_ID
Function: 5
Offset: 44h

Bit	Attr	Default	Description
7:0	RW	00h	**Memory-Mapped I/O Base:** This field specifies the lower limit for the low MMIO address range assigned to the Hub Interface buses for this and any other SIOHs in the system. These bits are compared against bits 31:24 of the transaction address. Bits 43:32 of the transaction address must be decoded as '0'.

3.28 Memory-Mapped I/O Limit Low Address Register (MMIOLL)

The MMIOBL register with the MMIOLL register specifies one of the two address ranges allocated for Hub Interface-destined transactions. MMIOBL and MMIOLL are intended to specify a memory-mapped I/O window below the 4 GB boundary. (Refer to Table 4-1 for how this register is decoded.)

For comparison purposes, address bits 23:0 are ignored and 43:32 must be zero.

Note: For E8870 chipset-based platforms, the upper limit of the MMIOL range is FDFF_FFFF. Therefore, this value should only be programmed to FD. (MMIOLL is inclusive for address decoding purposes.) More extensive programmability allows larger systems to implement their own address map restrictions.

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Device: Node_ID
Function: 5
Offset: 45h

Bit	Attr	Default	Description
7:0	RW	00h	**Memory-Mapped I/O Limit:** This field specifies the upper limit for the low MMIO address range assigned to the Hub Interface buses for this and any other SIOHs in the system. These bits are compared against bits 31:24 of the transaction address. Bits 43:32 of the transaction address must be decoded as '0'.

3.29 Memory-Mapped I/O Segment Low Register (MMIOSL[5:0])

The six MMIOSL registers specify the address ranges allocated for memory-mapped I/O transactions. The transaction address is compared to these boundaries for proper disposition to the low window. For comparison purposes, address bits 23:0 are ignored and 43:32 must be zero. For this decode, bits 43:32 must all be '0'. (Refer to Table 4-1 for how this register is decoded.)

The memory-mapped I/O space between MMIOSL[1] and MMIOSL[0] (port 0) is defined to be the compatibility port (interface to the ICH4 legacy bridges).

Note: It is assumed that the SIOH will never receive an address from a port that is destined for itself.

Device: Node_ID
Function: 5
Offset: 48h, 49h, 4Ah, 4Bh, 4Ch, 4Dh

Bit	Attr	Default	Description
7:0	RW	00h	**Memory-Mapped I/O Segment:** This field specifies the boundary between each of the five Hub Interface regions for *this* SIOH. These bits are compared against bits 31:24 of the transaction address.

3.30 Memory-Mapped I/O Base High Address Register (MMIOBH)

The MMIOBH registers with the MMIOLH registers specify the address range allocated for Hub Interface-destined transactions. MMIOBH and MMIOLH are intended to specify a MMIO window above the 4 GB boundary with a 64 MB granularity. The transaction address is compared against the base field for proper disposition. (Refer to Table 4-1 for how this register is decoded.)

Note: High MMIO space should always be programmed above the 4 GB boundary.

For comparison purposes, address bits 25:0 are ignored.

Device: Node_ID
Function: 5
Offset: 50h

Bit	Attr	Default	Description
15:0	RW	0000h	**Memory-Mapped I/O Base:** This field specifies the lower limit for the memory address range assigned to the Hub Interface buses for this and any other SIOHs in the system. These bits are compared against bits 41:26 of the transaction address.

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3.31 Memory-Mapped I/O Limit High Address Register (MMIOLH)

For comparison purposes, address bits 25:0 are ignored. MMIOLH is inclusive for address decoding purposes. (Refer to Table 4-1 for how this register is decoded.)

Note: High MMIO space should always be programmed above the 4 GB boundary.

Device: Node_ID
Function: 5
Offset: 52h

Bit	Attr	Default	Description
15:0	RW	0000h	**Memory-Mapped I/O Limit:** This field specifies the upper limit for the memory address range assigned to the Hub Interface buses for this and any other SIOHs in the system. These bits are compared against bits 41:26 of the transaction address.

3.32 Memory-Mapped I/O Segment High Address Register (MMIOSH[5:0])

The six MMIOSH registers specify the address ranges allocated for memory-mapped I/O transactions. The transaction address is compared to these boundaries for proper disposition to the high window. For comparison purposes, address bits 25:0 are ignored. (Refer to Table 4-1 for how this register is decoded.)

Notice that MMIOSH[0] specifies the top of the high MMIO window assigned to this SIOH component. The address compared to in this table is the transaction address from any port: five Hub Interface 2.0 ports, the Hub Interface 1.5 port, or either SP.

Note: High MMIO space should always be programmed above the 4 GB boundary.

For the SIOH, MMIOSH[0] and MMIOSH[1] should be programmed to the same value since the ICH4 cannot accept outbound accesses above the 4 GB boundary.

It is assumed that the SIOH will never receive an address from a port that is destined for itself.

Device: Node_ID
Function: 5
Offset: 54h, 56h, 58h, 5Ah, 5Ch, 5Eh

Bit	Attr	Default	Description
15:0	RW	0000h	**Memory-Mapped I/O Segment:** This field specifies the boundary between each of the five Hub Interface regions for *this* SIOH. These bits are compared against bits 41:26 of the transaction address.

3.33 PCI Configuration Bus Base Register (BUSNO[5:0])

These registers define the base (starting) PCI bus for the PCI configuration space for each Hub Interface port.

Device: Node_ID
Function: 5
Offset: 60h, 62h, 64h, 66h, 68h, 6Ah

Bit	Attr	Default	Description
15:8	RV	00h	*Reserved.*
7:0	RW	00h	**Start Bus Number:** The start PCI bus number of PCI configuration space to this port. This register is compared with BUS[7:0] of the configuration cycle (refer to Table 3-3).

3.34 SAPIC Segment Registers (SSEG[5:0])

The six SSEG registers specify the address ranges allocated for the memory-mapped I/O SAPIC, I/OAPIC, and PCI Hot-Plug regions. The transaction address is compared to these boundaries for proper disposition. For comparison purposes, address bits 43:20 are 000FECh (refer to Section 4.1.3, "SAPIC/IOAPIC and PCI Hot-Plug Ranges" for how these registers are decoded by the SIOH).

Device: Node_ID
Function: 5
Offset: 70h, 72h, 74h, 76h, 78h, 7Ah

Bit	Attr	Default	Description
15:13	RV	0	*Reserved.*
12:0	RW	0	**SAPIC Segment Register:** This field specifies the boundaries between the five SAPIC/Hot-Plug regions for *this* SIOH. These bits are compared against bits 19:8 of the transaction address.

3.35 I/O Link Registers (IOL[5:0])

The IOL registers specify the address range allocated for I/O space PCI transactions. The upper five bits of the transaction address (bits 15:11) is compared against the IOL registers for proper disposition. The I/O space for a given Hub Interface port has a 2 KB granularity.

If only one SIOH resides in the system, all of the 64K I/O space should be accounted for with the IOL registers. If two SIOHs reside in the system, both IOL register sets must be programmed so they do not overlap. In addition, the combination of both SIOH IOL register sets should account for the entire 64K I/O space. If there are two SIOH components in the system, IOL[0] of SIOH1 should be programmed to IOL[5] of SIOH0 (where SIOH0 interfaces the ICH4).

Refer to Section 4.1.2, "I/O Space" for how these registers are decoded for proper transaction routing.

Device: Node_ID
Function: 5
Offset: 80h, 81h, 82h, 83h, 84h, 85h

Bit	Attr	Default	Description
7:6	RV	0	*Reserved.*
5:0	RW	0	**I/O Port Base:** This field specifies the base I/O address of a particular Hub Interface port.

3.36 Chip Boot Configuration Registers (CBC)

These registers are used to relocate this chipset's configuration space to a different PCI bus. Information captured from the idle flits is valid only when the idle detection bit in the SPINCO register is set.

Note: BUS[7:0] should always be set to FF and Node ID[4:3] should always be set to 11.

Device: Node_ID
Function: 5
Offset: 98h

Bit	Attr	Default	Description
95:77	RV	0	*Reserved.*
76:72	RW	See Description	**Node ID[4:0]:** These bits define the device # of this SIOH. The default value is captured from the NODEID[4:0] pins on the rising edge of hard reset. These bits are sent in the idle flits.
71:67	RW	11111h	**Bus[7:3]:** The top five bits of this SIOH's configuration bus number. These bits are sent in the idle flits.
66:64	RW	See Description	**Bus[2:0]:** The lower 3 bits of this SIOH's configuration bus number. The default value is captured from BUSID[2:0] pins on the rising edge of hard reset. These bits are sent in the idle flits.
63:45	RV	0	*Reserved*
44:40	RO	11111h	**SP1 Node ID[4:0]:** Device number received from SP1's idle flits.
39:32	RO	FFh	**SP1 Bus[7:0]:** Bus number received from SP1's idle flits.
31:16	RV	0	*Reserved*
15	RWS	0	**StopOnErr:** 0 If an agent has detected an error and has sent an LLRReq and its local retry state machine is in RETRY_LOCAL_IDLE state, then it should not send any info or idle flits and sends a Ctrl flit with LLRIdle. 1 An agent will send idle or info flits when in RETRY_LOCAL_IDLE state.
14	RWS	0	**SndMultAck:** 0 LCC[7] = 0. Up to 25 ACKs will be sent in Byte D[4:0] of idle flits. Idle flits are forced whenever there are multiple acks. 1 0 or 1 ACK is sent in LCC[7] of idle flits. Byte D = 0.
13	RWS	0	**RcvMultAck:** 0 Up to 25 ACKs may be extracted from idle flits. Ack[4:0] = LCC[7] bit-wise OR'ed with Byte D[4:0]. Any particular idle flit will use either LCC[7] or Byte D, but not both. 1 0 or 1 ACK is extracted from LCC[7] of idle flits.
12:8	RO	11111h	**SP0 Node ID[4:0]:** Device number received from SP0's idle flits.
7:0	RO	FFh	**SP0 Bus[7:0]:** Bus number received from SP0's idle flits.

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3.37　Boot Flag Registers (BOFL)

To reset these registers back to the default value, system software writes to the SYRE register.

Device:　**Node_ID**
Function: 5
Offset:　**A4h**

Bit	Attr	Default	Description
31:8	RV	0	*Reserved.*
7:0	RO	A5h	**Signature:** This register is used to select boot strap CPU node. The first time this register is read, it will return a non-zero signature. All reads thereafter will return zeroes.

3.38　Scratch Pad Register (SPAD)

This scratch pad register is available for power-on software usage before any memory is available for use.This register is used during the boot process and SP Hot-Plug.

Device:　**Node_ID**
Function: 5
Offset:　**B0h**

Bit	Attr	Default	Description
31:0	RW	0	**System Scratch Pad.**

3.39　Scratch Pad Register Sticky (SPADS)

This scratch pad register is available for power-on software usage before any memory is available for use. The contents of this register remains sticky through reset. This register is used during the boot process and SP Hot-Plug.

Device:　**Node_ID**
Function: 5
Offset:　**B4h**

Bit	Attr	Default	Description
31:0	RWS	0	**System Scratch Pad:** The contents of this register is sticky.

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3.40   Performance Monitor Control Registers (PERFCON)

These registers are the common control and status registers for all of the performance monitor counters in the component. They have one control to enable all counters and another control to reset all performance monitor counters and registers to their default state. One status bit for each performance monitor module (two counters per module) is reflected in this register. The PMR registers for the specific module provide detailed status information. The status bit is activated by a count comparison event or an overflow from either counter of the module.

Device: Node_ID
Function: 5
Offset: BCh

Bit	Attr	Default	Description
31:11	RV	0	*Reserved.*
10	RO	0	**SPP_PM Count Status:** Status reported by the SP0_PM module. The OR of both "Event status" bits reported by either SP0_PM module for an overflow or max comparison condition.
9	RO	0	**HL4_PM Count Status:** Status reported by the HL3_PM module. The OR of both "Event status" bits reported by either HL3_PM module for an overflow or max comparison condition.
8	RO	0	**HL3_PM Count Status:** Status reported by the HL2_PM module. The OR of both "Event status" bits reported by either HL2_PM module for an overflow or max comparison condition.
7	RO	0	**HL2_PM Count Status:** Status reported by the HL1_PM module. The OR of both "Event status" bits reported by either HL1_PM module for an overflow or max comparison condition.
6	RO	0	**HL1_PM Count Status:** Status reported by the HL0_PM module. The OR of both "Event status" bits reported by either HL0_PM module for an overflow or max comparison condition.
5:2	RV	0	*Reserved.*
1	RW	0	**Local Count Enable:** Enables any counters on this component that have this bit assigned as the enable control in its individual PMR register. Each component counter can be programmed, via its PMR register, to be enabled by this bit or by an external EV pin.
0	RW	0	**Reset:** Reset all performance monitor registers in this component to default state. This will put every counter in an inactive state and allow programming only the counters of interest. The PERFCON register is not affected by this bit since it can be set to any desired value while setting the Reset control. This bit will automatically be cleared after the reset is completed so a separate programmed operation is not needed to clear it. For diagnostic purposes, the other registers can be read to verify proper operation.

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3.41 SP Performance Monitor Response and Control Registers (SP_PMR[1:0])

The PMR registers control operation of their associated counter, and provide overflow or max compare status information.

Device: Node_ID
Function: 5
Offset: C0h (SP_PMR[0]), C4h (SP_PMR[1])

Bit	Attr	Default	Description
31:26	RV	0	*Reserved.*
25	RW	0	**Req/RspType Bus Select:** 0 = Request Bus 1 = Response Bus
24	RW	0	**Event Register Select:** The PME register select events based on the SP header fields. The SP_PME_RSC register selects resource specific events that are mutually exclusive of the SP header events. One or the other of the event sets can be selected. 0 = SP events 1 = SP resources
23:22	RW	0	**Compare Mode:** This field defines how the PMCMP register is to be used. 00 - Compare mode disabled (PMCMP register not used). 01 - Max compare only: The PMCMP register value is compared with the counter value. If the counter value is greater then Count Compare Status (bit 13) of the "Event Status" field of this register will be set. 10 - Max compare with update of PMCMP at end of sample: The PMCMP register value is compared with the counter value, and if the counter value is greater, the PMCMP register is updated with the counter value. The Event Status field is not affected in this mode. 11 - Address compare mode where the PMCMP register is compared with the address field. Counter 0 of a counter pair will compare on an address greater than the register, and counter 1 will compare on an address equal to or lesser than the register (inverse of greater than). When both comparisons are valid, an address range comparison qualification is generated. This mode will cause the address range comparison to be AND'ed with the event qualification specified in the selected PME register of each counter. The Event Status field is not affected in this mode. The Address comparison range is A[38:7].
21:19	RW	0	**Reset Event Select:** Counter and event status will reset and counting will continue. 000 - No reset condition. 001 - Partner's event status: When the partner counter causes an event status condition to be activated, either by a counter overflow or max comparison, then this counter will reset and continue counting. 010 - Partners PME register event: When the partner counter detects a match condition that meets its selected PME register qualifications, then this counter will reset and continue counting. 011 - *Reserved* 100 - EV0 pin 101 - EV1 pin 110 - EV2 pin 111 - EV3 pin

Device: Node_ID
Function: 5
Offset: C0h (SP_PMR[0]), C4h (SP_PMR[1]) (Continued)

Bit	Attr	Default	Description
18:16	RW	0	**Count Event Select:** This field determines the counter enable source. 000 - PME register event. 001 - Partner event status (max compare or overflow). 010 - All clocks when enabled. 011 - *Reserved* 100 - EV0 pin 101 - EV1 pin 110 - EV2 pin 111 - EV3 pin
15:14	RW	0	**Count Mode:** 00 - Count event selected by **Count Event Select** field. 01 - Count clocks after event selected by **Count Event Select** field. 10 - Count transaction length of event selected by **Count Event Select** field. 11 - *Reserved*
13:12	RW	0	**Event Status:** This status bit captures an overflow or count compare event. The Event Status Output field can be programmed to allow this bit to be driven to an external EV pin. 00 - No event. x1 - Overflow -The PMD counter overflow status. 1x - Count compare - PMD counter greater than PMCMP register when in compare mode. This bit is sticky in that once an event is reported the status remains even though the original condition is no longer valid. This bit can be cleared by software or by starting a sample. Event status is always visible in the PERFCON register, except if "Event Status Output" field is in cascade mode. Note, if in address compare mode (compare mode = 11), the count compare bit is not activated.
11:9	RW	0	**Event Status Output:** This field selects where event status is reported, or an address compare if in address compare mode (compare mode = 11). 000 - Event status reported only in PERFCON register. 001 - Event status (overflow) reported to partner only. Used for cascading event counters. 100 - Event status or address comparison in PERFCON and on EV0 pin. 101 - Event status or address comparison in PERFCON and on EV1 pin. 110 - Event status or address comparison in PERFCON and on EV2 pin. 111 - Event status or address comparison in PERFCON and on EV3 pin.

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Bit	Attr	Default	Description
8:5	RW	0	**Counter Disable Source:** These bits control which input disables the counter. Note, if the "Enable Source" is inactive counting is also disabled. 1xxx - EV3 pin x1xx - EV2 pin xx1x - EV1 pin xxx1 - EV0 pin
4:2	RW	0	**Counter Enable Source:** These bits identify which input enables the counter. Default value disables counting. 000 - Disabled 001 - PERFCON **local_count_enable** field. 010 - Partner event status (max compare, overflow, or cascade). 011 - *Reserved* 100 - EV0 pin 101 - EV1 pin 110 - EV2 pin 111 - EV3 pin
1	RW	0	**Clear Overflow:** This bit clears the overflow bit in associated PMD counter. The counter continues counting. This bit is cleared by hardware when the operation is complete.
0	RW	0	**Reset:** Setting this bit resets all registers associated with this counter to the default state. It does not change this PMR register since any desired value can be loaded while setting the Reset bit. This Reset bit will clear itself after the reset is completed. For diagnostic purposes, the contents of the other registers can be read to verify operation of this bit. There is also a reset bit in the PERFCON register that clears all counter registers including the PMR.

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3.42 SP Performance Monitor Event Registers (SP_PME[1:0])

The SP performance counter logic provides the ability to monitor packets received by the SP interface of the SIOH. Events related to processor-generated PCI device requests and responses to PCI-initiated memory reads can be monitored.

The PME register is divided into major sub-groups. For some sub-groups, the events within a group are OR'ed together.

Device: Node_ID
Function: 5
Offset: C8h (SP_PME[0]), CCh (SP_PME[1])

Bit	Attr	Default	Description
31:28	RW	0	**DFT Events Mask (OR'ed group)**
27:25	RW	0	**DLEN Field:** Encodes the length of the transaction. 111 - Any length 000 - 0-8 bytes 001 - 16 bytes 010 - 32-bytes 011 - 64-bytes 100 - 128-bytes 101 to 110 - *Reserved*
24:21	RW	0	**Attribute:** 1111 - All attributes selected. xxxx - Value of the attribute field of the packet used to select (except 1111).
20:16	RW	0h	**Packet Src Node:** 11111 - All sources. xxxxx - Value of the Src Node ID used to select (except 11111).
15:14	RW	00	**SP Port Select:** 00 - *Reserved* 01 - SP0 10 - SP1 11 - SP0 or SP1
Packet Type Selection Group			
13:7	RW	0	**Type_Data:** xxxxyyz For request packets, the fields are: • xxxx is the request type major encoding. • yy is the request type minor encoding. • z is the coherency bit. For response packets, the fields are: • xxxx is the response type. • yy indicates the completion bit value (0y). • z is the coherency bit.
6:0	RW	0	**Type_Mask:** Determines which bits of the Type_Data field to be used in selecting the event. A value of 7Fh (all 1's) selects all packets.

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3.43 SP Performance Monitor Resource Event Registers (SP_PME_RSC[1:0])

These registers contain resource selections that are mutually exclusive to the event selections. These selections are not qualified by the event selections. Each individual field selection is OR'ed with the other fields to generate the counter match condition. These registers are selected via the Event Register Select Field in the PMR register.

Device: Node_ID
Function: 5
Offset: D0h (SP_PME_RSC[0]), D4h (SP_PME_RSC[1])

Bit	Attr	Default	Description
31:3	RW	0	*Reserved.*
2:0	RW	0	**Write Cache:** 000 - Disable count. 001 - Miss - Inbound write (request for ownership) results in a miss of the write cache. 010 -Inbound Hit Modified (unowned by any IOQ)- An inbound write hits a modified line in the write cache. 011 - Inbound Hit Modified, Stolen (different IOQ steals the line owned by another IOQ)- An inbound write hits a modified line in the write cache. 100 - Inbound Hit Exclusive (different IOQ steals the line)- An inbound write hits an exclusive line in the write cache. 101 - Outbound Invalidate Modified - Results in an implicit writeback. 110 - Outbound Invalidate Exclusive - SIOH gives up ownership of the line to the initiator on the SP. 111 - Line Eviction - Results in an explicit writeback.

3.44 SP Performance Monitor Data Registers (SP_PMD[1:0])

These registers are the actual counter value. The overflow bit can be cleared via the PMR register without perturbing the value of the counter. This counter is reset at the beginning of a sample period. The counter can be preloaded to cause an early overflow, otherwise it will be reset at the start of a sample period.

Device: Node_ID
Function: 5
Offset: D8h (SP_PMD[0]), DCh (SP_PMD[1])

Bit	Attr	Default	Description
31	RW	0	Overflow.
30:0	RW	0	Current counter value.

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3.45 SP Performance Monitor Compare Register (SP_PMCMP[1:0])

The compare register can be used three ways as selected in the "Compare Mode" field of the PMR register. First, when PMD is incremented, the value of PMD is compared to the value of PMCMP. If PMD is greater than PMCMP, this status is reflected in the PERFCON register and/or on EV pins as selected in the "Event Status Output" field of the PMR register. Secondly, update the PMCMP register with the value of PMD if the PMD register exceeds the contents of PMCMP.

The third mode is an address comparison mode. PMD0 compares on addresses greater than the PMCMP0 register, and PMD1 compares on addresses less than or equal to PMCMP1. The "AND" of these two comparisons is the address range comparison and it qualifies the other match event conditions for both counters. Note that the contents of PMCMP are compared to A[38:7].

Device: Node_ID
Function: 5
Offset: E0h (SP_PMCMP[0]), E4h (SP_PMCMP[1])

Bit	Attr	Default	Description
31:0	RW	FFFF_FFFFh	Counter compare value.

3.46 Error Command Registers (ERRCOM)

These registers enable error checking and flagging on various error conditions.

Device: Node_ID
Function: 6
Offset: 40h

Bit	Attr	Default	Description
15	RV	0	*Reserved.*
14:10	RW	11111	**SP Timer Duration:** Time-out = 2^{size} cycles, where *size* is determined by the value of this field. Maximum value is 24 (the timer is a 24-bit counter, incrementing at core clock divided by 8, or 25 MHz). The maximum time-out is approximately 2X the timer duration. If this field is all ones, the SP Timer is disabled.
9:3	RV	0	*Reserved.*
2	RW	0	**Error Freeze on Fatal Error:** 0 = Normal operation. 1 = Disable Hub Interfaces and SP interfaces when a fatal error is signaled or observed on the ERR[2:0]# pins.
1	RW	0	**Error Freeze Upon Non-Correctable Error:** 0 = Normal operation. 1 = Disable Hub Interfaces and SP interfaces when a non-correctable error is signaled or observed on the ERR[2:0]# pins.
0	RW	0	**Error Freeze Upon Correctable Error:** 0 = Normal operation. 1 = Disable Hub Interfaces and SP interfaces when a correctable error is signaled or observed on the ERR[2:0]# pins.

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3.47 First Error Status Registers (FERRST)

Errors are classified into two basic types: fatal (or non-recoverable) and non-fatal (or recoverable). Non-fatal errors are further classified into correctable and non-correctable errors. First fatal and/or non-fatal errors are flagged in the FERRST register. At most two errors can be reported by the FERRST; one for non-recoverable (or fatal) errors, one for recoverable (or uncorrectable and correctable) errors.

Associated with some of the errors flagged in the FERRST register are control and data logs. In some cases, the logs are duplicated for the same error. Fields in the FERRST register identify which unit has the corresponding error. Once a first error for a type of error has been flagged (and logged), the log registers for that error type remain fixed until either the bit associated with the error type in the FERRST is cleared, or a power-on reset. Contents of the error logs are not reliable unless an error associated with the log is reported in FERRST.

When the first error of a type is detected (fatal, uncorrectable, correctable), the value of the error status pin associated with this error type is latched in the FERRST register.

Device: Node_ID
Function: 6
Offset: 44h

Bit	Attr	Default	ERR Type	Description
63	ROS	Last State of ERR[2]# (inverted)	N/A	**Last Fatal Error State:** The value on the ERR[2]# pin input (inverted for active high indication) is captured here immediately when a fatal error is latched in the FERRST. This allows software to identify the component that drove the first *fatal* error when the ERR[2:0]# pins are wired-or together with the other components.
62	ROS	State of last ERR[1]# (inverted)	N/A	**Last Uncorrectable Error State:** The value on the ERR[1]# pin input (inverted for active high indication) is captured here immediately when an Uncorrectable error is latched in the FERRST. This allows software to identify the component that drove the first *uncorrectable* error when the ERR[2:0]# pins are wired-or together with the other components.
61	ROS	State of last ERR[0]# (inverted)	N/A	**Last Correctable Error State:** The value on the ERR[0]# pin input (inverted for active high indication) is captured here immediately when a correctable error is latched in the FERRST. This allows software to identify the component that drove the first *correctable* error when the ERR[2:0]# pins are wired-or together with the other components.
60:57	RV	0	N/A	*Reserved.*
Start of SPP Error Bits				
56	RCS	0	Fatal	**SP Protocol Error:** Set when the SP protocol state machines wind up in an indeterminate state, or for protocol errors.
55	RCS	0	Fatal	**SP Queue/Buffer (LRB) Time-out Error:** Refer to the ERRCOM register.
54	RCS	0	Fatal	**Received *Failed* or Unexpected *Unsupported* Response:** Set if a Failed or Unexpected unsupported response is received on the SP.
53	RCS	0	Fatal	**Strayed SP Transaction:** Set when strayed transactions are detected on SP cluster. A "strayed" transaction is one where a completion returns for a transaction that was never requested.
52	RV	0	N/A	*Reserved.*

Device: Node_ID
Function: 6
Offset: 44h (Continued)

Bit	Attr	Default	ERR Type	Description
51	RCS	0	Unc	**Partial Merge Multi-Bit Data ECC Error:** A partial write occurs to the write cache (requiring a RMW) and a multi-bit ECC error is detected on the data. ECC checking, correction and/or poisoning is done within the 8-byte boundary of the partial write.
50	RCS	0	Corr	**Partial Merge Single-Bit Data ECC Error:** A partial write occurs to the write cache (requiring a RMW) and a multi-bit ECC error is detected on the data. ECC checking, correction and/or poisoning is done within the 8-byte boundary of the partial write.
49	RCS	0	Corr	**Illegal SP Address Error:** Set when an illegal address is detected on the SP. This includes an inbound access when: • Both SP ports are disabled. • An inbound access targeting an inoperative SP port (unframed). • Outbound SP requests with illegal attributes. • Outbound addresses that miss all the SIOH address range registers.
48	RCS	0	Corr	**Received Master Abort Response:** Set if a master abort response is received on the SP.
Start of Hub Interface Error Bits				
47:45	ROS	000	N/A	**Hub Interface Fatal Error Pointer:** If a Hub Interface cluster has reported the first fatal error, this field indicates which cluster has reported the error. 000 - Hub Interface Port 0 001 - Hub Interface Port 1 010 - Hub Interface Port 2 011 - Hub Interface Port 3 100 - Hub Interface Port 4 101 to 111 - *Reserved*
44:42	ROS	0	N/A	**Hub Interface Uncorrectable Error Pointer:** If a Hub Interface cluster has reported the first non-fatal error and the error is uncorrectable, this field indicates which cluster has reported the error. 000 - Hub Interface Port 0 001 - Hub Interface Port 1 010 - Hub Interface Port 2 011 - Hub Interface Port 3 100 - Hub Interface Port 4 101 to 111 - *Reserved*
41:39	ROS	0	N/A	**Hub Interface Correctable Error Pointer:** If a Hub Interface cluster has reported the first non-fatal error and the error is correctable, this field indicates which cluster has reported the error. 000 - Hub Interface Port 0 001 - Hub Interface Port 1 010 - Hub Interface Port 2 011 - Hub Interface Port 3 100 - Hub Interface Port 4 101 to 111 - *Reserved*
38	RCS	0	Fatal	**Hub Interface Header Multi-Bit ECC Error (Hub Interface 2.0) or Parity Error (Compatibility Port):** Set if a multi-bit ECC error (Hub Interface 2.0)or parity error (Hub Interface 1.5) is detected in the header of a Hub Interface packet.

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Device: Node_ID
Function: 6
Offset: 44h (Continued)

Bit	Attr	Default	ERR Type	Description
37	RCS	0	Fatal	**Hub Interface - Received DO_SERR# Message:** The SIOH received a DO_SERR# special cycle on the Hub Interface.
36	RCS	0	Fatal	**Received Illegal Hub Interface Request, Unexpected or Invalid Response:** The SIOH received an unsupported transaction: • Inbound I/O read or write transaction. • Inbound Configuration read or write transaction. • Inbound Unsupported Special cycle. • Inbound Locked read or write transactions. • Any inbound write with a completion required. • Any outbound completion that does not match with any pending outbound request.
35	RV	0		*Reserved.*
34	RCS	0	Unc	**Received Hub Interface Target Abort:** A Hub Interface outbound read or delayed write receives a Target Abort completion.
33	RCS	0	Unc	**Inbound Hub Interface Multi-Bit Data ECC Error (Hub Interface 2.0) or Parity Error (Compatibility Port):** Set if a multi-bit ECC error (Hub Interface 2.0) or parity error (Hub Interface 1.5) is detected in the data of a Hub Interface packet. This bit applies to data flowing inbound (inbound write and outbound read completion).
32	RCS	0	Unc	**Outbound Multi-Bit Data ECC Error at Hub Interface 1.5 Cluster:** Before forwarding a packet on Hub Interface **1.5** (SIOH end points), the Hub Interface cluster detects a multi-bit ECC error on the *data*. This bit applies to data flowing outbound (outbound write and inbound read completion).
31	RV	0		*Reserved.*
30	RCS	0	Corr	**Inbound Hub Interface 2.0 Single-Bit Data ECC Error:** Set if a single-bit ECC error is detected in the data of a Hub Interface packet. This bit applies to data flowing inbound (inbound write and outbound read completion).
29	RCS	0	Corr	**Received Hub Interface 2.0 Header Single-Bit ECC Error:** Set if a single-bit ECC error is detected in the header of a Hub Interface packet.
28	RCS	0	Corr	**Outbound Single-Bit Data ECC Error at Hub Interface** 1.5**Cluster:** Before forwarding an outbound write or inbound read completion packet on Hub Interface 1.5 (SIOH end points), the Hub Interface cluster detects a single bit ECC error on the *data*.
27	RCS	0	Corr	**Hub Interface Illegal Address Error:** Set when an inbound illegal address is detected at the Hub Interface interface.
26	RCS	0	Corr	**Received Master Abort on Hub Interface or unimplemented special cycle:** This bit is asserted when the SIOH receives a master abort termination on the bus for an outbound transaction, or a special cycle that is not implemented by the interfacing component.
25:18	RV	0	N/A	*Reserved.*

Device: **Node_ID**
Function: **6**
Offset: **44h (Continued)**

Bit	Attr	Default	ERR Type	Description
Start of SPL Error Bits				
17:15	RV	0		*Reserved.*
14	ROS	0	N/A	**SPL Fatal Error Pointer:** If an SPL has reported the first fatal error, this field indicates which SP has reported the error. 0 = SP 0 1 = SP 1
13	ROS	0	N/A	**SPL Uncorrectable Error Pointer:** If an SPL has reported the first non-fatal error and the error is an uncorrectable error, this field indicates which SP has reported the error.
12	ROS	0	N/A	**SPL Correctable Error Pointer:** If an SPL has reported the first non-fatal error and the error is a correctable error, this field indicates which SP has reported the error.
11	RCS	0	Fatal	**Link Error:** Failed SP LLR, LLR not enabled, or strobe glitch error.
10	RCS	0	Unc	SP Multi-Bit Data ECC Error.
9	RCS	0	Corr	Idle Flit Duplication Error.
8	RCS	0	Corr	Parity Error on the Link.
7	RCS	0	Corr	SP Single-Bit Data ECC Error.
Start of Configuration Error Bits				
6:2	RV	0h		*Reserved.*
1	RCS	0	Fatal	**Configuration Multi-Bit Data ECC Error:** This bit is set when a multi-bit ECC error was detected on data written to the SIOH configuration registers.
0	RCS	0	Corr	**Configuration Single-Bit Data ECC Error:** This bit is set when a single-bit ECC error was detected on data written to the SIOH configuration registers.

Refer to Table 3-6 for the logging registers used with each group.

Table 3-6. Error Log Register Grouping

Error Bit Group	Logging Registers
SPP	RECSPP, NRECSPP
Hub Interface	RECHUB, REDHUB, NRECHUB, PCISTS
SPL	RECSPL[1:0], REDSPL[1:0]
Configuration	RECSPP

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3.48 Two or More Errors Status Register (SERRST)

This register indicates that two or more instances of errors have happened in the SIOH. Multiple bits can be set in this register. Each bit in this register (except FERRST[63:61]) corresponds to the same bit descriptions in the FERRST register.

Note: Multiple error occurrences cause the pointer fields of this register (SERRST[14:12] and SERRST[47:39]) to be invalid.

Device: Node_ID
Function: 6
Offset: 4Ch

Bit	Attr	Default	ERR Type	Description
63:57	RV	0	N/A	*Reserved.*
56:0	See the FERRST register for the definition, attribute and default state of each bit.			

3.49 Error Mask Registers (ERRMASK)

The size of this register exactly matches the size of FERRST register. Each bit in this register will mask the corresponding bit in FERRST and SERRST. "Mask" here means that while the corresponding bit in FERRST or SERRST register can still be set or cleared, it won't trigger events on ERR[2:0]#.

Device: Node_ID
Function: 6
Offset: 54h

Bit	Attr	Default	Description
63:57	RV	0	*Reserved.*
56:0	RW	All 1's	0 = No effect. 1 = Mask the corresponding bit in the FERRST and SERRST registers.

3.50 SPP Recoverable Error Control Register (RECSPP)

This register latches control information for the first non-fatal error detected inside the SP cluster. Not all errors have logs.

Device: Node_ID
Function: 6
Offset: 64h

Bit	Attr	Default	Description
63:0	ROS	0	SP request/response header or internal request/response header.

3.51 SPP Non-Recoverable Error Control Register (NRECSPP)

This register latches control information for the first fatal error detected inside the SPP cluster. Not all errors have logs.

Device: Node_ID
Function: 6
Offset: 78H

Bit	Attr	Default	Description
63:0	ROS	0	SP request/response header or internal request/response header.

3.52 SP Interface Control Registers (SPINCO[1:0])

These registers are common across all E8870 chipset components, and they provide the control and status for each SP. Two GPIO pins (GPIO[1:0]) are associated with each SP. These pins are open drain, and are observable and controllable from this register.

Device: Node_ID
Function: 6
Offset: 80h (SPINCO[0]), A0h (SPINCO[1])

Bit	Attr	Default	Description
31:26	RWS	0	**Scratch Bits:** These bits may be used by software to record information specific to this SP. For example, hot-plug sequencing history.
25	RO	GPIO[1] state	**GPIO[1] State:** This bit reflects the state of GPIO[1]. 0 = GPIO[1] pin is high. 1 = GPIO[1] pin is low.
24	RO	GPIO[0] state	**GPIO[0] State:** This bit reflects the state of GPIO[0]. 0 = GPIO[0] pin is high. 1 = GPIO[0] pin is low.
23	RWS	0	**GPIO[1] Output Enable:** This bit configures GPIO[1] as an input or output signal. 0 = Do not drive the GPIO[1] pin (input only). 1 = Drive the GPIO[1] pin low (open drain output).
22	RWS	0	**GPIO[0] Output Enable:** This bit configures GPIO[0] as an input or output signal. 0 = Do not drive the GPIO[0] pin (input only). 1 = Drive the GPIO[0] pin low (open drain output).
21	RW	0	**INT_OUT:** 0 = Do not drive the INT_OUT# pin low. 1 = Drive the INT_OUT# pin low (open drain output).
20:19	RO	0	**SPAlign:** The value of this field reflects the staging delays through the scalability port input mux to frame the transfer of data from the SP source synchronous data transfer to the core clock of the component.
18:16	RWS	101	**Response Credits:** Credits supported by this SP port on the response VC. Credit = 2^{size} except that when size >= 101, credit = 25 instead of 32. These bits are sent in the idle flits. Must be set to a value <= 25 for reliable SP operation.

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Bit	Attr	Default	Description
15:13	RWS	101	**Request Credits:** Credit supported by this SP port on request VC. Credit = 2^{size} except that when size >= 5 (101b), credit = 25 instead of 32. These bits are sent in the idle flits. Must be set to a value <= 25 for reliable SP operation.
12	RW	0	**Disable SP Link Level Retry (LLR):** When set, this bit will disable link level retry on SP. Note: SP LLR is always disabled during framing/initialization.
11:9	RO	0	**Connecting SP Response Credits:** Credits supported by the response VC of the device connected to this SP port. Credit = 2^{size} except that when size= 5 (101b), credit = 25 instead of 32. This field is captured and updated from the idle flits.
8:6	RO	0	**Connecting SP Request Credits:** Credits supported by the request VC of the device connected to this SP port. Credit = 2^{size} except that when size = 5 (101b), credit = 25 instead of 32. This field is captured and updated from the idle flits.
5	RWS	1	**Enable SP:** 0 = The port is disabled. The outputs of the SP excluding SPSync are tri-stated. Deassertion will cause the port to deassert SPSync and enter initialization sequence. Disabling an SP should not be done with a configuration transaction from the same SP as the one being disabled. The configuration write will not complete. 1 = Enable SP output drivers. The port must complete initialization and framing before data can be transferred.
4	RO	0	**Idle Flit Acknowledgment Detected:** Detected idle_ack from the idle flits received by this SP. This bit is cleared at the beginning of the initialization sequence.
3	RO	0	**Idle Flit Detected:** Set during framing when 256 valid idle flits in a row are detected by the SP receiver. This bit is cleared at the beginning of the initialization sequence.
2	RW	0	**Interrupt on SP Idle Flit State Change:** 1 = A 0->1 transition of the idle-flit-detected bit in the above field will trigger an interrupt from this chip via INT_OUT#. 0 = De-assert the interrupt request controlled by this bit. The open drain interrupt pin (INT_OUT#) may remain asserted if other interrupt conditions exist. Note that the detection mechanism is initialized at the start of port framing only.
1	RO	See Description	**SP_PRES State:** This bit follows the SP_PRES pin associated with this SP. When deasserted, the output of the SP are tri-stated, and transactions targeting the SP are master-aborted.
0	RW	0	**Interrupt on Pin SP_PRES State Change:** 1 = A 0->1 or 1->0 transition in the above field will trigger an interrupt from this chip (via INT_OUT#). 0 = De-assert the interrupt request controlled by this bit. The open drain interrupt pin (INT_OUT#) may remain asserted if other interrupt conditions exist.

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3.53 SPL Recoverable Error Control Register (RECSPL[1:0])

This register latches control information for the first non-fatal error detected inside the SPL cluster. Not all errors have logs.

Device: Node_ID
Function: 6
Offset: 84h (RECSPL[0]), A4h (RECSPL[1])

Bit	Attr	Default	Description
63:0	ROS	0	SP request/response header or SP PHIT#, PHIT parity and PHIT, SP LLR retry counts.

3.54 SPL Recoverable Error Data Registers (REDSPL[1:0])

These registers latch Syndrome and ECC information for the first non-fatal error detected inside the SPL cluster. Not all errors have logs.

Device: Node_ID
Function: 6
Offset: 84h (REDSPL[0]), A4h (REDSPL[1])

Bit	Attr	Default	Description
15:8	ROS	00h	**Syndrome:** This field is the calculated syndrome. This field points to the error type (multi or single-bit) and the data bit in error for single-bit errors.
7:0	ROS	00h	**ECC:** This field is the ECC packet received on the SP for the flit in error.

![intel® logo]

Address Map 4

4.1 Address Ranges

Relatively few memory spaces are positively decoded by the SIOH. Any inbound address that falls outside the regions described in this chapter is routed to the SP interface.

4.1.1 Memory-Mapped I/O

Figure 4-1 shows the memory-mapped I/O map as seen by the SIOH component. There are two MMIO regions for the SIOH. One region is programmed to a window below 4 GB with MMIOBL, MMIOLL, and MMIOSL[5:0] while the other is programmed above 4 GB with MMIOBH, MMIOLH, and MMIOSH[5:0]. The registers defining each of these regions are described in Chapter 3, "Configuration Registers". These registers restrict the low MMIO granularity to 16 MB and the high MMIO granularity to 64 MB.

The purpose for two regions is to support the added requirement of PCI-X, which inherently supports addressing above 4 GB (greater than 32-bit). Applications such as clustering require large MMIO spaces so that one server has a window into the other server's memory space.

Note: Figure 4-1 illustrates an image when there is no memory-mapped I/O space associated with Hub Interface Port 1. In addition, since the ICH4 cannot support MMIO space greater than 32-bits, Port 0 will not be programmed to have a high MMIO range.

For E8870 chipset-based platforms, the MMIOLL register will be programmed to an upper limit of FDFF_FFFFh. For ease of BIOS PCI enumeration, the compatibility bus MMIO space is at the top. BIOS sets up the MMIO space for the compatibility bus (bus 0) first. If this space was not at the top, it would need to be first programmed to the top and continually reprogrammed (moved down) throughout the enumeration process.

When the platform supports two SIOH components, MMIOBL, MMIOBH, MMIOLL, and MMIOLH must be programmed identically in both SIOH components. For proper peer-to-peer operation, the MMIOS registers of the second SIOH component must be programmed within MMIOB{H/L} and MMIOL{H/L}.

Note: In order to allow an SIOH to manage a contiguous MMIO space, the base (MMIOB{H/L}) or limit register (MMIOL{H/L}) must be programmed to the same value as either MMIOS{H/L}[0] or MMIOS{H/L}[5].

Figure 4-1 illustrates a correct programming example. Programming the base *and* limit registers outside of the aperture defined by the contiguous segment registers is an invalid programming model.

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Figure 4-1. SIOH Memory-Mapped I/O Space Example
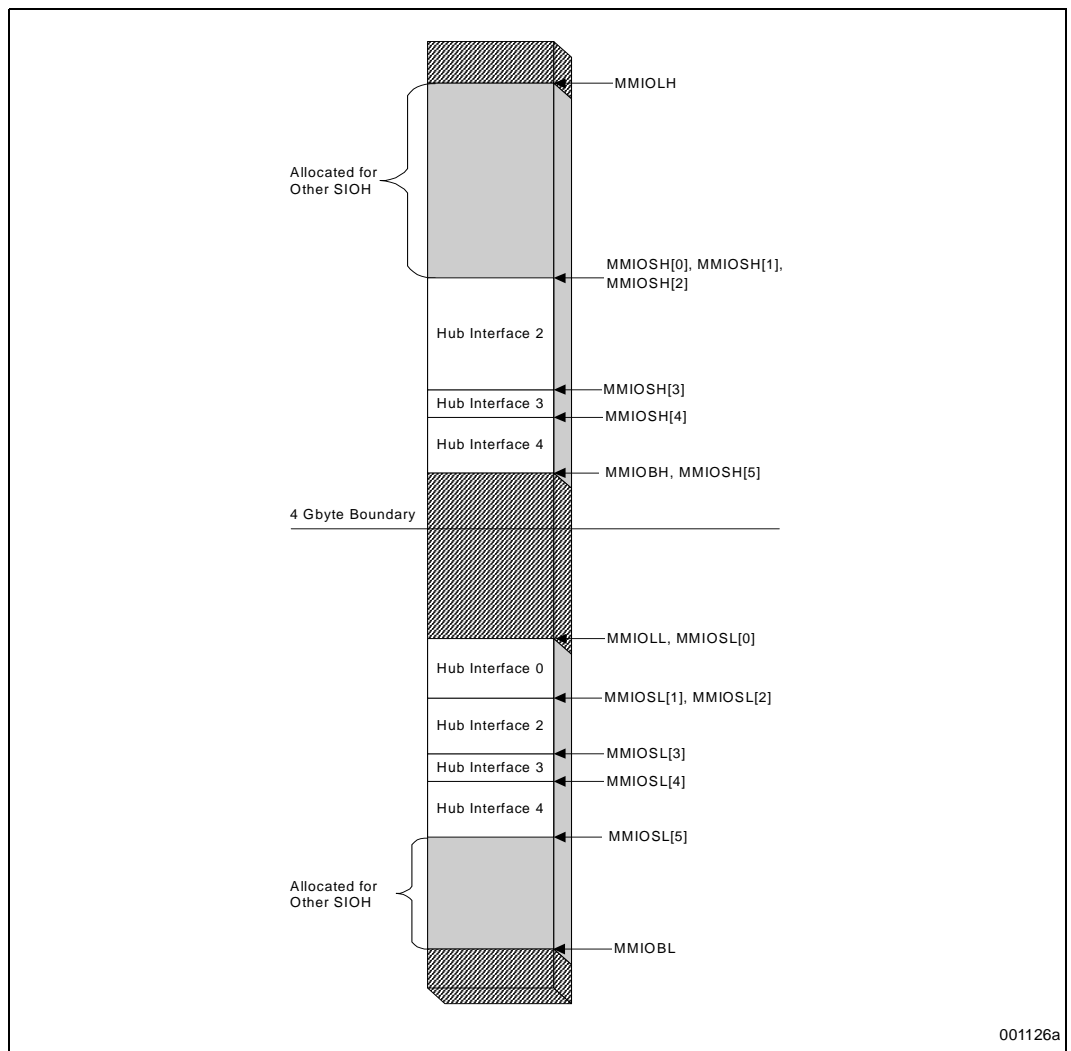
To determine where to forward a memory-mapped I/O cycle, refer to Table 4-1.

Table 4-1. Memory-Mapped I/O Cycle Routing

Forward to	Address Comparison
SPS (inbound only)	MMIOLH >= Address[41:26] > MMIOSH[0] (Address[63:42] = 0)
	MMIOSH[5] >= Address[41:26] > MMIOBH (Address[63:42] = 0)
	MMIOLL >= Address[31:24] > MMIOSL[0] (Address[63:32] = 0)
	MMIOSL[5] >= Address[31:24] > MMIOBL (Address[63:32] = 0)
Hub Interface Port 0	MMIOSH[0] >= Address[41:26] > MMIOSH[1] (Address[43:42] = 0)
	MMIOSL[0] >= Address[31:24] > MMIOSL[1] (Address[43:32] = 0)
Hub Interface Port 1	MMIOSH[1] >= Address[41:26] > MMIOSH[2] (Address[43:42] = 0)
	MMIOSL[1] >= Address[31:24] > MMIOSL[2] (Address[43:32] = 0)

Table 4-1. Memory-Mapped I/O Cycle Routing (Continued)

Forward to	Address Comparison
Hub Interface Port 2	MMIOSH[2] >= Address[41:26] > MMIOSH[3] (Address[43:42] = 0)
	MMIOSL[2] >= Address[31:24] > MMIOSL[3] (Address[43:32] = 0)
Hub Interface Port 3	MMIOSH[3] >= Address[41:26] > MMIOSH[4] (Address[43:42] = 0)
	MMIOSL[3] >= Address[31:24] > MMIOSL[4] (Address[43:32] = 0)
Hub Interface Port 4	MMIOSH[4] >= Address[41:26] > MMIOSH[5] (Address[43:42] = 0)
	MMIOSL[4] >= Address[31:24] > MMIOSL[5] (Address[43:32] = 0)

For example, assume that MMIOSL[0] is programmed to FD and MMIOSL[1] is programmed to F9. This programming indicates that Hub Interface Port 0 claims the range from FA00_0000h to FDFF_FFFFh.

To disable an MMIO range, the base and limit registers for that segment are programmed to the same value. For example, to disable Hub Interface Port 2, program MMIOSH[2] and MMIOSH[3] to the same value and MMIOSL[2] and MMIOSL[3] to the same value.

4.1.2   I/O Space

Figure 4-2 shows the I/O memory map seen by the SIOH. There is a total of 64 KB of legacy I/O space for the system. The SIOH component must be programmed so that I/O spaces do not overlap.

Note: Figure 4-2 illustrates the image when there is no I/O space associated with Hub Interface Port 3.

Refer to Table 4-2 to determine where to forward an I/O cycle based on the I/O address. If the SIOH receives an I/O transaction where the address does not fall within any of the I/O spaces and the attribute is set to DND, then the transaction should be master aborted.

Figure 4-2. SIOH I/O Space
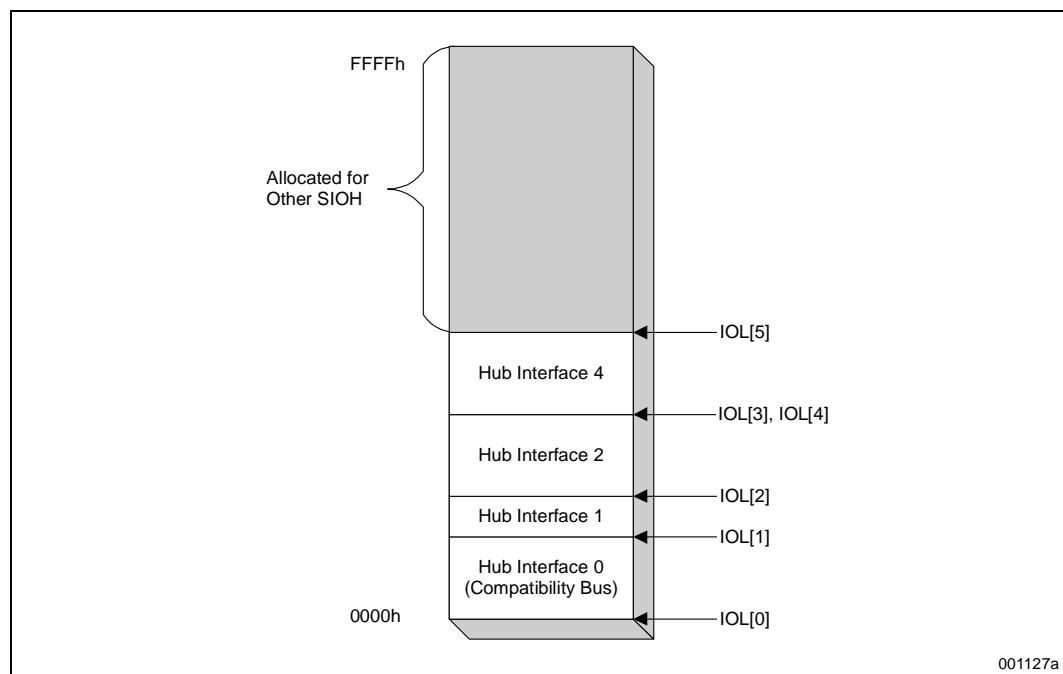
Table 4-2. I/O Cycle Routing

Forward to	Address Comparison
Hub Interface Port 0	IOL[0] <= Address[15:11] < IOL[1]
Hub Interface Port 1	IOL[1] <= Address[15:11] < IOL[2]
Hub Interface Port 2	IOL[2] <= Address[15:11] < IOL[3]
Hub Interface Port 3	IOL[3] <= Address[15:11] < IOL[4]
Hub Interface Port 4	IOL[4] <= Address[15:11] < IOL[5]

Note: The IOL registers have one bit more than the address bits they compare with (15:11). This is necessary since the upper boundary (IOL[5] for example) actually points to one block *above* the port it indicates.

The compatibility port is required to have a 4 KB region allocated to it. The highest dedicated I/O address required for legacy is 0CF9 (reset generator) and therefore exceeds the 2 KB granularity of the SIOH.

4.1.2.1 I/O Space Programming Example

Assume that a single SIOH consumes the entire I/O space (0000 - FFFFh). Table 4-3 lists an example of I/O space partitioning and how the IOL registers would be programmed. In terms of comparison, IOL[5:0] is compared with I/O address[16:11], even though for I/O addresses, A[16] doesn't exist.

Table 4-3. I/O Space Programming Example

Hub Interface	I/O Region	IOL Programming
0	0000 - 3FFFh	IOL[0] = 00h
1	4000 - BFFFh	IOL[1] = 08h
2	C000 - D7FFh	IOL[2] = 18h
3	D800 - EFFFh	IOL[3] = 1Bh
4	F000 - FFFFh	IOL[4] = 1Eh IOL[5] = 20h

4.1.3 SAPIC/IOAPIC and PCI Hot-Plug Ranges

There are five SAPIC/IOAPIC/PCI Hot-Plug ranges (SAR ranges) programmed for the SIOH. Each Hub Interface port correlates with one range implying that the P64H2's two SAPIC and PCI Hot-Plug controllers (one per PCI-X bus) must reside within the same contiguous region.

Refer to Table 4-4 to determine where to forward SAR transactions.

Note: System software must ensure that both the SAPIC and Hot-Plug ranges for the PCI bridge are within the same region.

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Figure 4-3. SIOH SAPIC Space
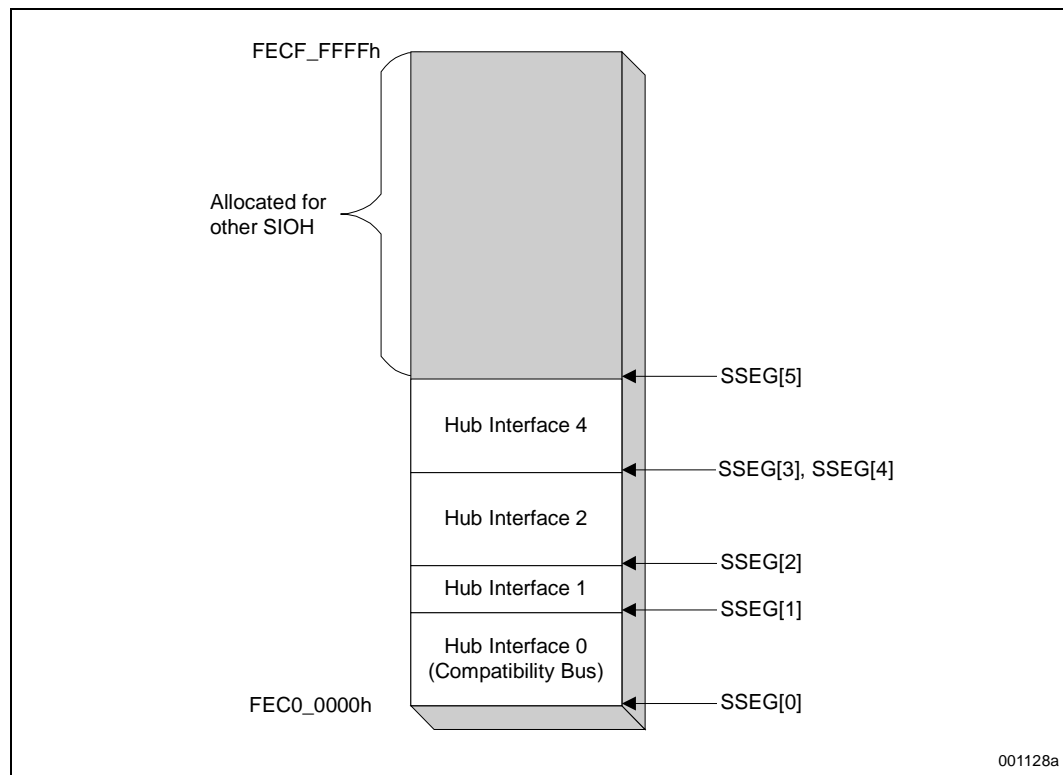
Table 4-4. SAPIC/IOAPIC and PCI Hot-Plug Cycle Routing

Forward to	Address Comparison[1]
SPS (inbound only)	Address[19:8] < SSEG[0]
	SSEG[5] <= Address[19:8]
Hub Interface Port 0	SSEG[0] <= Address[19:8] < SSEG[1]
Hub Interface Port 1	SSEG[1] <= Address[19:8] < SSEG[2]
Hub Interface Port 2	SSEG[2] <= Address[19:8] < SSEG[3]
Hub Interface Port 3	SSEG[3] <= Address[19:8] < SSEG[4]
Hub Interface Port 4	SSEG[4] <= Address[19:8] < SSEG[5]

1. Address[43:20] must match 000FECh.

For example, assume that SSEG[0] is programmed to 000h, and SSEG[1] is programmed to 100h. This programming indicates that Hub Interface Port 0 claims the range from FEC0_0000h to FEC0_FFFFh.

To disable a range, the base and limit registers for that segment are programmed to the same value. For example, to disable Hub Interface Port 2, program SSEG[2] and SSEG[3] to the same value.

Note: The SSEG registers have one bit more than the address bits they compare with (19:8). This is necessary since the upper boundary (SSEG[5] for example) actually points to one block *above* the port it indicates.

4.1.4 Compatibility Bus

The IOCTL register defines if the compatibility bus interfaces *this* SIOH component. The compatibility bus is defined as the Hub Interface port interfacing the ICH4 component and is always Hub Interface Port 0 throughout this document. (Refer to Section 3.25, "SIOH Control Registers (IOCTL)" for details.)

4.1.5 VGA Space

The IOCTL register defines the Hub Interface port that connects to the bridge interfacing the video adapter. The SIOH uses this register as a pointer to send accesses to the legacy VGA space. This register allows the VGA adapter to reside on any Hub Interface port. (Refer to Section 3.25, "SIOH Control Registers (IOCTL)" for details.)

4.1.5.1 MDA Space

The IOCTL register defines a bit that enables the legacy Monochrome Display Adapter space on the compatibility bus. This legacy MMIO space comprises 000B_0000h to 000B_7FFFh. If enabled, all inbound MDA accesses are routed to the compatibility port. This routing allows a monochrome adapter to reside on the compatibility bus whereas the VGA adapter might reside wherever the IOCTL indicates. If the bit is disabled, accesses to this range are sent to the VGA port.

4.2 Illegal Addresses

For most illegal accesses, the transaction is master aborted. Master Abort has different specifics depending on the initiating interface.

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Clocking 5

5.1 SIOH Clocking

This chapter describes the external clocking required for the SIOH. Figure 5-1 illustrates an example of how the SIOH receives and provides clocks between other E8870 chipset components.

Figure 5-1. SIOH Platform Clocking Example
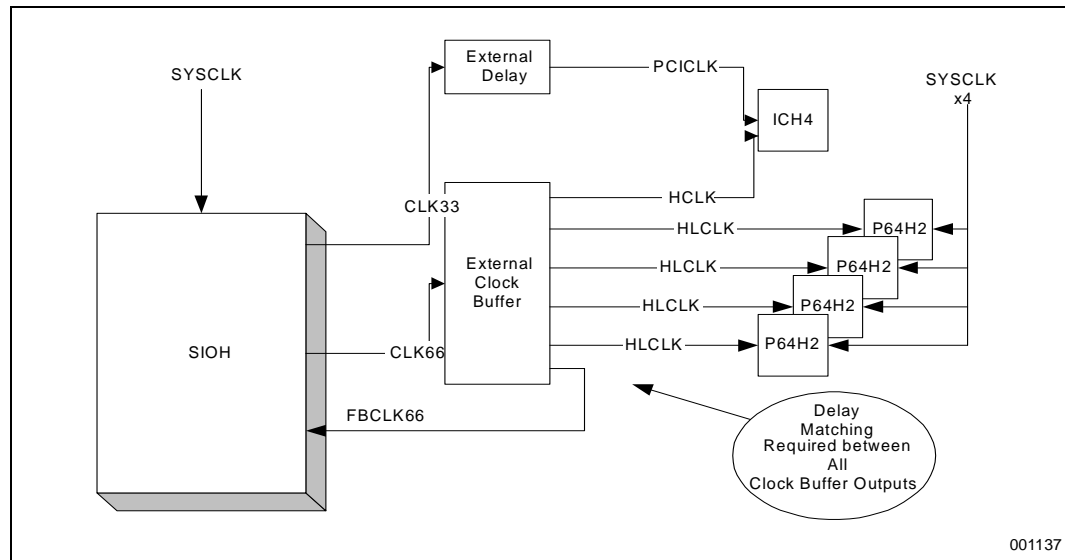
5.2 Reference Clock (SYSCLK)

In all E8870 chipset-based systems, a 200 MHz system clock is provided to the SIOH. This clock has no required phase relationship with respect to the SNC clock. This is possible because there are no common clock signals across the SP. This is the reference clock for all SIOH PLLs. The SIOH has multiple external interfaces: SP, 8-bit Hub Interface and 16-bit Hub Interface. The Hub Interfaces have a base frequency of 66 MHz.

These interfaces have common clock signals and require an in-phase clock at both sides of the interface. In addition, the 8-bit Hub Interfaces require clocks for quad-pumping the source-synchronous data and 16-bit Hub Interfaces require octal-pumping of the source-synchronous data. The SIOH supplies external Hub Interface components with a 66 MHz clock. To minimize cascaded jitter effects, the E8870 chipset requires a 200 MHz system clock be provided to the P64H2 components.

5.3 Clock Outputs

For the downstream Hub Interface components, the SIOH provides external 66 MHz and 33 MHz clock outputs, with the 66 MHz clock in phase with the reference clock, and the 33 MHz delayed from the 66 MHz output by 1 to 3.5 ns. The SIOH also provides 266 MHz and 533 MHz source-synchronous clock outputs that are in-phase with the reference. The 33 MHz external clock is the only clock signal NOT guaranteed to rise when the synchronization signal indicates rising edge alignment, due to its lower frequency.

5.4 Feedback and Matching

The external 66 MHz clock output also serves as a feedback path to the PLL in the external Hub Interface clock unit. The path from the pad of the external clock and the feedback off of the external clock tree to the clock unit must be matched. The delay of all output legs should be matched. This will put all external devices in-phase with the reference clock and the Hub Interface internal clocks. The external feedback must be matched to the distribution to the P64H2s and ICH4. Mismatches will degrade or break I/O timings.

5.5 JTAG Test Access Port

Logic circuits exist in the JTAG unit to accommodate metastability and synchronization of TCK to SIOH core clocks for private instructions. Two synchronizers are used to provide rising and falling edge detection of the JTAG clock.

5.6 SMBus Clocking

Logic circuits exist in the SIOH to accommodate metastability and synchronization of the serial clock line (SCL) and the serial data line (SDA) to the SIOH core clocks for processing serial data streams. Also included is a 4-bit counter to suppress glitches less than 60 ns in width.

5.7 Spread Spectrum Support

Spread Spectrum Clocking (SSC) is a frequency modulation technique for EMI reduction. Instead of maintaining a constant frequency, SSC modulates the clock frequency/period along a predetermined path (i.e. the modulation profile), with a predetermined modulation frequency.

The chipset supports SSC. The modulation will be done with a frequency modulation of 30 kHz with a downspread of 0.5%.

5.8 No Stop Clock or Thermal Shutdown

Clocks in the SIOH can not be stopped. There are no power reduction features in the SIOH. However, the E8870 chipset does support power reduction features through other components such as the processor and ICH4.

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5.9　Deterministic Systems

In any SIOH system, the core clock and all SP clocks will be deterministic by default, since they are generated off of the 200 MHz system clock and their frequencies are either equal to that 200 MHz, or a multiple of it.

The external CLK33 is CLK66 divided by two. The divider is non-deterministic, so this clock could be non-deterministic as well. It is pointless to clear this divider at the determinism synch-point, since CLK66 will subsequently lose lock, and the 33 MHz phase will not be deterministic when lock is regained.

The phase of this signal can still be made deterministic by creating a reference pulse every sixth 200 MHz clock. After the synchronizing event, this pulse occurs at the same time as every other pulse used to qualify 200 MHz edges for comparison with CLK66. If the 33 MHz clock is ever high on the rising edge of the 200 MHz core clock qualified by the divide-by-6, the 33 MHz clock will be inverted, thus generating a deterministic CLK33. To ensure the proper operation of this scheme, the external trace delay of CLK66 (also CLK33) must be no longer than 8 ns from the point where it leaves the SIOH to its point of delivery.

The above synchronization is not performed if the DET pin is strapped low.

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Reset 6

6.1 Reset Sequence Overview

The following sections describe the power-up and reset sequences illustrated in Figure 6-1. The timing parameters are listed in Table 6-1.

Figure 6-1. SIOH Reset Sequence
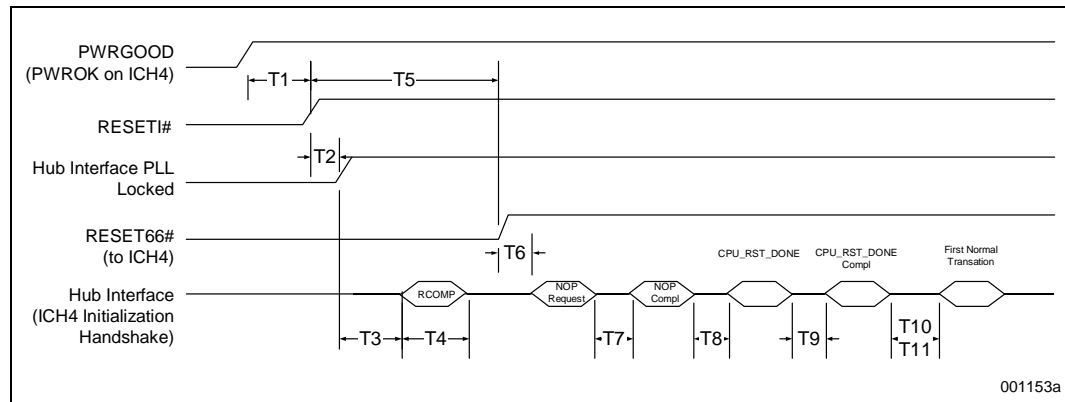
Table 6-1. Power-Up and Hard Reset Timings

	Description	Min	Max	Unit	Comments
T1	PWRGOOD assertion to RESETI# deassertion.	1	2	ms	PWRGOOD is asserted by the system.
T2	RESETI# deassertion to Hub Interface PLL locked.	0	1000	SYSCLK	Applies only to first RESETI# deassertion when DET is asserted.
T3	First RESETI# deassertion to start of initial Hub Interface RCOMP.	1024		SYSCLK	A 10-bit counter from PWRGOOD initiates the first RCOMP. Subsequent resets will not affect the periodic RCOMP and this initial RCOMP is not generated.
T4	Hub Interface RCOMP sequence.	0	T5-T3	SYSCLK	
T5	RESETI# complete to RESET66# deassertion.	4002	4007	SYSCLK	
T6	RESET66# deassertion to NOP request.	16	20	CLK66	Hub Interface 2.0 requires a minimum of 16 clocks. For the ICH4 there is no requirement.
T7	NOP request to NOP completion.	0	32	CLK66	ICH4 specification. When NOP returns, HLCTL[8] set.
T8	NOP completion to CPU_RST_DONE request.	0	10	CLK66	No ICH4 requirement.
T9	CPU_RST_DONE request to CPU_RST_DONE completion.	0	32	CLK66	ICH4 specification.
T10	CPU_RST_DONE completion to first valid outbound transaction.	0	N/A	CLK66	No ICH4 requirement.
T11	CPU_RST_DONE completion to first valid inbound transaction.	16	N/A	CLK66	SIOH requirement.

6.2 Power-Up Sequence

When the SIOH sees PWRGOOD asserted, it begins a power-up sequence. PWRGOOD is typically initiated by system power supplies or local DC/DC converter circuits. PWRGOOD resets all system components to a known reset state (except for some battery back-up circuits). PWRGOOD clears all sticky bits.

6.2.1 PWRGOOD Deasserted

The SIOH asserts RESET66# asynchronously.

Internal clocks will not be within specifications while PWRGOOD is deasserted and, therefore, must be treated as asynchronous. All E8870 chipset components will reset any core logic that can be asynchronously reset, and all logic must be forced into a non-destructive state. For example, multiple drivers must not attempt to drive the same signal to different logic values. JTAG chains and any logic clocked by TCK should be cleared. The TAP will not be operational until PWRGOOD is asserted. TCK may or may not be active at this time. All outputs (except for any reset outputs) are placed in a high impedance state.

6.2.2 PWRGOOD Assertion

RESETI# must be asserted by the system for 1 ms after PWRGOOD rises to allow E8870 chipset PLLs to lock. All logic in E8870 chipset components may be reset while RESETI# is asserted the first time after PWRGOOD. Fuse bits are sensed and parallel loaded during PWRGOOD assertion. Fuse bit download that requires sequential operation is not performed at this point as internal clocks are not stable. Clocks stabilize at some point before RESETI# rises, so the parallel loaded fuse information is valid by the time RESETI# rises. Public JTAG chains and any logic clocked by TCK must be operational (even though RESETI# is still asserted). Private JTAG chains need not be operational while RESETI# is asserted.

All logic reset by PWRGOOD may be held in reset until Hard Reset Deassertion.The SIOH drives RESET66# asynchronously to CLK66 to reset Hub Interface devices.

6.2.3 First RESETI# Deassertion

The SIOH continues to assert RESET66# (see Figure 6-1). The SIOH resets all clocks lower than 200 MHz on the synchronization point created by first RESETI# deassertion.

Sticky configuration bits are cleared, and a Hard Reset Deassertion sequence is started to initialize all SIOH states (see Section 6.3.2, "Hard Reset Deassertion"). When RESETI# is deasserted, reset straps (e.g. NodeID and BusID) are sampled and latched.

6.3 Hard Reset

Hard Reset is triggered by setting the SIOH reset bit in the SYRE register or RESETI# assertions. For resets initiated with the SIOH SYRE register, Hard Reset of the SIOH is delayed until T5 after SYRE[0] is set. This allows the configuration write to the SYRE register to complete back to the initiator before the SIOH state machines are reset.

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The SIOH behaves the same for all types of Hard Reset. (There is no difference in the SIOH response to a Local or Domain Hard Reset.) Since a Hard Reset Assertion response and a Hard Reset Deassertion response always occur together in the SIOH, they may be combined into a single flow.

6.3.1 Hard Reset Assertion

All logic reset by PWRGOOD may be held in reset between Hard Reset Assertion and Hard Reset Deassertion. Sticky configuration bits are not cleared. RESET66# is driven by the SIOH synchronous to CLK66 to reset Hub Interface devices.

6.3.2 Hard Reset Deassertion

After RESET66# deasserts synchronous to CLK66, the SIOH begins a CPU_RESET_DONE handshake with the ICH4:

1. SIOH is done with reset (deassertion of RESET66# and PWRGOOD).

2. Send a NOP transaction down the ICH4 Hub Interface. If no completion is received for the NOP transaction (normal or unsupported special cycle), HLCTL[8] is not set and any subsequent transactions targeting the Hub Interface will be master-aborted.

3. If a completion is received for the NOP transaction, issue a CPU_RST_DONE special cycle to the ICH4.

4. After the SIOH receives the CPU_RST_DONE completion (normal or Unsupported Special Cycle) the SIOH remains idle and begins normal operation. HLCTL[8] for function 0 is set, indicating a present Hub Interface component.

While the SIOH reset sequence is being performed the SIOH cannot issue other transactions to the ICH4.

For a waveform illustrating the above sequence, refer to Figure 6-1.

All other logical outputs of the SIOH should be deterministic from Hard Reset. That is, all storage elements in IOs, PLLs, and synchronous logic (except for sticky configuration bits) should be cleared by Hard Reset. During the Hard Reset sequence, any logic feeding into sticky configuration bits should not change the state of those bits.

Hard Reset Deassertion also invalidates all the read caches, the write cache, LRB, RRB, and all queues throughout the SIOH component.

6.3.3 Non-Existent Hub Interface Devices

It is possible that the SIOH could have Hub Interface 2.0 ports that are not populated by any components. When RESETI# is deasserted, the SIOH samples REQ# on the Hub Interface 2.0 ports. If no component exists, then HLCTL[8] is not set. Once presence is detected, the HLCTL[2] default value is set appropriately. Any further transactions targeting a disabled interface are master aborted.

Note: The default state of the Hub Interface enable bits (HLCTL[2]) is determined by whether a Hub Interface device is detected on the port or not. Software could choose to override this default setting by enabling or disabling that port.

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6.3.3.1 Non-Existent ICH4

For a large system implementing two SIOH components, only one of the SIOHs will interface a ICH4 component. Therefore, the SIOH without an ICH4 will attempt the reset handshake and the NOP will never complete. The default state of HLCTL[2] for function 0 is based on a successful or unsuccessful reset handshake. If the Hub Interface reset state machine completes normally, the interface is enabled. Otherwise, the interface remains disabled and any transactions targeting it are Master Aborted.

Note: The default state of the Hub Interface enable bits (HLCTL[2]) is determined on whether a Hub Interface device was detected on the port or not. Software could choose to override this default setting by enabling or disabling that port.

6.4 Reset Signals

This section describes the different reset signals interfacing the SIOH.

6.4.1 PWRGOOD

PWRGOOD will be deasserted as the voltage supplies come up, or may be pulsed after power-on to clear the system. Slew rate requirements are specified in Section 8.8, "Miscellaneous Signal Group" . The assertion of power-good signal indicates that external clocks and power at the SIOH is stable.

6.4.2 RESETI#

This pin is the Hard Reset input to the SIOH. It may be driven by the ICH4 PCIRST# signal or, if determinism is required, by system reset control logic.

6.4.3 RESET66#

This pin is asserted in combination, while RESETI# is asserted asynchronously after PWRGOOD assertion or if the Hard Reset bit is set in the SIOH SYRE register. RESET66# will rise synchronous to CLK66. This pin will be driven to the P64H2 RSTIN# pin, requiring voltage level translation from 1.5V to 3.3V.

6.4.4 DET

The DET pin is strapped high to enable determinism in the SIOH. If high, CLK33 and CLK66 references are reset on first Hard Reset Deassertion.

If this pin is low, the dividers that provide references for these clocks can come up at an arbitrary phase relative to the same clocks on other SIOHs and SNC memory maintenance operations.

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Reliability, Availability and Serviceability (RAS)   **7**

7.1   Data Integrity

Errors are classified into two basic types: fatal (or non-recoverable) and non-fatal (or recoverable).[1] Fatal errors include protocol errors, parity errors on header fields, time-outs, failed link-level retry, etc. For fatal errors, continued operation of the chipset may be compromised.

The SIOH can continue operations (transactions are completed, resources de-allocated, etc.) with non-fatal errors. Non-fatal errors are further classified into correctable and non-correctable errors. Non-correctable errors are those that are not "corrected" by the SIOH. Non-correctable errors may or may not be correctable by software. Correctable errors include single bit ECC errors, successful link level retry, and those transactions where the SIOH performs a *master abort* of the transaction.

The SIOH indicates an error condition on external pins. A pin (open drain) is provided for each error type (fatal, uncorrectable, and correctable). It is up to the system to decide what is the best course of action upon the detection of an error.

The SIOH provides error logging and error status for the first error detected by the component and error status for subsequent errors. Errors are detected and logged at intermediate entry points (on the inbound SP interface, for example). Errors are also detected and logged at the end points (where the packet is consumed or translated to another interface with different error coverage/detection). For data errors, the end-point is where the error is corrected or the data is poisoned[2]. This method of error correction and error logging is called *end-to-end* error correction.

The data that is logged and the name of the error log is also listed. Some errors may be detected in more than one component, as is the case for many of the SP related errors.

7.1.1   End-to-End Error Correction

ECC errors are passed along to the end point. If the data path does not have ECC all the way, single-bit errors will be corrected just before the first ECC-less interface. Intermediate interfaces will not correct single-bit ECC errors. The ECC check bits and parity check bits are always passed along with data internally. A typical error will leave a trail behind in each component it passes. The system can use this to pinpoint source of error and recover from error conditions.

The SIOH has the following end points for data:

Hub Interface 1.5

- Outbound data cycles:

  — If no ECC error, generate good parity.

  — If SBE, correct the error and generate good parity.

  — If MBE, generate bad parity.

---

1. These are hardware definitions used by the E8870 chipset, and are not the same error types that are used by software (MCA).
2. ECC data is poisoned by flipping ECC check bits 7:1, which will result in a syndrome value of 11111110. Parity data is poisoned by flipping all of the parity bits associated with the data. Parity data is poisoned by flipping the parity bit.

- Inbound data cycles:
    - — If no parity error, generate good ECC.
    - — If parity error, generate poisoned ECC.

PCI/PCI-X (performed by the P64H2)

- Outbound data cycles:
    - — If no ECC error, generate good parity.
    - — If SBE, correct the error and generate good parity.
    - — If MBE, generate bad parity.
- Inbound data cycles:
    - — If no parity error, generate good ECC.
    - — If parity error, generate poisoned ECC.

Configuration Registers

- Writes:
    - — If no ECC error, write the configuration register with data.
    - — If SBE, correct the error and write the configuration register with corrected data.
    - — If MBE, drop the write.
- Reads:
    - — Generate good ECC from the data.

Partial (unaligned to 8-byte boundary) Write Merge Buffers

- If no ECC error, merge the new data with the old and re-generate ECC.
- If SBE on one or more 8-byte chunks, correct errors, merge the new data with the old and re-generate ECC for the 8-byte chunks.
- If MBE on one or more 8-byte chunks, merge the new data with the old and poison the 8-byte chunks.

7.1.2   Error Reporting

The SIOH provides error status and logging registers that are specific to the E8870 chipset. The E8870 chipset specific registers are implemented in a similar manner across the chipset. In addition, the SIOH provides error status and log registers that are defined as part of the PCI standard interface. Below is a description of the E8870 chipset specific implementations. For details regarding the PCI specific registers, see the *PCI Local Bus Specification,* Revision 2.2.

7.1.2.1   Error Status and Log Registers

Error status registers are provided per component; FERRST (first error status register), and SERRST (second, or subsequent error status register). First fatal and/or first non-fatal errors are flagged in the FERRST register, subsequent errors are indicated in the SERRST. Associated with some of the errors flagged in the FERRST register are control and data logs. In some cases, the logs are duplicated for the same error (for example, two Hub Interfaces on the SIOH may have the same error log registers). When error logs are duplicated, a pointer to the cluster that reported the first error is provided.

The contents of FERRST and SERRST are "sticky" across a reset (where power remains good). This provides the ability for firmware to perform diagnostics across reboots. Note that only the contents of FERRST effects the update of the any error log registers.

To summarize, the rules for the FERRST and SERRST registers and error logs are as follows:

1. First fatal and first non-fatal (uncorrectable, correctable) errors are flagged in the FERRST. For example, if a correctable error has been flagged, and a fatal error is detected, the FERRST should be updated to indicated that a fatal error has been detected as well. Both errors will be flagged in the FERRST. At most two bits will be asserted in the FERRST.

2. If more than one fatal error is detected simultaneously, the error with the MSB in the FERRST will be selected. If more than one non-fatal error is detected, uncorrectable errors will be selected to be flagged before correctable errors. If two errors of the same sub-type are detected, the MSB algorithm is applied.

3. If more than one fatal error is detected simultaneously, one is selected to be flagged in the FERRST, the other is flagged in the SERRST. The same algorithm applies to non-fatal errors.

4. In the case where there are multiple duplicate log registers for an error, a pointer to the unit reporting the error is updated in FERRST.

5. FERRST, SERRST and error log registers are sticky across reset (where PWRGOOD remains asserted).

7.1.2.2   Error Signaling

Three open-drain error pins are associated with each of FERRST/SERRST registers, one for each error type: fatal, uncorrectable and correctable (ERR[2:0]# respectively). If not masked (ERRMSK register), these pins will reflect the error status of each type in the two error status registers.

The value of the error pins when an error is flagged is also stored in the FERRST to facilitate the identification of the first error in the system. For example, when a first fatal error detected on the component, the value of the error status pin associated with fatal errors is also latched into the FERRST.

For reliable signaling of errors in the system, each component guarantees that the pin associated with the error is asserted within four system clock cycles (200 MHz) after the error is detected by the component. For example, if a multi-bit ECC error is detected at the SP interface in cycle x, the uncorrectable error pin (ERR[1]#) is asserted in cycle x+3. The error pins are asynchronous I/O signals.

7.1.2.3   Error Logs

Control and/or data logs are provided for some errors. The "non-recoverable" error logs are used to log information associated with first fatal errors. The "recoverable" error logs are used for first non-fatal errors.

Once a first error for a type of error has been flagged (and logged), the log registers for that error type remain fixed until either 1) all bits associated with the error type in the FERRST are cleared, or 2) a power-on reset. More specifically, when the status bits associated with fatal errors are cleared in FERRST, updates to the non-recoverable error logs are enabled. When the status bits associated with non-fatal errors are cleared in FERRST, updates to the recoverable error logs are enabled.

7.1.3   Interface Details

Major interfaces in the chipset can be enabled/disable via software to aid fault isolation. Any requests routed to a disabled interface will be master-aborted. Any responses will be absorbed. That is, no issue is required on the disabled interface, but the disabled interface must not assert internal flow control.

Scalability Port

- Data is protected by ECC. ECC is checked only on entry of packets.

- Flits transfers are protected by parity.

- The information contained in the SP control and idle flits packet are protected by both parity and duplication (each field is duplicated on different wires to enhance error detection).

- Link level retry is supported on the SP. Link level retry is entered when parity errors are detected on flits, or when phits within an idle flit have a duplication error.

- Whenever the SIOH returns a Master Abort status, a PCMP_D completion is returned where the data length is zero. In the case where the SIOH receives a *failed* response status, the error is reported immediately to FERRST/SERRST but the transaction continues as if the completion was normal. When a *failed* response status is received, the transaction may not be able to complete. (For instance, a PRIL may receive the data, but never the PCMP due to the failure).

Hub Interface 2.0 Interfaces

- Protected by ECC:

  — ECC checking disabled with HLCTL.

- Inbound transactions that receive a failed response are discarded. A Target Abort will be returned to the initiator with enough data phases to match the initial request.

- Special cycle errors are logged by the SIOH.

Hub Interface 1.5 Interfaces

- 1 parity bit per 32-bit data:

  — Parity checking disabled with HLCTL.

- Special cycles will be logged by SIOH.

- Inbound transactions with fatal errors are discarded. A hard fail completion packet will be returned to the initiator.

- Outbound transactions that encounter fatal errors like target abort should be terminated with hard fail completion (needs support from ICH4).

PCI-X/PCI

- Parity bits are generated and checked independently for each PCI bus:

  — Parity checking disabled with PCICMD.

- Standard PCI checking for aborts, PERR# and SERR# are also done.

- Parity errors or aborts can be configured to assert SERR# special cycles on Hub Interface. The SIOH will log the SERR cycles and assert its error pins.

- Upon receiving hard fail completion from Hub Interface, the failed transaction on PCI-X/PCI will be terminated with target abort (needs support from P64H2 and ICH4).

Configuration Register

- ECC is checked on configuration writes.

Partial Write Merge Buffer

- ECC is checked before the merge.

SMBus

- The SMBus port supports the optional Packet Error Correction feature of *SMBus Specification*, Revision 2.0. This feature allows the slave to append an 8-bit CRC to read completions.

7.1.4   Time-Out

When an entry in the LRB is allocated, it becomes valid and is tracked by the master timer logic. The timer is a 24-bit wrap-around counter, incrementing at 25 MHz (200 MHz core clock divided by 8).The time-out period is programmable (a value in the ERRCOM register that determines the size of the counter). The timer interval must be greater than the worst case latency required in the system to de-allocate the queue entry. For example, the LRB interval must be set to greater than the worst case latency from the SP issue to the response, including contention scenarios for all resources the request must acquire.

An entry times-out if the counter wraps around (toggles the high-order) bit twice. As a result, the time-out period can be from 1x to 2x the timer value.

It is possible for multiple entries in a queue to time-out simultaneously. When a time-out occurs, the hardware selects one entry as the "first error" for logging. The presence of more than one error is indicated in the SERRST registers.

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Electrical Specifications **8**

8.1 Non-Operational Maximum Rating

The absolute maximum non-operational DC ratings are provided in Table 8-1. Functional operation at the absolute maximum and minimum ratings is neither implied nor guaranteed. The SIOH should not receive a clock while subjected to these conditions. Functional operating conditions are given in the AC and operational DC tables. Furthermore, although the SIOH contains protective circuitry to resist damage from static discharge, one should always take precautions to avoid high static voltages or electric fields.

Table 8-1. Absolute Maximum Non-Operational DC Ratings at the Package Pin

Symbol	Parameter	Min	Max	Unit	Notes
Tstorage	SIOH Storage Temperature	−10	45	°C	
Vcc (All)	SIOH Supply Voltages with Respect to Vss	−0.50	Operating voltage + 0.50	V	
Vcc (CMOS)	CMOS Buffer DC Input Voltage with Respect to Vss	−0.50	Vcc (CMOS) + 0.50	V	

8.2 Operational Power Delivery Specification

The SIOH power requirements are outlined in this section. All parameters in Table 8-2 are specified at the pin of the component package.

Table 8-2. Voltage and Current Specifications

Symbol	Parameter	Min	Typical	Max	Unit	Notes
Vcc15	Core Voltage	1.425	1.5	1.575	V	
ICC$_{Core}$	Core Current			12.6	A	a
dICC/dt$_{Core}$	Core Transient Slew Rate			2.0	A/ns	
Vccsp	Scalability Port Supply Voltage	1.209	1.30	1.391	V	b, c, d
Isp	Scalability Port Current			0.50	A	e, f
dIsp/dt	SP Transient Slew Rate			1.0	A/ns	g
Vcc18= Vth1	1.8 Supply Voltage	1.71	1.8	1.89	V	
Vcc18-I$_{CC}$= Ith1	1.8 Supply Voltage Transient Current			0.70	A	
dIvcc18=dIth1/dt	1.8 Supply Voltage Transient Slew Rate			1.00	A/ns	
Vcc33	3.3 Volt Supply	3.135	3.3	3.465	V	h
Vcc33-I$_{CC}$	3.3 Volt Transient Supply Current			0.10	A	

a. The maximum ICC current is the worst case specification, (i.e. Vcc max, low temperature and application mix) intended for power supply design.
b. Vccsp budget is ±3% DC, and (DC + AC) at ±7% noise delivered at the pin.

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c. The power pins are separated at the package from the Vcc core or other supplies on-die.
d. The power supply must be local to each component. The SP power supply between two communicating ports needs to be separate.
e. The current requirement per scalability port (SP) port.
f. Under normal operating conditions. However, under certain test conditions, Isp might exceed the specification.
g. The specification is per SP port at the package pin.
h. I²C circuitry does not contribute significantly to the 3.3V transient load.

8.3   Scalability Port (SP) Signal Group

The SP interface is a source-synchronous interface with coincident data and continuous strobe transmission. The data and strobe signals are launched simultaneously and are expected to arrive at the receiver with the same timing relationship to one another.

Each SP port consists of two strands that are further subdivided into two bundles. Each SP port consists of thirty-two data bits, four 4 ECC bits, two parity bits, two SSO coding bits, two link layer control (LLC) bits, four strobe pairs (eight signal pins), reserved pins, and eight reference voltage pairs (sixteen signal pins).

The simultaneous bi-directional (SBD) signaling can create conditions for three logic levels on the interconnect (0, 0.65, 1.3)V, depending on the data values driven from each end of the trace.

All SBD signals are terminated via on-die termination. The reference voltages are generated on die and are set to 1/4Vccsp and 3/4Vccsp, so no external logic is needed to generate these reference voltages.

Each SP voltage reference pin is required to be interlinked to the corresponding SP port.

Table 8-3 summarizes the signal grouping of the SP interface. The "x" in the signal names is replaced with the specific SP port on the SIOH (0 or 1).

Table 8-3. Scalability Port Interface Signal Group

Signal	Signal Description
SBD I/O	SPxAD[15;0],SPxBD[15;0], SPxASTBP[1:0], SPxASTBPN[1:0], SPxBSTBP[1:0], SPxBSTBPN[1:0], SPxAEP[2:0], SPxBEP[2:0], SPxALLC, SPxBLLC, SPxASSO, SPxBSSO
CMOS1.5 I/O OD[a]	SPxGPIO[1:0]
CMOS1.3 INPUT[a]	SPxPRES[a]
CMOS1.3 I/O	SPxSYNC[a]
Power/Other	Vccsp[b], Vss
Analog I/O[c]	SPxZUPD[1:0][d], SPxAVREFH[3:0], SPxBVREFH[3:0], SPxAVREFL[3:0], SPxBVREFL[3:0][e]
SP Analog Input	VCCASP[e], VSSASP

a. See Section 8.8 for "CMOS1.3" specifications.
b. Vccsp is to be supplied to the SP port externally. See Table 8-2.
c. Reference voltages are generated on-die.
d. SPxZUPD0 impedance update pins are connected through a 45-ohm, 1% resistor to Vccsp; SPxZUPD1 impedance update pins are connected through 45-ohm, 1% resistor to Vss.
e. PLL analog voltage for SP, connected on the motherboard to Vcc15 supply (1.5V nominal ±5%) through a filter network. See Section 8.8.

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8.4 Hub Interface 2.0 (HI 2.0) Signal Group

The HI 2.0 is a 16-bit source-synchronous interface. All signals are terminated on-die at the receiver end of the interface to Vss. Table 8-4 summarizes the HI 2.0 signal groups. Unless otherwise noted, all specifications are at the component die pad.

Note: The P64H2 and ICH4 Hub Interface specifications are published independently.

Table 8-4. Hub Interface 2.0 Signal Groups [a, b]

Signal Group	Type	Signal Description
Source-Synchronous I/O	iGTL+	HLxPD[17:0], HLxPSTRB[F,S], HLxPUSTRB[F,S]
Common Clock, Output	iGTL+	HLxRQout
Common Clock, Input	iGTL+	HLxRQin
Common Clock, IO	iGTL+	HLxSTOP, HLxIOH
Analog Input	iGTL+	HLxVswing[c], HLxVref[c], HLRcomp[d], VCCAHL[e], VSSAHL

a. iGTL+ means "inverted" GTL+.
b. The signal name x is replaced with the hub port number on the device (1-4) for SIOH.
c. Vref and Vswing are supplied on the motherboard.
d. Rcomp value is equal to [Zo * (Vcc-Vswing) /Vswing]. Zo = nominal HI 2.0 trace impedance; Vswing = 0.8V; Vcc = typical HI voltage = 1.5v for SIOH HI 2.0.
e. Connected to 1.5V ±5% on the motherboard.

8.4.1 Hub Interface 2.0 DC Specifications

Table 8-5. Hub Interface 2.0 DC Parameters [a, b, c]

Symbol	Parameter	Min	Max	Unit	Notes
Vcc	Driver Power Rail	1.425	1.575	V	
Vil	Input Low Voltage	−0.3	Vref − 0.1	V	d
Vih	Input High Voltage	Vref + 0.1		V	d
Vol	Output Low Voltage		0.05	V	e, f
Voh	Output High Voltage	Vswing − 0.05	Vswing +0.05	V	e, f
Ili	Input Leakage Current		100	μA	
Ilo	Output Leakage Current		100	μA	
Ioh	Output High Current	−19.6		mA	g
Cin	Input Capacitance		5	pF	
Cclk	Clock input Capacitance	5	8	pF	
ΔCin	Strobe to Data Capacitance Difference		±0.5	pF	

a. All specification are at the die pad.
b. Parameters apply to all inputs, outputs and I/O buffers.
c. All voltages are referenced to Vss.
d. Vil_{min} is a function of the process. Vih_{max} is not defined explicitly but is a function of Voh across the transmission line.
e. Vol@ 1mA. Voh@ (0.6/Zo) mA.
f. Vol_{min} and Voh_{max} are not valid DC operating points.
g. Measured as (Vswing +10%)/(Zo–10%).

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Table 8-6. Hub Interface 2.0 Reference Voltages [a, b, c, d, e]

Symbol	Parameter	Min	Typical	Max	Units	Notes
HLxVref	HI 2.0 Reference Voltage	0.343	0.35	0.357	V	[f]
HLxVswing	HI 2.0 Reference Swing Voltage	0.784	0.80	0.816	V	[f, g, h]

a. All specifications are at the die pad.
b. Resistor-divider chain implemented to generate reference and swing voltages should use less than 1k-ohm resistors in order to ensure the reference voltage tolerance is met over the input leakage specification.
c. All voltages are referenced to Vss and generated from VCC15.
d. Uncorrected noise must be controlled to less than 10% peak to peak of the swing. This tight tolerance is required in order to have enough noise margin for the incoming signal.
e. Based on a 1% divergent variation of resistive ladder. Numbers will additionally scale with Vcc variation.
f. Hub Interface 2.0 reference and swing voltage generation circuitry must be capable of supplying 500 µA while maintaining DC specifications.
g. Change to the Hub Interface specification requires reference swing voltage to be 0.8V.
h. This pin feeds a high impedance input requiring about 50mA of current.

8.5 Hub Interface 1.5 (HI 1.5) Signal Group

The 8-bit Hub Interface is designated as HL0 of the five Hub Interfaces supported on the SIOH.

8.5.1 HI 1.5 Signal Groups

The HI 1.5 is an 8-bit source-synchronous interface for data transfer. All signals are terminated on-die to Vss at the receiving end of the interface. Table 8-7 summarizes the signal groups for HI 1.5.

Table 8-7. Hub Interface 1.5 Signal Group [a, b]

Signal Group	Type	Signal
Source Synchronous, I/O	iGTL	HLPD[7:0]#, HLSTRB[S,F]#[c]
Common Clock, I/O	iGTL	HLSTOP#,HLPAR#
Common Clock, Output	iGTL	HL0RQOUT#[d]
Common Clock, Input	iGTL	HL0RQIN#[d]
Analog Input	NA	HL0RCOMP[e], HL0VSwing[f], HL0VREF[f]

a. HI 1.5 signals are all active high asserted on the bus.
b. iGTL means "inverted" GTL with receiver terminated through on die NMOS-resistors to Vss.
c. Strobes are defined as HLSTRBF (first) and HLSTRBS (second).
d. The HL0RQIN# signal of the SIOH will connect to the RQOUT# signal of the opposing chip and vice versa.
e. Please see Section 8.6.1. for RCOMP details.
f. Reference and swing voltages are supplied from the motherboard.

8.5.2 Hub Interface 1.5 DC Specifications

Table 8-8. Hub Interface 1.5 DC Signaling Specifications [a, b, c, d]

Symbol	Parameter	Min	Max	Units	Notes
Vcc	Driver Power Rail	1.71	1.89	V	
Vih	Input High Voltage	Vref+0.1	1.2	V	
Vil	Input Low Voltage	−0.3	Vref-0.1	V	
Voh	Output High Voltage	0.65	0.75	V	[e]

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Table 8-8. Hub Interface 1.5 DC Signaling Specifications (Continued) [a, b, c, d]

Symbol	Parameter	Min	Max	Units	Notes
Vol	Output Low Voltage		0.05	V	f
Ioh	Output High Current	16		mA	g
Cin	Input Capacitance		5	pF	
Cclk	Clock input Capacitance	5	8	pF	
ΔCin	Strobe to Data Capacitance difference		±0.5	pF	

a. All specifications are at the pin of the package.
b. All voltages are referenced to Vss.
c. Parameters apply to all inputs, outputs and I/O buffers.
d. All input and output signal levels must comply with the Vil min, ViH max specification.
e. Iout = $0.8/Z_{Target}$.
f. Iout = 1mA.
g. Measured at Voh = Vswing/50.

Table 8-9. SIOH Hub Interface 1.5 Reference Voltages [a, b, c, d, e]

Symbol	Parameter	Min	Typical	Max	Unit	Notes
HL0Vref	HI 1.5 Reference Voltage	0.343	0.35	0.357	V	f
HL0Vswing	HI 1.5 Reference Swing Voltage	0.784	0.8	0.816	V	f, g, h

a. All specifications are at the pin of the package.
b. Resistor-divider chain implemented to generate reference and swing voltages should use less than 1k-ohm resistors in order to ensure the reference voltage tolerance is met over the input leakage specification.
c. Vcc18 is the driver power supply from which both references are generated.
d. Uncorrected noise must be controlled to less than 10% peak to peak of the swing. This tight tolerance is required in order to have enough noise margin for the incoming signal.
e. This range accounts for 1% divergent variation of the reference voltage generation resistors. The reference voltage will, in addition, vary linearly with Vcc18.
f. The reference and swing voltage generation circuitry must be capable of supplying 500 uA while maintaining DC specifications.
g. Change to the Hub Interface specification reconnects HI 1.5 reference swing voltage to be 0.8V.
h. This pin feeds a high impedance input requiring about 50mA of current.

8.6 Analog Inputs

8.6.1 Hub Interface Impedance Compensation (RCOMP)

The RCOMP pin is to be connected through a resistor to the appropriate voltage rail to make impedance compensation possible. The value of the resistor changes depending on the characteristic impedance of the bus. See Table 8-10 for details.

Note: In all cases, use [1%-tolerance, 1/4 watt] or better resistors.

Table 8-10. Table of Values for the RCOMP Resistor

Component Interface	50-ohm Bus	60-ohm Bus	Tied To:
HI 2.0[a]	43.2	52.3	Vcc15
HI 1.5[b]	50	60	GND

a. HI 2.0 RCOMP = $[Z_0 * (VCC15 - Vswing) / Vswing]$. Z_O = nominal HI trace impedance; Vcc = typical HI voltage = 1.5v for SIOH HI 2.0.
b. HI 1.5 RCOMP = Z_O to GND. This is SIOH-dependent for HI 1.5 support. This requirement does not apply to the ICH4 component.

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8.6.2 Hub Interface Vref/Vswing Decoupling

Decoupling capacitors used for HI2.0 and HI1.5 Vref/Vswing decoupling must have low equivalent series resistance (ESR) and inductance (ESL). The Vref/Vswing generator and its decoupling must be placed close to the HI interface to derive the benefit of accurately capturing the effect of power supply variations.

Generic guidelines would be a 0.1 uF decoupling capacitor placed as close as possible to the Vref/Vswing generation resistor divider circuit, and a 0.001 uF bypass capacitor placed as close as possible to the Vref/Vswing pin.

If the Vref/Vswing divider is shared by multiple chips over a distance of greater than 1 inch, then each interface should have its own 0.001 uF bypass cap placed as close as possible to the Vref/Vswing pins. Noise coupling from other signals should be kept to less than 20 mV. The trace spacing around the Vref/Vswing signal should be a minimum of .025 inches (25 mils) or 5X the dielectric thickness (whichever is greater) to reduce the crosstalk and maintain signal integrity.

8.7 SMBus and TAP Signal Group

The SIOH shares the same SMBus and TAP signal groups as the SNC and SPS components of the E8870 chipset, and uses open-drain outputs and its own defined logic levels, which are different than CMOS logic levels.

The TAP connection input signals require external termination. No reference voltage is required for these signals.

The SMBus and TAP signals require termination to 3.3V and 1.5V on the motherboard, respectively.

For specifications for related components, or external tools that will interface with the SIOH, refer to that component's or tool's associated specification.

Table 8-11. SMBus and TAP Interface Signal Group [a]

Signal Group	Signal Description
SMBus (I/O)	SPDCLK, SPDDA, SCL, SDA
TAP (Input)	TCK, TDI, TMS, TRST#
TAP (Output)	TDO

a. I/O designations are with respect to the SIOH component.

Table 8-12. TAP Signal Terminations [a, b]

TCK	27-ohm to GND
TMS	39-ohm to Vcc
TDI[c]	150-ohm to Vcc
TDO, TDI	75-ohm to Vcc
TRST#	500- to 680-ohm to GND

a. Termination values for input pins are based on requirements of Intel's in-target probe. Requirements for other applications may differ.
b. All resistances are nominal with a tolerance allowance of ±5%.
c. This TDI pull-up value applies only to TDI inputs driven by Intel's in-target probe TAP controller.

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8.7.1　　SMBus and TAP DC Specifications

Table 8-13. TAP DC Parameters [a]

Symbol	Parameter	Min	Max	Unit	Notes
Vil	Input Low Voltage	-0.4	0.76	V	
Vih	Input High Voltage	1.16	1.8	V	
V_T-	Negative-going Threshold Voltage	0.76	1.03	V	[b]
V_T+	Positive-going Threshold Voltage	0.91	1.16	V	[b]
V_H	Hysteresis Voltage	130		mV	[b]
Vol	Output Low Voltage	0.34	0.49	V	[c]
I_{li}	Input Leakage Current		50	µA	[c]
I_{ol}	Output Low Current	12.7		mA	[c]

a. All specifications are at the pin of the package.
b. See Figure 8-1.
c. Measured with a 75-ohm ±10% test load to Vcc.
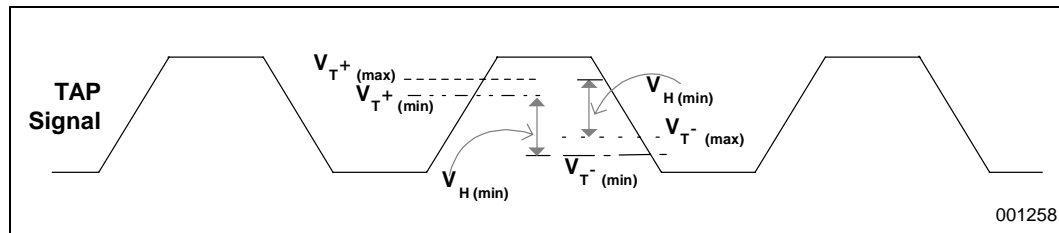
Figure 8-1. TAP DC Thresholds

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Table 8-14. SMBus DC Parameters [a, b]

Symbol	Parameter	Min	Max	Unit	Notes
Vil	Input Low Voltage	−0.5	0.8	V	
Vih	Input High Voltage	2.1	3.47	V	
Vol	Output Low Voltage		0.4	V	[c]
Ili	Input Leakage Current		50	µA	
Ipullup	Current through Pull-up Resistor	4.0		mA	
Cin	Input Capacitance		10	pF	
Vnoise	Signal Noise Immunity	300		mV	[d, e]

a. All specifications are at the pin of the package.
b. Parameters apply to SMBus inputs, outputs and I/O buffers.
c. At Vol max, Iol = 4 mA.
d. At 1 MHz to 5 MHz range.
e. Peak-to-peak.

8.7.2 SMBus and TAP AC Specifications

Table 8-15. SMBus Signal Group AC Specifications [a]

Symbol	Parameter	Min	Max	Unit	Notes
f_{smb}	Operating Frequency	10	100	kHz	
T60	SMBus Output Valid Delay		1.0	us	
T61	SMBus Input Setup Time	250		ns	
T62	SMBus Input Hold Time	300		ns	
T_r	Clock/Data Rise Time		1000	ns	b
T_f	Clock/Data Fall Time		300	ns	c
	Bus Free Time	4.70		us	d

a. All AC timings for the SMBus signals are referenced to the SM_CLK signal at 0.5 * SM_VCC at the package pins. All SMBus signal timings (SM_DAT, SM_ALERT#, etc.) are referenced at 0.5 * SM_VCC at the package pins.
b. $T_r = (V_{il,max}-0.15)$ to $(V_{ih,min}+0.15)$.
c. $T_f = (V_{ih,min}+0.15)$ to $(V_{il,max}-0.15)$.
d. Minimum time allowed between request cycles.

Table 8-16. TAP Signal Group AC Specifications [a]

Symbol	Parameter	Min	Max	Unit	Notes
	TCK Frequency	1.0	20	MHz	
T58	TCK, TMS, TDI Rise Time	0.5	16	ns	b
T59	TCK, TMS, TDI Fall Time	0.5	16	ns	c
	TDO Rise Time	2.3	4.6	ns	c
	TDO Fall Time	1.2	5.3	ns	c
T60	TDO Clock to Output Delay	2.5	10	ns	c
T61	TDI, TMS Setup Time	5		ns	d, e
T62	TDI, TMS Hold Time	18		ns	e
TRST#	Assert Time	300		ns	

a. All AC timings for the TAP signals are referenced to TCK at 50% voltage level.
b. Rise and fall times are measured from the 20% to 80% points of the signal swing.
c. Referenced to the falling edge of TCK.
d. Specification for a minimum swing defined between TAP V IL_MAX to V IH_MIN. This assumes a minimum edge rate of 0.5V per ns.
e. Referenced to the rising edge of TCK at the component pin.

8.7.3   SMBus and TAP AC Timing Waveforms

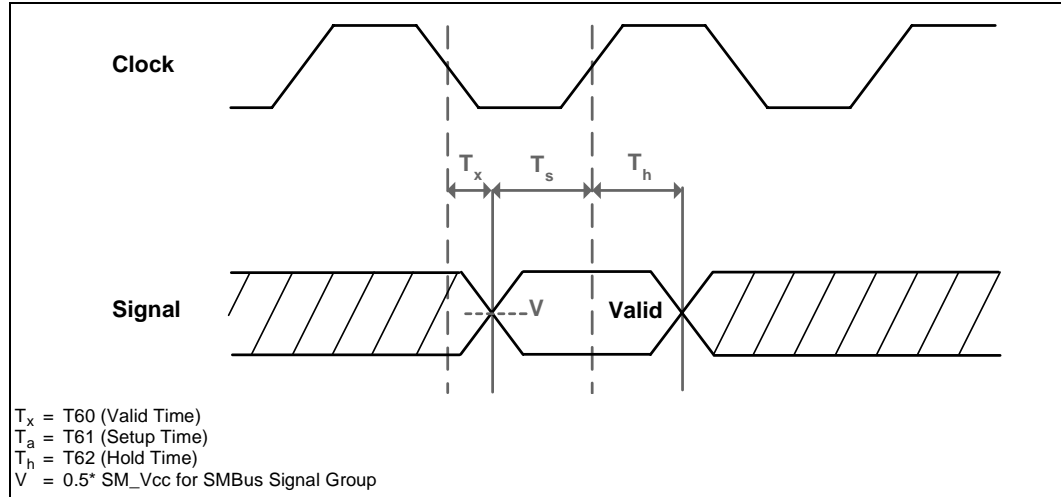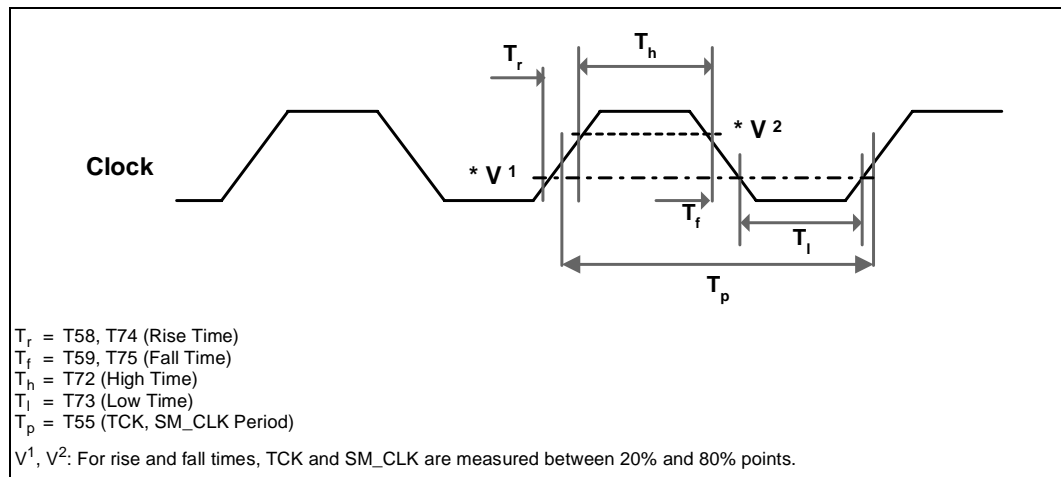**Figure 8-2. TAP and SMBus Valid Delay Timing Waveform**

T_x = T60 (Valid Time)
T_a = T61 (Setup Time)
T_h = T62 (Hold Time)
V   = 0.5* SM_Vcc for SMBus Signal Group

Figure 8-3. TCK and SM_CLK Clock Waveform

T_r = T58, T74 (Rise Time)
T_f = T59, T75 (Fall Time)
T_h = T72 (High Time)
T_l = T73 (Low Time)
T_p = T55 (TCK, SM_CLK Period)

V^1, V^2: For rise and fall times, TCK and SM_CLK are measured between 20% and 80% points.

8.8   Miscellaneous Signal Group

All buffer types that do not belong to one of the major buses in the system are listed as miscellaneous signals (refer to Table 8-17).

Table 8-17. Miscellaneous Signal Group

Signal Group	Signal Description
CMOS1.3 Input	SPxPRES
CMOS1.3 I/O	SPxSYNC
CMOS1.5 I/O OD	ERR[2:0]#, EV[3:0]#, SPxGPIO[1:0]
CMOS1.5 O OD	INT_OUT#

Table 8-17. Miscellaneous Signal Group (Continued)

Signal Group	Signal Description
CMOS1.5 Input	BUSID[2:0], LVHSTLODTEN, NODEID[4:0], PWRGOOD, RESETI#[a], DET
CMOS1.5 Output	RESET66#
ANALOG INPUT VCC	VREFFBCLK66, VCCACORE[b], VSSACORE

a. Requires external 330-ohm pull-up resistor.
b. PLL analog voltage input for core PLL, connect to 1.5V ±5% through a network filter.

Table 8-18. VREFFBCLK66 Reference Voltage [a, b]

Symbol	Parameter	Min	Typical	Max	Unit	Notes
Vreffbclk66	SIOH 66 MHz Feedback Clock V_{REF}	1.568	1.65	1.733	V	

a. All specifications are at the pin of the package.
b. Vreffbclk66 = Vcc33/2.

8.8.1   Miscellaneous Signal DC Specifications

Table 8-19. CMOS 1.3V DC Parameters [a, b]

Symbol	Parameter	Min	Max	Unit	Notes
Vil	Input Low Voltage	−0.3	0.35	V	
Vih	Input High Voltage	1.11	Vccsp + 0.3	V	
Vol	Output Low Voltage	−0.15	0.26	V	[c]
Voh	Output High Voltage	1.21	1.39	V	[c]
I_{li}	Input Leakage Current		10	µA	
Ron_p	On-Resistance P-device	300	700	ohms	
Ron_n	On-Resistance N-device	27	72	ohms	

a. All specifications are at the pin of the package.
b. Parameters apply to all CMOS 1.3V buffer types unless otherwise noted.
c. Parameters are not applicable to the "CMOS 1.3V Input" signal group.

Table 8-20. CMOS 1.5V Open Drain DC Parameters [a]

Symbol	Parameter	Min	Max	Unit	Notes
V_{IH}	Input High Voltage	1.15	Vcc + 0.3	V	
V_{IL}	Input Low Voltage	−0.3	0.70	V	
V_{oH}	Output High Voltage	1.3	Vcc + 0.3	V	[b]
V_{oL}	Output Low Voltage		0.54	V	[c]
I_{ol}	Output Low Current		52.0	mA	[c]
I_{li}	Input Leakage Current		50	µA	

a. Supply voltage at 1.5V ±5% tolerance.
b. RI = 50 or 25 Ohms.
c. RI = 25 Ohms.

Table 8-21. CMOS 1.5V DC Parameters [a]

Symbol	Parameter	Min	Max	Unit	Notes
V_{IH}	Input High Voltage	0.90	Vcc+0.3	V	
V_{IL}	Input Low Voltage	−0.30	0.50	V	
V_{oH}	Output High Voltage	0.8*Vcc	Vcc+0.3	V	
V_{oL}	Output Low Voltage		0.20*Vcc	V	
$V_{hysteresis}$	Hysteresis Voltage	0.10		V	
Ron	Output Impedance	30	80	ohms	
I_{li}	Input Leakage Current		70	µA	

a. Supply voltage at 1.5V ±5% tolerance.

8.8.2   Miscellaneous Signal AC Specifications

Table 8-22. CMOS 1.3V Open Drain AC Parameters [a]

Symbol	Parameter	Min	Max	Unit	Notes
Tco	Clock to Output Valid Delay	0.15	15.0	ns	
Tsu	Input Setup Time	N/A		ns	
Thold	Input Hold Time	N/A		ns	
SRf	Output Slew Rate Fall	0.25	0.7	V/ns	
SRr	Output Slew Rate Rise	0.5	15.0	V/ns	

a. Clock delay is in reference to the 200 MHz clock.

Table 8-23. CMOS 1.5V Open Drain AC Parameters [a, b, c]

Symbol	Parameter	Min	Max	Unit	Notes
Tco	Clock to Output Valid Delay	0.15	2.69	ns	[d, e]
Tsu	Input Setup Time	0.98		ns	
Thold	Input Hold Time	0.38		ns	
SRf	Output Slew Rate Fall	0.25	0.91	V/ns	[e]
SRr	Output Slew Rate Rise	0.37	1.18	V/ns	[e]
Signal: INT_OUT#					
Tco	Clock to Output Valid Delay		8.3	ns	

a. Supply voltage at 1.5V ±5% tolerance.
b. Clock delay is in reference to the 200 MHz clock.
c. Specification doesn't apply to signals EV[3:0]#, ERR[2:0]#, SPxGPIO[1:0]. See Table 8-25.
d. Specification doesn't apply to INT_OUT#.
e. RI = 25 ohms.

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Table 8-24. CMOS 1.5V Input AC Parameters [a, b]

Symbol	Parameter	Min	Max	Unit	Notes
Tco	Clock to Output Valid Delay	−0.28	1.44	ns	[c]
Tsu	Input Setup Time	0.84		ns	
Thold	Input Hold Time	0.35		ns	
SRf	Output Slew Rate Fall	2.00	5.00	V/ns	
SRr	Output Slew Rate Rise	1.90	4.9	V/ns	
Signal: RESET66#					
Tco	Clock to Output Valid Delay		1.7	ns	

a. Supply voltage at 1.5v ±5% tolerance.
b. Clock delay is in reference to the 200 MHz clock.
c. Specification doesn't apply to RESET66#.

Table 8-25. CMOS 1.5 I/O Open Drain AC Parameters

Symbol	Parameter	Min	Max	Unit	Notes
Signals: EV[3:0]#, ERR[2:0]#					
Tco	Clock to Output Valid Delay	1.9	5.2	ns	
Tsu	Input Setup Time	0.9		ns	
Thold	Input Hold Time	0.20		ns	
SRf	Output Slew Rate Fall	0.25	0.91	V/ns	
SRr	Output Slew Rate Rise	0.37	1.18	V/ns	
Signal: SPxGPIO[1:0]					
Tco	Clock to Output Valid Delay		6.7	ns	
Tsu	Input Setup Time	2.5		ns	
Thold	Input Hold Time	−2.0		ns	
SRf	Output Slew Rate Fall	0.25	0.91	V/ns	
SRr	Output Slew Rate Rise	0.37	1.18	V/ns	

8.9 Clock Signal Groups

Table 8-26. Clock Signal Groups

Signal Group	Signals
LVHSTL Differential Inputs	SYSCLK, SYSCLK#

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Table 8-27. LVHSTL Clock DC Parameters

Symbol	Parameter	Min	Typ	Max	Unit
V_{IH}	Input High Voltage	0.78		1.3	V
V_{IL}	Input Low Voltage	−0.3		0.5	V
V_X	Input Crossover Voltage	0.55		0.85	V
C_{CLK}	Input Capacitance	1.0		11.5	pF

8.9.1   AC Specification

Table 8-28. LVHSTL Differential Clock AC Specification

Symbol	Parameter	Min	Typ	Max	Unit	Notes
T_{period}	SYSCLK Period		5.0		ns	a
f_{BCLK}	SYSCLK Frequency	200		200	MHz	a, b
T_{jitter}	SYSCLK Input Jitter			100	ps	a, c
T_{high}	SYSCLK High Time	2.25	2.5	2.75	ns	a, d
T_{low}	SYSCLK Low Time	2.25	2.5	2.75	ns	a
T_{rise}	SYSCLK Rise Time	333	500	667	ps	a
T_{fall}	SYSCLK Fall Time	333	500	667	ps	a
V_{PP}	Minimum Input Swing		600		mV	a, e

a. See Figure 8-4.
b. Measured on cross point of rising edge of SYSCLK and falling edge of SYSCLK#. Long term jitter is defined as peak-to-peak variation measured by accumulating a large number of clock cycles and recording peak-to-peak jitter.
c. Long term jitter is defined as peak-to-peak variation measured by accumulating a large number of clock cycles and recording peak-to-peak jitter.
d. Measured on cross point of rising edge of SYSCLK and falling edge of SYSCLK#.
e. V_{PPmin} is defined as the minimum input differential voltage which will cause no increase in the clock receiver timing.

Figure 8-4. Generic Differential Clock Waveform

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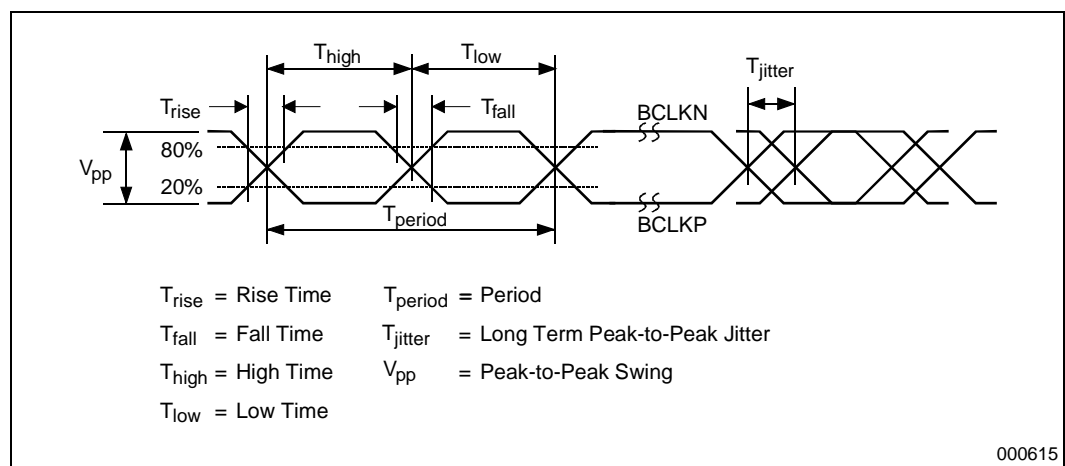
Package and Ballout   **9**

9.1   1012-Ball OLGA2b Package Information

The 1012-ball OLGA2b package of the SIOH has an exposed die mounted on a package substrate. The package's coplanarity has a mean of approximately 8-mils and a tolerance at 4-sigma of approximately 4-mils. A heatsink, with appropriate interface material and retention capabilities, is required for proper operation (refer to Figure 9-1 and Figure 9-2).

Figure 9-1. 1012-Ball OLGA2b Package Dimensions – Top View

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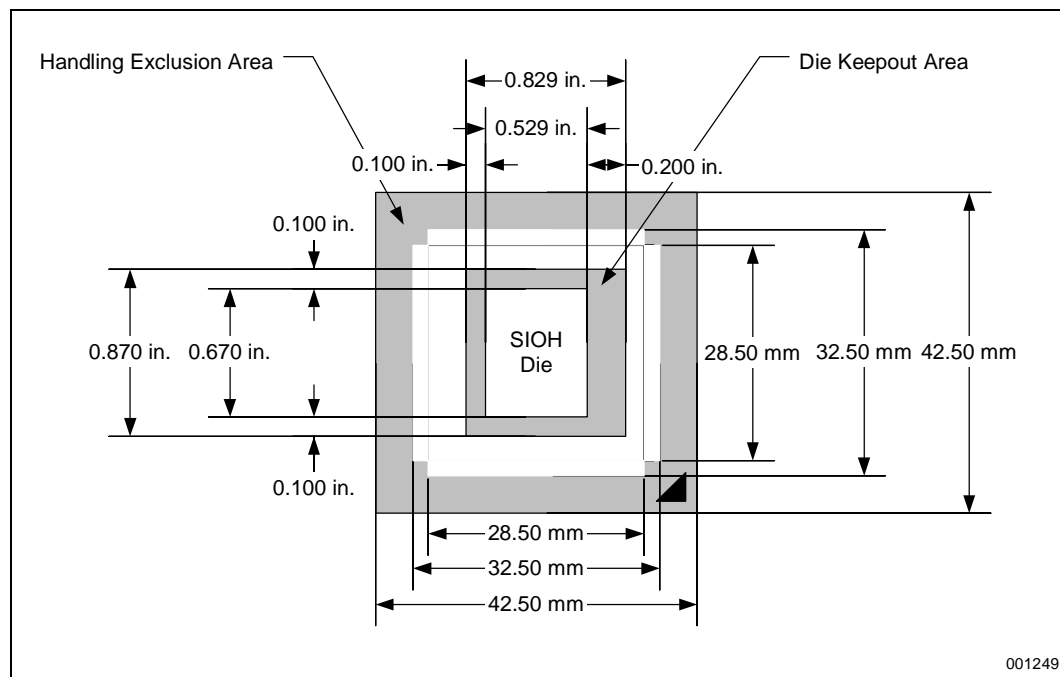
Figure 9-2. 1012-Ball OLGA2b Package Dimensions – Bottom View

NOTE: All dimensions are in millimeters.

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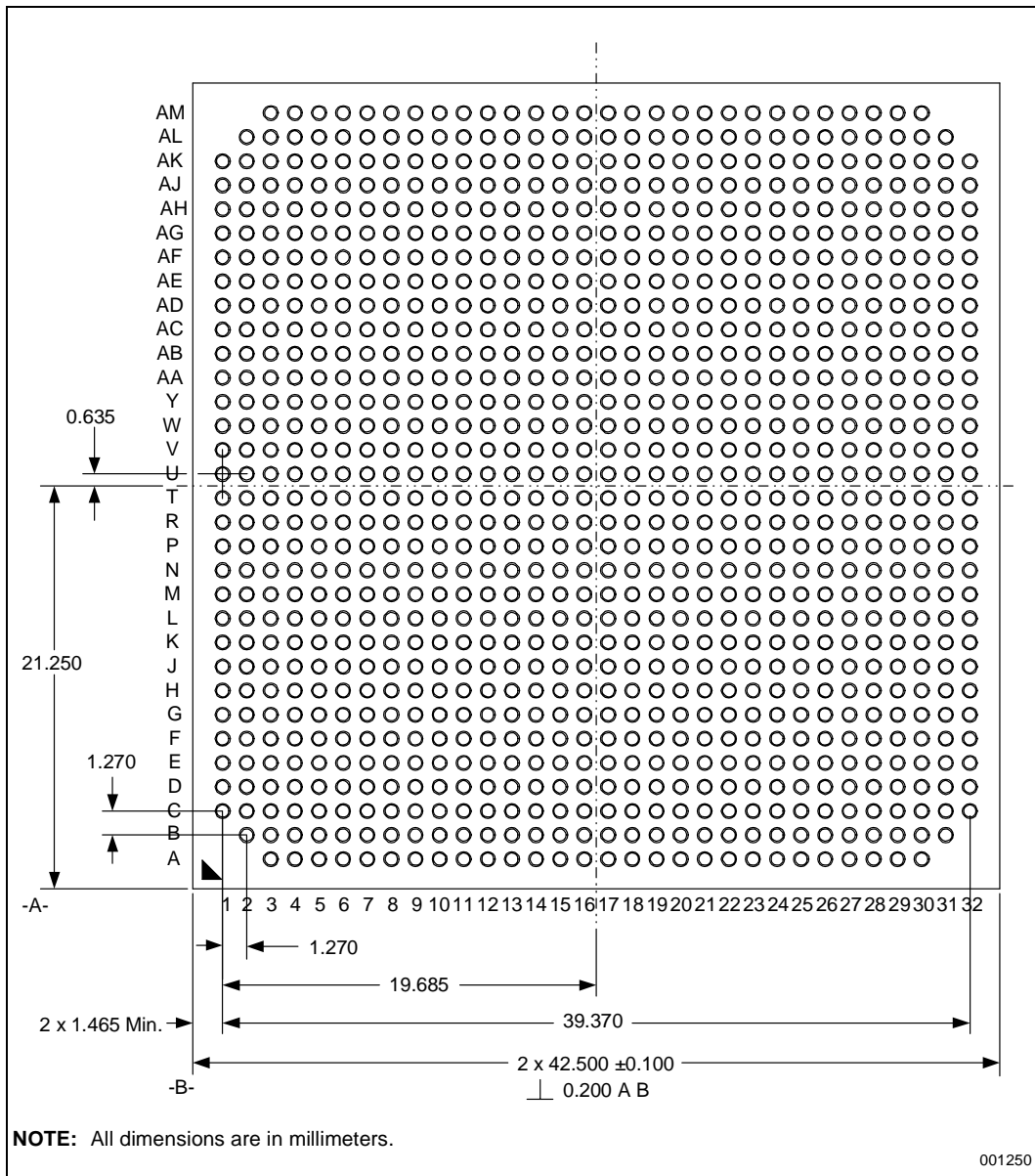
Figure 9-3. 1012-Ball OLGA2b Solder Ball Detail

NOTE: All dimensions are in millimeters.

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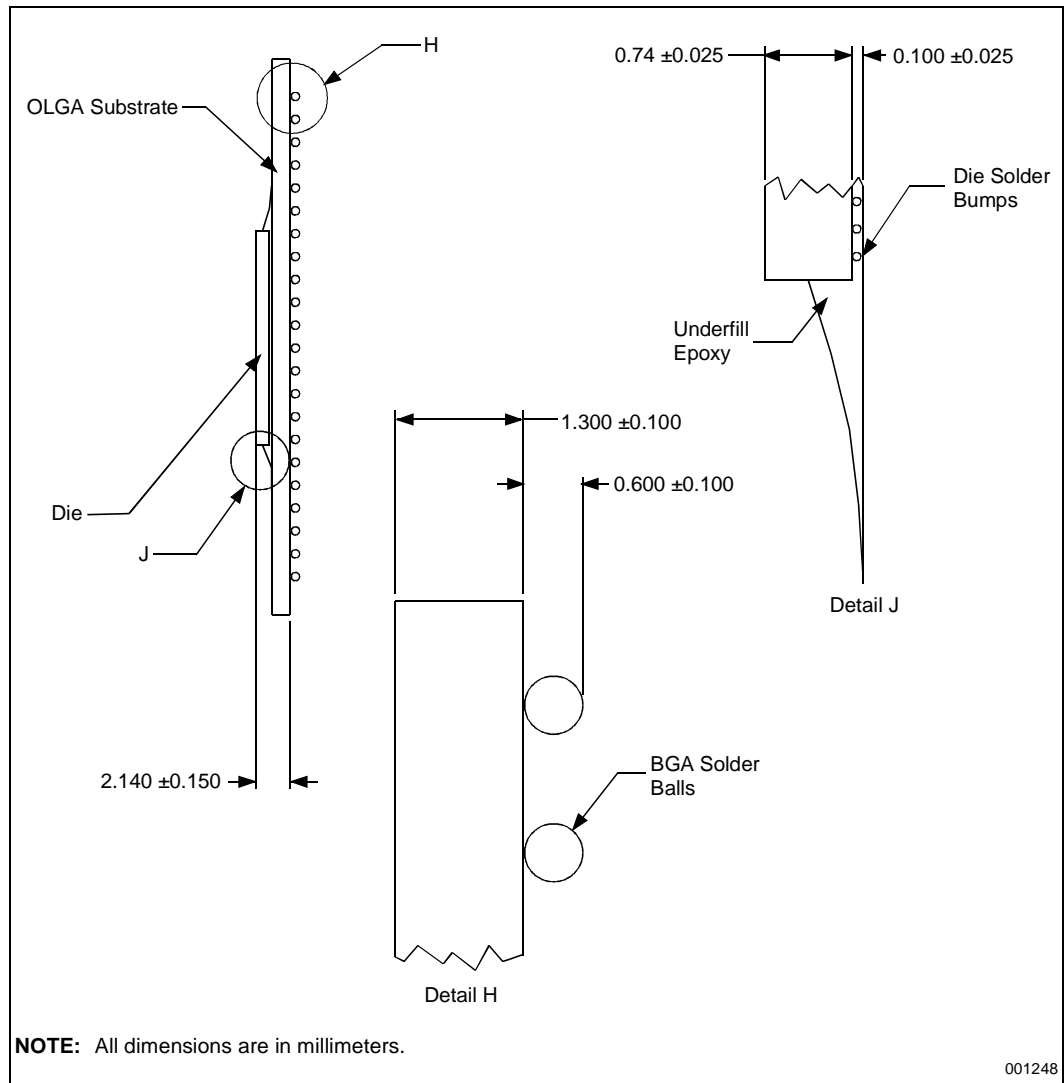
9.2 Ballout – Signal List

Table 9-1. SIOH Ball List

Ball Number	Signal		Ball Number	Signal
A3	Vss		B11	HL4PD[16]
A4	Vcc		B12	Vss
A5	Vss		B13	HL4PSTRBF
A6	HL4PD[15]		B14	Vss
A7	Vss		B15	HL4PD[2]
A8	HL4PUSTRBS		B16	Vss
A9	Vss		B17	HL0VREF[0]
A10	HL4PD[9]		B18	Vss
A11	Vcc		B19	HL0PSTRBF
A12	HL4PD[6]		B20	Vss
A13	Vss		B21	HL0PD[2]#
A14	HL4PD[4]		B22	Vss
A15	Vss		B23	SP1BD[14]
A16	HL4PD[0]		B24	Vccsp
A17	Vcc18		B25	SP1BVREFL[3]
A18	HL0PD[6]#		B26	Vss
A19	Vss		B27	SP1BVREFH[3]
A20	HL0PSTRBS		B28	Vccsp
A21	Vss		B29	SP1BD[11]
A22	HL0PD[0]#		B30	Vss
A23	Vss		B31	SP1BD[5]
A24	SP1BD[13]		C1	Vss
A25	Vss		C2	Vcc
A26	SP1BD[15]		C3	Vss
A27	Vss		C4	Vcc
A28	SP1BD[12]		C5	Vss
A29	Vss		C6	HL4PD[17]
A30	SP1BSSO		C7	Vss
B2	Vss		C8	HL4PUSTRBF
B3	Vcc		C9	Vss
B4	Vss		C10	HL4PD[10]
B5	Vcc		C11	Vcc
B6	Vcc		C12	HL4PD[7]
B7	HL4PD[13]		C13	Vss
B8	Vss		C14	HL4PSTRBS
B9	HL4PD[11]		C15	Vss
B10	Vss		C16	HL4PD[1]

Table 9-1. SIOH Ball List (Continued)

Ball Number	Signal		Ball Number	Signal
C17	>= 1k-ohm P/D		D24	Vss
C18	HL0PD[7]#		D25	SP1BSTBN[1]
C19	Vss		D26	Vccsp
C20	HL0PD[4]#		D27	SP1BSTBP[1]
C21	Vcc18		D28	Vss
C22	HL0PD[1]#		D29	SP1BVREFL[1]
C23	Vss		D30	Vccsp
C24	SP1BD[10]		D31	SP1BVREFH[1]
C25	Vss		D32	Vss
C26	SP1BRSVD		E1	HL3PD[0]
C27	Vss		E2	Vss
C28	SP1BD[6]		E3	HL3PD[1]
C29	Vss		E4	Vcc
C30	SP1BD[7]		E5	HL3RCOMP
C31	Vss		E6	HL4RQOUT
C32	SP1BD[4]		E7	Vcc
D1	Vcc		E8	HL4STOP
D2	Vss		E9	Vss
D3	Vcc		E10	HL4RQIN
D4	Vss		E11	Vss
D5	Vcc		E12	HL4VREF[1]
D6	Vss		E13	Vcc
D7	HL4PD[14]		E14	HL4VSWING
D8	Vss		E15	Vss
D9	HL4PD[12]		E16	HL4RCOMP
D10	Vss		E17	HL0RCOMP
D11	HL4PD[8]		E18	HL0STOP#
D12	Vss		E19	Vss
D13	HL4PD[5]		E20	HL0PAR#
D14	Vss		E21	Vss
D15	HL4PD[3]		E22	N/C
D16	Vcc		E23	Vss
D17	Vss		E24	SP1BD[9]
D18	Vcc18		E25	Vss
D19	HL0PD[5]#		E26	SP1BLLC
D20	Vss		E27	Vss
D21	HL0PD[3]#		E28	SP1BEP[0]
D22	Vss		E29	Vss
D23	330-ohm P/D		E30	SP1BD[3]

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Table 9-1. SIOH Ball List (Continued)

Ball Number	Signal	Ball Number	Signal
E31	Vss	G6	Vss
E32	SP1BD[2]	G7	N/C
F1	Vss	G8	Vss
F2	HL3PD[2]	G9	330-ohm P/D
F3	Vss	G10	N/C
F4	HL3PD[3]	G11	Vcc
F5	Vss	G12	N/C
F6	N/C	G13	DET
F7	Vss	G14	330-ohm P/D
F8	N/C	G15	Vcc
F9	HL4VREF[0]	G16	N/C
F10	LVHSTLODTEN	G17	330-ohm P/D
F11	CLK66	G18	N/C
F12	Vss	G19	Vss
F13	CLK33	G20	VCCACORE
F14	330-ohm P/D	G21	VSSACORE
F15	330-ohm P/D	G22	VssAHL
F16	Vss	G23	SP1SYNC
F17	HL0VSWING	G24	N/C
F18	HL0RQIN#	G25	Vss
F19	HL0RQOUT#	G26	SP1BD[8]
F20	Vcc18	G27	Vss
F21	HL0VREF[1]	G28	SP1BEP[2]
F22	Vcc18	G29	Vss
F23	SP1PRES	G30	SP1BD[1]
F24	Vccsp	G31	Vss
F25	SP1BVREFH[2]	G32	SP1BEP[1]
F26	Vss	H1	Vss
F27	SP1BVREFL[2]	H2	HL3PSTRBF
F28	Vccsp	H3	Vss
F29	SP1BSTBN[0]	H4	HL3PD[5]
F30	Vss	H5	Vcc
F31	SP1BSTBP[0]	H6	HL4VREF[2]
F32	Vss	H7	Vcc
G1	HL3PD[4]	H8	330-ohm P/D
G2	Vss	H9	330-ohm P/D
G3	HL3PSTRBS	H10	Vss
G4	Vss	H11	N/C
G5	HL3VSWING	H12	N/C

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Table 9-1. SIOH Ball List (Continued)

Ball Number	Signal
H13	330-ohm P/D
H14	Vss
H15	330-ohm P/D
H16	330-ohm P/D
H17	N/C
H18	Vss
H19	SYSCLK#
H20	VCCASP
H21	VssASP
H22	Vss
H23	SP1ZUPD[0]
H24	Vss
H25	SP1AD[8]
H26	Vccsp
H27	N/C
H28	Vss
H29	SP1BVREFH[0]
H30	Vccsp
H31	SP1BVREFL[0]
H32	Vss
J1	HL3PD[6]
J2	Vss
J3	HL3PD[7]
J4	Vss
J5	HL3VREF[1]
J6	Vss
J7	Vcc
J8	Vcc
J9	Vcc
J10	Vcc
J11	Vcc
J12	Vcc
J13	Vcc
J14	Vcc
J15	Vcc
J16	Vcc
J17	Vcc
J18	330-ohm P/D
J19	VCCAHL

Ball Number	Signal
J20	SYSCLK
J21	Vss
J22	FBCLK66
J23	Vss
J24	SP1AVREFL[2]
J25	Vss
J26	SP1AVREFH[2]
J27	Vss
J28	N/C
J29	Vss
J30	SP1BD[0]
J31	Vss
J32	SP1AD[0]
K1	Vcc
K2	HL3PD[16]
K3	Vcc
K4	HL3PD[8]
K5	Vss
K6	HL3VREF[0]
K7	Vcc
K8	Vss
K9	Vcc
K10	Vcc
K11	Vcc
K12	Vss
K13	Vcc
K14	Vcc
K15	Vcc
K16	Vss
K17	Vcc
K18	Vcc
K19	VCCACOM
K20	VCC33
K21	VssACOM
K22	VREFFBCLK66
K23	SP1ZUPD[1]
K24	Vccsp
K25	SP1ALLC
K26	Vss

Table 9-1. SIOH Ball List (Continued)

Ball Number	Signal
K27	SP1AD[9]
K28	Vccsp
K29	SP1AVREFL[0]
K30	Vss
K31	SP1AVREFH[0]
K32	Vss
L1	HL3PD[9]
L2	Vss
L3	HL3PD[10]
L4	Vss
L5	HL3RQIN
L6	Vss
L7	Vcc
L8	Vcc
L9	Vcc
L10	Vcc
L11	Vcc
L12	Vcc
L13	Vss
L14	Vcc
L15	Vss
L16	Vcc
L17	Vss
L18	Vcc
L19	Vss
L20	Vcc33
L21	Vss
L22	Vcc
L23	Vss
L24	SP1ASTBP[1]
L25	Vss
L26	SP1ASTBN[1]
L27	Vss
L28	N/C
L29	Vss
L30	SP1AEP[2]
L31	Vss
L32	SP1AD[1]
M1	Vss

Ball Number	Signal
M2	HL3PD[11]
M3	Vss
M4	HL3PD[12]
M5	Vss
M6	N/C
M7	Vcc
M8	Vss
M9	Vcc
M10	Vcc
M11	Vcc
M12	Vss
M13	Vcc
M14	Vss
M15	Vcc
M16	Vss
M17	Vcc
M18	Vss
M19	Vcc
M20	Vss
M21	Vcc
M22	Vss
M23	SP0PRES
M24	Vss
M25	SP1ARSVD
M26	Vccsp
M27	SP1AD[10]
M28	Vss
M29	SP1ASTBP[0]
M30	Vccsp
M31	SP1ASTBN[0]
M32	Vss
N1	HL3PUSTRBS
N2	Vss
N3	HL3PUSTRBF
N4	Vss
N5	HL3STOP
N6	N/C
N7	Vss
N8	Vcc

Table 9-1. SIOH Ball List (Continued)

Ball Number	Signal	Ball Number	Signal
N9	Vss	P16	Vss
N10	Vcc	P17	Vcc
N11	Vss	P18	Vss
N12	Vcc	P19	Vcc
N13	Vss	P20	Vss
N14	Vcc	P21	Vcc
N15	Vss	P22	Vss
N16	Vcc	P23	SP0SYNC
N17	Vss	P24	Vccsp
N18	Vcc	P25	SP1AVREFH[3]
N19	Vss	P26	Vss
N20	Vcc	P27	SP1AVREFL[3]
N21	Vss	P28	Vccsp
N22	Vcc	P29	SP1AVREFH[1]
N23	Vss	P30	Vss
N24	SP1AD[11]	P31	SP1AVREFL[1]
N25	Vss	P32	Vss
N26	SP1ASSO	R1	HL3PD[15]
N27	Vss	R2	Vcc
N28	SP1AEP[1]	R3	HL3PD[17]
N29	Vss	R4	Vss
N30	SP1AD[2]	R5	HL3RQOUT
N31	Vss	R6	N/C
N32	SP1AD[3]	R7	Vss
P1	Vss	R8	Vcc
P2	HL3PD[13]	R9	Vss
P3	Vss	R10	Vcc
P4	HL3PD[14]	R11	Vss
P5	Vcc	R12	Vcc
P6	Vss	R13	Vss
P7	Vcc	R14	Vcc
P8	Vss	R15	Vss
P9	Vcc	R16	Vcc
P10	Vss	R17	Vss
P11	Vcc	R18	Vcc
P12	Vss	R19	Vss
P13	Vcc	R20	Vcc
P14	Vss	R21	Vss
P15	Vcc	R22	Vcc

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Table 9-1. SIOH Ball List (Continued)

Ball Number	Signal
R23	Vss
R24	SP1AD[12]
R25	Vss
R26	SP1AD[15]
R27	Vss
R28	SP1AEP[0]
R29	Vss
R30	SP1AD[4]
R31	Vss
R32	SP1AD[7]
T1	Vss
T2	N/C
T3	Vss
T4	N/C
T5	HL3VREF[2]
T6	Vss
T7	Vcc
T8	Vss
T9	Vcc
T10	Vss
T11	Vcc
T12	Vss
T13	Vcc
T14	Vss
T15	Vcc
T16	Vss
T17	Vcc
T18	Vss
T19	Vcc
T20	Vss
T21	Vcc
T22	Vss
T23	SP0ZUPD[0]
T24	Vss
T25	SP1AD[13]
T26	Vccsp
T27	SP1AD[14]
T28	Vss
T29	SP1AD[6]

Ball Number	Signal
T30	Vccsp
T31	SP1AD[5]
T32	Vss
U1	HL2PD[0]
U2	Vss
U3	HL2PD[1]
U4	Vcc
U5	HL2RCOMP
U6	HL2VREF[0]
U7	Vss
U8	Vcc
U9	Vss
U10	Vcc
U11	Vss
U12	Vcc
U13	Vss
U14	Vcc
U15	Vss
U16	Vcc
U17	Vss
U18	Vcc
U19	Vss
U20	Vcc
U21	Vss
U22	Vcc
U23	Vss
U24	Vss
U25	SP0BD[13]
U26	Vccsp
U27	SP0BD[14]
U28	Vss
U29	SP0BD[6]
U30	Vccsp
U31	SP0BD[5]
U32	Vss
V1	Vss
V2	HL2PD[2]
V3	Vss
V4	HL2PD[3]

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Table 9-1. SIOH Ball List (Continued)

Ball Number	Signal	Ball Number	Signal
V5	Vss	W12	Vcc
V6	N/C	W13	Vss
V7	Vcc	W14	Vcc
V8	Vss	W15	Vss
V9	Vcc	W16	Vcc
V10	Vss	W17	Vss
V11	Vcc	W18	Vcc
V12	Vss	W19	Vss
V13	Vcc	W20	Vcc
V14	Vss	W21	Vss
V15	Vcc	W22	Vcc
V16	Vss	W23	Vss
V17	Vcc	W24	Vccsp
V18	Vss	W25	SP0BVREFH[3]
V19	Vcc	W26	Vss
V20	Vss	W27	SP0BVREFL[3]
V21	Vcc	W28	Vccsp
V22	Vss	W29	SP0BVREFH[1]
V23	SP0ZUPD[1]	W30	Vss
V24	SP0BD[12]	W31	SP0BVREFL[1]
V25	Vss	W32	Vss
V26	SP0BD[15]	Y1	Vss
V27	Vss	Y2	HL2PSTRBF
V28	SP0BEP[0]	Y3	Vss
V29	Vss	Y4	HL2PD[5]
V30	SP0BD[4]	Y5	Vcc
V31	Vss	Y6	N/C
V32	SP0BD[7]	Y7	Vcc
W1	HL2PD[4]	Y8	Vss
W2	Vss	Y9	Vcc
W3	HL2PSTRBS	Y10	Vss
W4	Vss	Y11	Vcc
W5	HL2VSWING	Y12	Vss
W6	Vss	Y13	Vcc
W7	Vss	Y14	Vss
W8	Vcc	Y15	Vcc
W9	Vss	Y16	Vss
W10	Vcc	Y17	Vcc
W11	Vss	Y18	Vss

Table 9-1. SIOH Ball List (Continued)

Ball Number	Signal
Y19	Vcc
Y20	Vss
Y21	Vcc
Y22	Vss
Y23	SP0GPIO[0]
Y24	SP0BD[11]
Y25	Vss
Y26	SP0BSSO
Y27	Vss
Y28	SP0BEP[1]
Y29	Vss
Y30	SP0BD[2]
Y31	Vss
Y32	SP0BD[3]
AA1	HL2PD[6]
AA2	Vss
AA3	HL2PD[7]
AA4	Vss
AA5	HL2VREF[1]
AA6	N/C
AA7	Vss
AA8	Vcc
AA9	Vss
AA10	Vcc
AA11	Vss
AA12	Vcc
AA13	Vss
AA14	Vcc
AA15	Vss
AA16	Vcc
AA17	Vss
AA18	Vcc
AA19	Vss
AA20	Vcc
AA21	Vss
AA22	Vcc
AA23	330-ohm P/D
AA24	Vss
AA25	SP0BRSVD

Ball Number	Signal
AA26	Vccsp
AA27	SP0BD[10]
AA28	Vss
AA29	SP0BSTBP[0]
AA30	Vccsp
AA31	SP0BSTBN[0]
AA32	Vss
AB1	Vcc
AB2	HL2PD[16]
AB3	Vcc
AB4	HL2PD[8]
AB5	Vss
AB6	N/C
AB7	N/C
AB8	Vss
AB9	Vss
AB10	Vcc
AB11	Vss
AB12	Vss
AB13	Vcc
AB14	Vss
AB15	Vcc
AB16	Vss
AB17	TDIOCATHODE
AB18	Vss
AB19	Vcc
AB20	Vss
AB21	Vcc
AB22	Vss
AB23	SP0GPIO[1]
AB24	SP0BSTBP[1]
AB25	Vss
AB26	SP0BSTBN[1]
AB27	Vss
AB28	N/c
AB29	Vss
AB30	SP0BEP[2]
AB31	Vss
AB32	SP0BD[1]

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Table 9-1. SIOH Ball List (Continued)

Ball Number	Signal
AC1	HL2PD[9]
AC2	Vss
AC3	HL2PD[10]
AC4	Vss
AC5	HL2RQIN
AC6	Vss
AC7	Vss
AC8	Vss
AC9	Vss
AC10	Vss
AC11	Vss
AC12	Vcc
AC13	Vss
AC14	Vss
AC15	Vss
AC16	Vss
AC17	SDA
AC18	Vcc
AC19	NODEID[0]
AC20	NODEID[1]
AC21	Vss
AC22	INT_OUT#
AC23	Vss
AC24	Vccsp
AC25	SP0BLLC
AC26	Vss
AC27	SP0BD[9]
AC28	Vccsp
AC29	SP0BVREFH[0]
AC30	Vss
AC31	SP0BVREFL[0]
AC32	Vss
AD1	Vss
AD2	HL2PD[11]
AD3	Vss
AD4	HL2PD[12]
AD5	Vss
AD6	HL2VREF[2]
AD7	Vss

Ball Number	Signal
AD8	Vcc
AD9	Vss
AD10	Vss
AD11	Vss
AD12	Vss
AD13	Vss
AD14	Vcc
AD15	Vss
AD16	SCL
AD17	Vss
AD18	330-ohm P/D
AD19	BUSID[2]
AD20	Vcc
AD21	N/C
AD22	300-ohm P/D
AD23	SP1GPIO[0]
AD24	SP0BVREFL[2]
AD25	Vss
AD26	SP0BVREFH[2]
AD27	Vss
AD28	N/C
AD29	Vss
AD30	SP0AD[0]
AD31	Vss
AD32	SP0BD[0]
AE1	HL2PUSTRBS
AE2	Vss
AE3	HL2PUSTRBF
AE4	Vss
AE5	HL2STOP
AE6	HL1VREF[0]
AE7	Vss
AE8	Vss
AE9	Vss
AE10	Vcc
AE11	300-ohm P/D
AE12	Vss
AE13	Vss
AE14	Vss

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Table 9-1. SIOH Ball List (Continued)

Ball Number	Signal	Ball Number	Signal
AE15	ERR#[1]	AF22	NODEID[3]
AE16	VCC33	AF23	Vss
AE17	Vss	AF24	N/C
AE18	EVBPOUT#	AF25	Vss
AE19	Vss	AF26	SP0AD[8]
AE20	N/C	AF27	Vss
AE21	NODEID[2]	AF28	SP0AEP[1]
AE22	Vcc	AF29	Vss
AE23	SP1GPIO[1]	AF30	SP0AD[1]
AE24	Vss	AF31	Vss
AE25	SP0BD[8]	AF32	SP0AEP[2]
AE26	Vccsp	AG1	HL2PD[15]
AE27	N/C	AG2	Vcc
AE28	Vss	AG3	HL2PD[17]
AE29	SP0AVREFH[0]	AG4	Vss
AE30	Vccsp	AG5	HL2RQOUT
AE31	SP0AVREFL[0]	AG6	N/C
AE32	Vss	AG7	N/C
AF1	Vss	AG8	Vcc
AF2	HL2PD[13]	AG9	N/C
AF3	Vss	AG10	HL1VREF[2]
AF4	HL2PD[14]	AG11	Vss
AF5	Vcc	AG12	ERR#[2]
AF6	Vss	AG13	BUSID[0]
AF7	330-ohm P/D	AG14	Vcc
AF8	300-ohm P/D	AG15	ITEST
AF9	Vss	AG16	330-ohm P/D
AF10	300-ohm P/D	AG17	Vss
AF11	Vss	AG18	RESETI#
AF12	Vcc	AG19	N/C
AF13	Vss	AG20	Vcc
AF14	ERR#[0]	AG21	N/C
AF15	Vss	AG22	N/C
AF16	TDIOANODE	AG23	NODEID[4]
AF17	BUSID[1]	AG24	Vccsp
AF18	Vcc	AG25	SP0AVREFH[2]
AF19	N/C	AG26	Vss
AF20	N/C	AG27	SP0AVREFL[2]
AF21	Vss	AG28	Vccsp

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Table 9-1. SIOH Ball List (Continued)

Ball Number	Signal		Ball Number	Signal
AG29	SP0ASTBN[0]		AJ4	Vss
AG30	Vss		AJ5	Vcc
AG31	SP0ASTBP[0]		AJ6	Vcc
AG32	Vss		AJ7	HL1PD[3]
AH1	Vss		AJ8	Vss
AH2	Vcc		AJ9	HL1PD[5]
AH3	Vss		AJ10	Vss
AH4	Vcc		AJ11	HL1PD[8]
AH5	Vss		AJ12	Vss
AH6	HL1RCOMP		AJ13	HL1PD[12]
AH7	Vss		AJ14	Vss
AH8	HL1VSWING		AJ15	HL1PD[14]
AH9	Vcc		AJ16	Vss
AH10	HL1VREF[1]		AJ17	TDI
AH11	Vss		AJ18	Vcc
AH12	HL1RQIN		AJ19	EV#[1]
AH13	Vss		AJ20	N/C
AH14	HL1STOP		AJ21	Vss
AH15	Vcc		AJ22	N/C
AH16	HL1RQOUT		AJ23	N/C
AH17	TDO		AJ24	Vss
AH18	TMS		AJ25	SP0ASTBN[1]
AH19	Vss		AJ26	Vccsp
AH20	N/C		AJ27	SP0ASTBP[1]
AH21	N/C		AJ28	Vss
AH22	Vcc		AJ29	SP0AVREFL[1]
AH23	EVBPIn#		AJ30	Vccsp
AH24	SP0AD[9]		AJ31	SP0AVREFH[1]
AH25	Vss		AJ32	Vss
AH26	SP0ALLC		AK1	Vss
AH27	Vss		AK2	Vcc
AH28	SP0AEP[0]		AK3	Vss
AH29	Vss		AK4	Vcc
AH30	SP0AD[3]		AK5	Vss
AH31	Vss		AK6	HL1PD[1]
AH32	SP0AD[2]		AK7	Vss
AJ1	Vcc		AK8	HL1PSTRBS
AJ2	Vss		AK9	Vss
AJ3	Vcc		AK10	HL1PD[7]

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Table 9-1. SIOH Ball List (Continued)

Ball Number	Signal	Ball Number	Signal
AK11	Vcc	AL21	N/C
AK12	HL1PD[10]	AL22	Vcc
AK13	Vss	AL23	SP0AD[14]
AK14	HL1PUSTRBF	AL24	Vccsp
AK15	Vss	AL25	SP0AVREFL[3]
AK16	HL1PD[17]	AL26	Vss
AK17	TSO	AL27	SP0AVREFH[3]
AK18	RESET66#	AL28	Vccsp
AK19	EV#[2]	AL29	SP0AD[11]
AK20	Vcc	AL30	Vss
AK21	N/C	AL31	SP0AD[5]
AK22	N/C	AM3	Vss
AK23	Vss	AM4	Vcc
AK24	SP0AD[10]	AM5	Vss
AK25	Vss	AM6	HL1PD[0]
AK26	SP0ARSVD	AM7	Vss
AK27	Vss	AM8	HL1PD[4]
AK28	SP0AD[6]	AM9	Vss
AK29	Vss	AM10	HL1PD[6]
AK30	SP0AD[7]	AM11	Vcc
AK31	Vss	AM12	HL1PD[9]
AK32	SP0AD[4]	AM13	Vss
AL2	Vss	AM14	HL1PUSTRBS
AL3	Vcc	AM15	Vss
AL4	Vss	AM16	HL1PD[15]
AL5	Vcc	AM17	TCK
AL6	Vss	AM18	Vcc
AL7	HL1PD[2]	AM19	EV#[3]
AL8	Vss	AM20	EV#[0]
AL9	HL1PSTRBF	AM21	Vss
AL10	Vss	AM22	N/C
AL11	HL1PD[16]	AM23	Vss
AL12	Vss	AM24	SP0AD[13]
AL13	HL1PD[11]	AM25	Vss
AL14	Vss	AM26	SP0AD[15]
AL15	HL1PD[13]	AM27	Vss
AL16	Vcc	AM28	SP0AD[12]
AL17	TRST#	AM29	Vss
AL18	PWRGOOD	AM30	SP0ASSO
AL19	Vss		
AL20	N/C		

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9.3 Signal – Ball Number List

Table 9-2. SIOH Signal – Ball Number

Signal	Ball Number
330-ohm P/D	G14
330-ohm P/D	F14
330-ohm P/D	F15
330-ohm P/D	H16
330-ohm P/D	AD18
330-ohm P/D	G9
330-ohm P/D	H8
330-ohm P/D	J18
330-ohm P/D	AE11
330-ohm P/D	AF8
330-ohm P/D	H13
330-ohm P/D	G17
330-ohm P/D	AD22
330-ohm P/D	AF10
330-ohm P/D	AF7
330-ohm P/D	D23
330-ohm P/D	H15
330-ohm P/D	H9
330-ohm P/D	AA23
330-ohm P/D	AG16
BUSID[0]	AG13
BUSID[1]	AF17
BUSID[2]	AD19
CLK33	F13
CLK66	F11
DET	G13
ERR#[0]	AF14
ERR#[1]	AE15
ERR#[2]	AG12
EV#[0]	AM20
EV#[1]	AJ19
EV#[2]	AK19
EV#[3]	AM19
EVBPIn#	AH23
EVBPOUT#	AE18
FBCLK66	J22
>= 1k-ohm P/D	C17

Signal	Ball Number
HL0PAR#	E20
HL0PD[0]#	A22
HL0PD[1]#	C22
HL0PD[2]#	B21
HL0PD[3]#	D21
HL0PD[4]#	C20
HL0PD[5]#	D19
HL0PD[6]#	A18
HL0PD[7]#	C18
HL0PSTRBF	B19
HL0PSTRBS	A20
HL0RCOMP	E17
HL0RQIN#	F18
HL0RQOUT#	F19
HL0STOP#	E18
HL0VREF[0]	B17
HL0VREF[1]	F21
HL0VSWING	F17
HL1PD[0]	AM6
HL1PD[1]	AK6
HL1PD[10]	AK12
HL1PD[11]	AL13
HL1PD[12]	AJ13
HL1PD[13]	AL15
HL1PD[14]	AJ15
HL1PD[15]	AM16
HL1PD[16]	AL11
HL1PD[17]	AK16
HL1PD[2]	AL7
HL1PD[3]	AJ7
HL1PD[4]	AM8
HL1PD[5]	AJ9
HL1PD[6]	AM10
HL1PD[7]	AK10
HL1PD[8]	AJ11
HL1PD[9]	AM12
HL1PSTRBF	AL9

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Table 9-2. SIOH Signal – Ball Number (Continued)

Signal	Ball Number		Signal	Ball Number
HL1PSTRBS	AK8		HL2VREF[2]	AD6
HL1PUSTRBF	AK14		HL2VSWING	W5
HL1PUSTRBS	AM14		HL3PD[0]	E1
HL1RCOMP	AH6		HL3PD[1]	E3
HL1RQIN	AH12		HL3PD[10]	L3
HL1RQOUT	AH16		HL3PD[11]	M2
HL1STOP	AH14		HL3PD[12]	M4
HL1VREF[0]	AE6		HL3PD[13]	P2
HL1VREF[1]	AH10		HL3PD[14]	P4
HL1VREF[2]	AG10		HL3PD[15]	R1
HL1VSWING	AH8		HL3PD[16]	K2
HL2PD[0]	U1		HL3PD[17]	R3
HL2PD[1]	U3		HL3PD[2]	F2
HL2PD[10]	AC3		HL3PD[3]	F4
HL2PD[11]	AD2		HL3PD[4]	G1
HL2PD[12]	AD4		HL3PD[5]	H4
HL2PD[13]	AF2		HL3PD[6]	J1
HL2PD[14]	AF4		HL3PD[7]	J3
HL2PD[15]	AG1		HL3PD[8]	K4
HL2PD[16]	AB2		HL3PD[9]	L1
HL2PD[17]	AG3		HL3PSTRBF	H2
HL2PD[2]	V2		HL3PSTRBS	G3
HL2PD[3]	V4		HL3PUSTRBF	N3
HL2PD[4]	W1		HL3PUSTRBS	N1
HL2PD[5]	Y4		HL3RCOMP	E5
HL2PD[6]	AA1		HL3RQIN	L5
HL2PD[7]	AA3		HL3RQOUT	R5
HL2PD[8]	AB4		HL3STOP	N5
HL2PD[9]	AC1		HL3VREF[0]	K6
HL2PSTRBF	Y2		HL3VREF[1]	J5
HL2PSTRBS	W3		HL3VREF[2]	T5
HL2PUSTRBF	AE3		HL3VSWING	G5
HL2PUSTRBS	AE1		HL4PD[0]	A16
HL2RCOMP	U5		HL4PD[1]	C16
HL2RQIN	AC5		HL4PD[10]	C10
HL2RQOUT	AG5		HL4PD[11]	B9
HL2STOP	AE5		HL4PD[12]	D9
HL2VREF[0]	U6		HL4PD[13]	B7
HL2VREF[1]	AA5		HL4PD[14]	D7

Table 9-2. SIOH Signal – Ball Number (Continued)

Signal	Ball Number	Signal	Ball Number
HL4PD[15]	A6	N/C	AK22
HL4PD[16]	B11	N/C	AK21
HL4PD[17]	C6	N/C	AJ20
HL4PD[2]	B15	N/C	E22
HL4PD[3]	D15	N/C	AG9
HL4PD[4]	A14	N/C	V6
HL4PD[5]	D13	N/C	Y6
HL4PD[6]	A12	N/C	AG6
HL4PD[7]	C12	N/C	AG7
HL4PD[8]	D11	N/C	AB6
HL4PD[9]	A10	N/C	G7
HL4PSTRBF	B13	N/C	R6
HL4PSTRBS	C14	N/C	M6
HL4PUSTRBF	C8	N/C	N6
HL4PUSTRBS	A8	N/C	F8
HL4RCOMP	E16	N/C	F6
HL4RQIN	E10	N/C	AD21
HL4RQOUT	E6	N/C	AA6
HL4STOP	E8	N/C	AB7
HL4VREF[0]	F9	N/C	AE27
HL4VREF[1]	E12	N/C	AF24
HL4VREF[2]	H6	N/C	G24
HL4VSWING	E14	N/C	H27
INT_OUT#	AC22	N/C	T2
ITEST	AG15	N/C	T4
LVHSTLODTEN	F10	N/C	H17
N/C	AE20	N/C	H12
N/C	AG22	N/C	H11
N/C	AF19	N/C	G16
N/C	AH20	N/C	G18
N/C	AM22	N/C	G10
N/C	AL21	N/C	G12
N/C	AL20	N/C	AD28
N/C	AG19	N/C	AB28
N/C	AG21	N/C	L28
N/C	AJ23	N/C	J28
N/C	AJ22	NODEID[0]	AC19
N/C	AF20	NODEID[1]	AC20
N/C	AH21	NODEID[2]	AE21

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Table 9-2. SIOH Signal – Ball Number (Continued)

Signal	Ball Number		Signal	Ball Number
NODEID[3]	AF22		SP0AVREFL[2]	AG27
NODEID[4]	AG23		SP0AVREFL[3]	AL25
PWRGOOD	AL18		SP0BD[0]	AD32
RESET66#	AK18		SP0BD[1]	AB32
RESETI#	AG18		SP0BD[10]	AA27
SCL	AD16		SP0BD[11]	Y24
SDA	AC17		SP0BD[12]	V24
SP0AD[0]	AD30		SP0BD[13]	U25
SP0AD[1]	AF30		SP0BD[14]	U27
SP0AD[10]	AK24		SP0BD[15]	V26
SP0AD[11]	AL29		SP0BD[2]	Y30
SP0AD[12]	AM28		SP0BD[3]	Y32
SP0AD[13]	AM24		SP0BD[4]	V30
SP0AD[14]	AL23		SP0BD[5]	U31
SP0AD[15]	AM26		SP0BD[6]	U29
SP0AD[2]	AH32		SP0BD[7]	V32
SP0AD[3]	AH30		SP0BD[8]	AE25
SP0AD[4]	AK32		SP0BD[9]	AC27
SP0AD[5]	AL31		SP0BEP[0]	V28
SP0AD[6]	AK28		SP0BEP[1]	Y28
SP0AD[7]	AK30		SP0BEP[2]	AB30
SP0AD[8]	AF26		SP0BLLC	AC25
SP0AD[9]	AH24		SP0BRSVD	AA25
SP0AEP[0]	AH28		SP0BSSO	Y26
SP0AEP[1]	AF28		SP0BSTBN[0]	AA31
SP0AEP[2]	AF32		SP0BSTBN[1]	AB26
SP0ALLC	AH26		SP0BSTBP[0]	AA29
SP0ARSVD	AK26		SP0BSTBP[1]	AB24
SP0ASSO	AM30		SP0BVREFH[0]	AC29
SP0ASTBN[0]	AG29		SP0BVREFH[1]	W29
SP0ASTBN[1]	AJ25		SP0BVREFH[2]	AD26
SP0ASTBP[0]	AG31		SP0BVREFH[3]	W25
SP0ASTBP[1]	AJ27		SP0BVREFL[0]	AC31
SP0AVREFH[0]	AE29		SP0BVREFL[1]	W31
SP0AVREFH[1]	AJ31		SP0BVREFL[2]	AD24
SP0AVREFH[2]	AG25		SP0BVREFL[3]	W27
SP0AVREFH[3]	AL27		SP0GPIO[0]	Y23
SP0AVREFL[0]	AE31		SP0GPIO[1]	AB23
SP0AVREFL[1]	AJ29		SP0PRES	M23

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Table 9-2. SIOH Signal – Ball Number (Continued)

Signal	Ball Number	Signal	Ball Number
SP0SYNC	P23	SP1BD[10]	C24
SP0ZUPD[0]	T23	SP1BD[11]	B29
SP0ZUPD[1]	V23	SP1BD[12]	A28
SP1AD[0]	J32	SP1BD[13]	A24
SP1AD[1]	L32	SP1BD[14]	B23
SP1AD[10]	M27	SP1BD[15]	A26
SP1AD[11]	N24	SP1BD[2]	E32
SP1AD[12]	R24	SP1BD[3]	E30
SP1AD[13]	T25	SP1BD[4]	C32
SP1AD[14]	T27	SP1BD[5]	B31
SP1AD[15]	R26	SP1BD[6]	C28
SP1AD[2]	N30	SP1BD[7]	C30
SP1AD[3]	N32	SP1BD[8]	G26
SP1AD[4]	R30	SP1BD[9]	E24
SP1AD[5]	T31	SP1BEP[0]	E28
SP1AD[6]	T29	SP1BEP[1]	G32
SP1AD[7]	R32	SP1BEP[2]	G28
SP1AD[8]	H25	SP1BLLC	E26
SP1AD[9]	K27	SP1BRSVD	C26
SP1AEP[0]	R28	SP1BSSO	A30
SP1AEP[1]	N28	SP1BSTBN[0]	F29
SP1AEP[2]	L30	SP1BSTBN[1]	D25
SP1ALLC	K25	SP1BSTBP[0]	F31
SP1ARSVD	M25	SP1BSTBP[1]	D27
SP1ASSO	N26	SP1BVREFH[0]	H29
SP1ASTBN[0]	M31	SP1BVREFH[1]	D31
SP1ASTBN[1]	L26	SP1BVREFH[2]	F25
SP1ASTBP[0]	M29	SP1BVREFH[3]	B27
SP1ASTBP[1]	L24	SP1BVREFL[0]	H31
SP1AVREFH[0]	K31	SP1BVREFL[1]	D29
SP1AVREFH[1]	P29	SP1BVREFL[2]	F27
SP1AVREFH[2]	J26	SP1BVREFL[3]	B25
SP1AVREFH[3]	P25	SP1GPIO[0]	AD23
SP1AVREFL[0]	K29	SP1GPIO[1]	AE23
SP1AVREFL[1]	P31	SP1PRES	F23
SP1AVREFL[2]	J24	SP1SYNC	G23
SP1AVREFL[3]	P27	SP1ZUPD[0]	H23
SP1BD[0]	J30	SP1ZUPD[1]	K23
SP1BD[1]	G30	SYSCLK	J20

Table 9-2. SIOH Signal – Ball Number (Continued)

Signal	Ball Number	Signal	Ball Number
SYSCLK#	H19	Vcc	AG2
TCK	AM17	Vcc	AG8
TDI	AJ17	Vcc	AG14
TDIOANODE	AF16	Vcc	AG20
TDIOCATHODE	AB17	Vcc	AH2
TDO	AH17	Vcc	AH4
TMS	AH18	Vcc	AH9
TRST#	AL17	Vcc	AH15
TSO	AK17	Vcc	AH22
Vcc	K18	Vcc	AJ1
Vcc	H7	Vcc	AJ3
Vcc	L11	Vcc	AJ5
Vcc	J7	Vcc	AJ6
Vcc	K7	Vcc	A4
Vcc	M11	Vcc	A11
Vcc	J11	Vcc	AA8
Vcc	K11	Vcc	AA10
Vcc	K15	Vcc	AA12
Vcc	J15	Vcc	AA14
Vcc	J12	Vcc	AA16
Vcc	J14	Vcc	AA18
Vcc	M7	Vcc	AA20
Vcc	L8	Vcc	AA22
Vcc	J10	Vcc	AB1
Vcc	K9	Vcc	AB3
Vcc	L9	Vcc	AB10
Vcc	M9	Vcc	AB13
Vcc	K10	Vcc	AB15
Vcc	M10	Vcc	AB19
Vcc	J8	Vcc	AB21
Vcc	L7	Vcc	AC12
Vcc	K14	Vcc	AC18
Vcc	K13	Vcc	AD8
Vcc	K17	Vcc	AD14
Vcc	J16	Vcc	AD20
Vcc	AE22	Vcc	AE10
Vcc	AF5	Vcc	E4
Vcc	AF12	Vcc	E7
Vcc	AF18	Vcc	E13

Table 9-2. SIOH Signal – Ball Number (Continued)

Signal	Ball Number	Signal	Ball Number
Vcc	G11	Vcc	R12
Vcc	G15	Vcc	R14
Vcc	H5	Vcc	R16
Vcc	J9	Vcc	R18
Vcc	J13	Vcc	R20
Vcc	J17	Vcc	R22
Vcc	K1	Vcc	T7
Vcc	K3	Vcc	T9
Vcc	L10	Vcc	T11
Vcc	L12	Vcc	T13
Vcc	L14	Vcc	T15
Vcc	L16	Vcc	T17
Vcc	L18	Vcc	T19
Vcc	L22	Vcc	T21
Vcc	AJ18	Vcc	U4
Vcc	AK2	Vcc	U8
Vcc	AK4	Vcc	U10
Vcc	AK11	Vcc	M13
Vcc	AK20	Vcc	M15
Vcc	AL3	Vcc	M17
Vcc	AL5	Vcc	M19
Vcc	AL16	Vcc	M21
Vcc	AL22	Vcc	N8
Vcc	AM4	Vcc	N10
Vcc	AM11	Vcc	N12
Vcc	AM18	Vcc	N14
Vcc	B3	Vcc	N16
Vcc	B5	Vcc	N18
Vcc	B6	Vcc	N20
Vcc	C2	Vcc	N22
Vcc	C4	Vcc	P5
Vcc	C11	Vcc	P7
Vcc	D1	Vcc	P9
Vcc	D3	Vcc	P11
Vcc	D5	Vcc	P13
Vcc	D16	Vcc	P15
Vcc	R2	Vcc	P17
Vcc	R8	Vcc	P19
Vcc	R10	Vcc	P21

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Table 9-2. SIOH Signal – Ball Number (Continued)

Signal	Ball Number		Signal	Ball Number
Vcc	W18		VCCACOM	K19
Vcc	W20		VCCACORE	G20
Vcc	W22		VCCAHL	J19
Vcc	Y5		VCCASP	H20
Vcc	Y7		Vccsp	D30
Vcc	Y9		Vccsp	F24
Vcc	Y11		Vccsp	F28
Vcc	Y13		Vccsp	H26
Vcc	Y15		Vccsp	H30
Vcc	Y17		Vccsp	K24
Vcc	Y19		Vccsp	K28
Vcc	Y21		Vccsp	M26
Vcc	U12		Vccsp	M30
Vcc	U14		Vccsp	P24
Vcc	U16		Vccsp	P28
Vcc	U18		Vccsp	T26
Vcc	U20		Vccsp	T30
Vcc	U22		Vccsp	U26
Vcc	V7		Vccsp	U30
Vcc	V9		Vccsp	W24
Vcc	V11		Vccsp	W28
Vcc	V13		Vccsp	AA26
Vcc	V15		Vccsp	AA30
Vcc	V17		Vccsp	AC24
Vcc	V19		Vccsp	AC28
Vcc	V21		Vccsp	AE26
Vcc	W8		Vccsp	AE30
Vcc	W10		Vccsp	AG24
Vcc	W12		Vccsp	AG28
Vcc	W14		Vccsp	AJ26
Vcc	W16		Vccsp	AJ30
Vcc18	A17		Vccsp	AL24
Vcc18	C21		Vccsp	AL28
Vcc18	D18		Vccsp	B24
Vcc18	F20		Vccsp	B28
Vcc18	F22		Vccsp	D26
Vcc33	AE16		VREFFBCLK66	K22
Vcc33	K20		Vss	AF11
Vcc33	L20		Vss	AF13

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Table 9-2. SIOH Signal – Ball Number (Continued)

Signal	Ball Number	Signal	Ball Number
Vss	AE9	Vss	AB31
Vss	AD7	Vss	AC2
Vss	AD10	Vss	AC4
Vss	AC7	Vss	AC6
Vss	AC8	Vss	AC9
Vss	AB8	Vss	AC15
Vss	AB9	Vss	AC21
Vss	AC10	Vss	AC23
Vss	AB11	Vss	AC26
Vss	AC11	Vss	A15
Vss	AE8	Vss	A19
Vss	AD9	Vss	A21
Vss	AC16	Vss	A23
Vss	AE14	Vss	A25
Vss	AD15	Vss	A27
Vss	AE12	Vss	A29
Vss	AC14	Vss	AA2
Vss	AD13	Vss	AA4
Vss	AD12	Vss	AA7
Vss	AC13	Vss	AA9
Vss	A3	Vss	AA11
Vss	A5	Vss	AA13
Vss	A7	Vss	AA15
Vss	A9	Vss	AA17
Vss	A13	Vss	AA19
Vss	AA21	Vss	AE19
Vss	AA24	Vss	AE24
Vss	AA28	Vss	AE28
Vss	AA32	Vss	AE32
Vss	AB5	Vss	AF1
Vss	AB12	Vss	AF3
Vss	AB14	Vss	AF6
Vss	AB16	Vss	AF9
Vss	AB18	Vss	AF15
Vss	AB20	Vss	AF21
Vss	AB22	Vss	AF23
Vss	AB25	Vss	AF25
Vss	AB27	Vss	AF27
Vss	AB29	Vss	AF29

Table 9-2. SIOH Signal – Ball Number (Continued)

Signal	Ball Number	Signal	Ball Number
Vss	AF31	Vss	AK23
Vss	AG4	Vss	AK25
Vss	AG11	Vss	AK27
Vss	AG17	Vss	AK29
Vss	AG26	Vss	AK31
Vss	AG30	Vss	AL2
Vss	AG32	Vss	AL4
Vss	AH1	Vss	AL6
Vss	AH3	Vss	AL8
Vss	AH5	Vss	AL10
Vss	AH7	Vss	AL12
Vss	AH11	Vss	AL14
Vss	AC30	Vss	AL19
Vss	AC32	Vss	AL26
Vss	AD1	Vss	AL30
Vss	AD3	Vss	AH13
Vss	AD5	Vss	AH19
Vss	AD11	Vss	AH25
Vss	AD17	Vss	AH27
Vss	AD25	Vss	AH29
Vss	AD27	Vss	AH31
Vss	AD29	Vss	AJ2
Vss	AD31	Vss	AJ4
Vss	AE2	Vss	AJ8
Vss	AE4	Vss	AJ10
Vss	AE7	Vss	AJ12
Vss	AE13	Vss	AJ14
Vss	AE17	Vss	AJ16
Vss	AJ21	Vss	B8
Vss	AJ24	Vss	B10
Vss	AJ28	Vss	B12
Vss	AJ32	Vss	B14
Vss	AK1	Vss	B16
Vss	AK3	Vss	B18
Vss	AK5	Vss	B20
Vss	AK7	Vss	B22
Vss	AK9	Vss	B26
Vss	AK13	Vss	B30
Vss	AK15	Vss	C1

Table 9-2. SIOH Signal – Ball Number (Continued)

Signal	Ball Number	Signal	Ball Number
Vss	C3	Vss	F1
Vss	C5	Vss	F3
Vss	C7	Vss	F5
Vss	C9	Vss	F7
Vss	C13	Vss	F12
Vss	C15	Vss	F16
Vss	C19	Vss	F26
Vss	C23	Vss	F30
Vss	C25	Vss	F32
Vss	C27	Vss	G2
Vss	C29	Vss	G4
Vss	C31	Vss	G6
Vss	D2	Vss	G8
Vss	D4	Vss	G19
Vss	D6	Vss	G25
Vss	D8	Vss	G27
Vss	D10	Vss	G29
Vss	D12	Vss	G31
Vss	AM3	Vss	H1
Vss	AM5	Vss	H3
Vss	AM7	Vss	H10
Vss	AM9	Vss	D14
Vss	AM13	Vss	D17
Vss	AM15	Vss	D20
Vss	AM21	Vss	D22
Vss	AM23	Vss	D24
Vss	AM25	Vss	D28
Vss	AM27	Vss	D32
Vss	AM29	Vss	E2
Vss	B2	Vss	E9
Vss	B4	Vss	E11
Vss	E15	Vss	J23
Vss	E19	Vss	J25
Vss	E21	Vss	J27
Vss	E23	Vss	J29
Vss	E25	Vss	J31
Vss	E27	Vss	K5
Vss	E29	Vss	K8
Vss	E31	Vss	K12

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Table 9-2. SIOH Signal – Ball Number (Continued)

Signal	Ball Number	Signal	Ball Number
Vss	K16	Vss	N15
Vss	K26	Vss	N17
Vss	K30	Vss	N19
Vss	K32	Vss	N21
Vss	L2	Vss	N23
Vss	L4	Vss	N25
Vss	L6	Vss	N27
Vss	L13	Vss	N29
Vss	L15	Vss	N31
Vss	L17	Vss	P1
Vss	L19	Vss	P3
Vss	L21	Vss	P6
Vss	L23	Vss	P8
Vss	L25	Vss	P10
Vss	L27	Vss	P12
Vss	L29	Vss	P14
Vss	L31	Vss	P16
Vss	M1	Vss	P18
Vss	M3	Vss	P20
Vss	M5	Vss	P22
Vss	M8	Vss	P26
Vss	M12	Vss	P30
Vss	M14	Vss	P32
Vss	M16	Vss	R4
Vss	H14	Vss	R7
Vss	H18	Vss	R9
Vss	H22	Vss	R11
Vss	H24	Vss	M18
Vss	H28	Vss	M20
Vss	H32	Vss	M22
Vss	J2	Vss	M24
Vss	J4	Vss	M28
Vss	J6	Vss	M32
Vss	J21	Vss	N2
Vss	N4	Vss	R27
Vss	N7	Vss	R29
Vss	N9	Vss	R31
Vss	N11	Vss	T1
Vss	N13	Vss	T3

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Table 9-2. SIOH Signal – Ball Number (Continued)

Signal	Ball Number	Signal	Ball Number
Vss	T6	Vss	V29
Vss	T8	Vss	V31
Vss	T10	Vss	W2
Vss	T12	Vss	W4
Vss	T14	Vss	W6
Vss	T16	Vss	W7
Vss	T18	Vss	W9
Vss	T20	Vss	W11
Vss	T22	Vss	W13
Vss	T24	Vss	W15
Vss	T28	Vss	W17
Vss	T32	Vss	W19
Vss	U2	Vss	W21
Vss	U7	Vss	W23
Vss	U9	Vss	W26
Vss	U11	Vss	W30
Vss	U13	Vss	W32
Vss	U15	Vss	Y1
Vss	U17	Vss	Y3
Vss	U19	Vss	Y8
Vss	U21	Vss	Y10
Vss	U23	Vss	Y12
Vss	U24	Vss	Y14
Vss	U28	Vss	Y16
Vss	U32	Vss	Y18
Vss	V1	Vss	Y20
Vss	V3	Vss	Y22
Vss	V5	Vss	Y25
Vss	V8	Vss	Y27
Vss	V10	Vss	Y29
Vss	R13	Vss	Y31
Vss	R15	Vss	V12
Vss	R17	Vss	V14
Vss	R19	Vss	V16
Vss	R21	Vss	V18
Vss	R23	VSSACOM	K21
Vss	R25	VSSACORE	G21
Vss	V20	VSSAHL	G22
Vss	V22	VSSASP	H21
Vss	V25		
Vss	V27		

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