Empowered by Innovation

NEC

2002·February

Empower your creativity

V850

Embedded Controller

The V850 Series™ of embedded microcontrollers answers diversified needs in all kinds of application systems. It realizes lower power consumption and noise while achieving higher performance and multiple functions. Consisting of a rich lineup, the V850 Series offers optimum solutions for next-generation embedded systems.

Inverter-type air conditioners

Digital video cameras

Automotive electronics

DVD players

Digital still cameras

Cellular phones

Storage devices

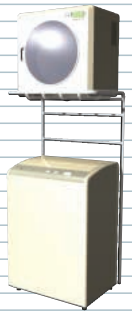
Fax machines

Single-lens reflex cameras

Network modems

Microwave ranges

PDA

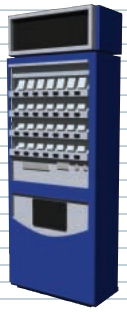


Washing machines

Digital video recorders

Printers

Home audio



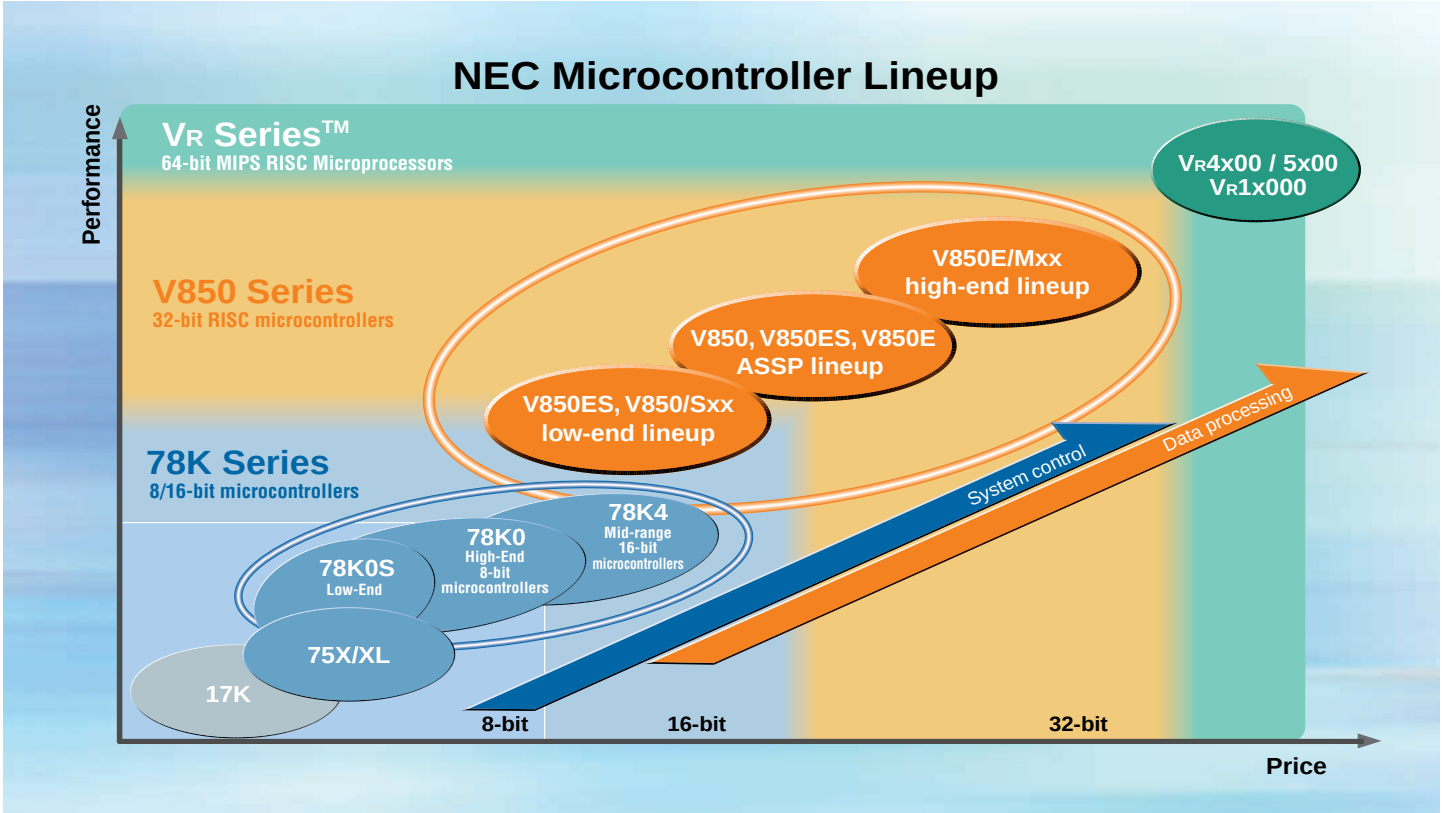
Vending machines

Electronic music instruments

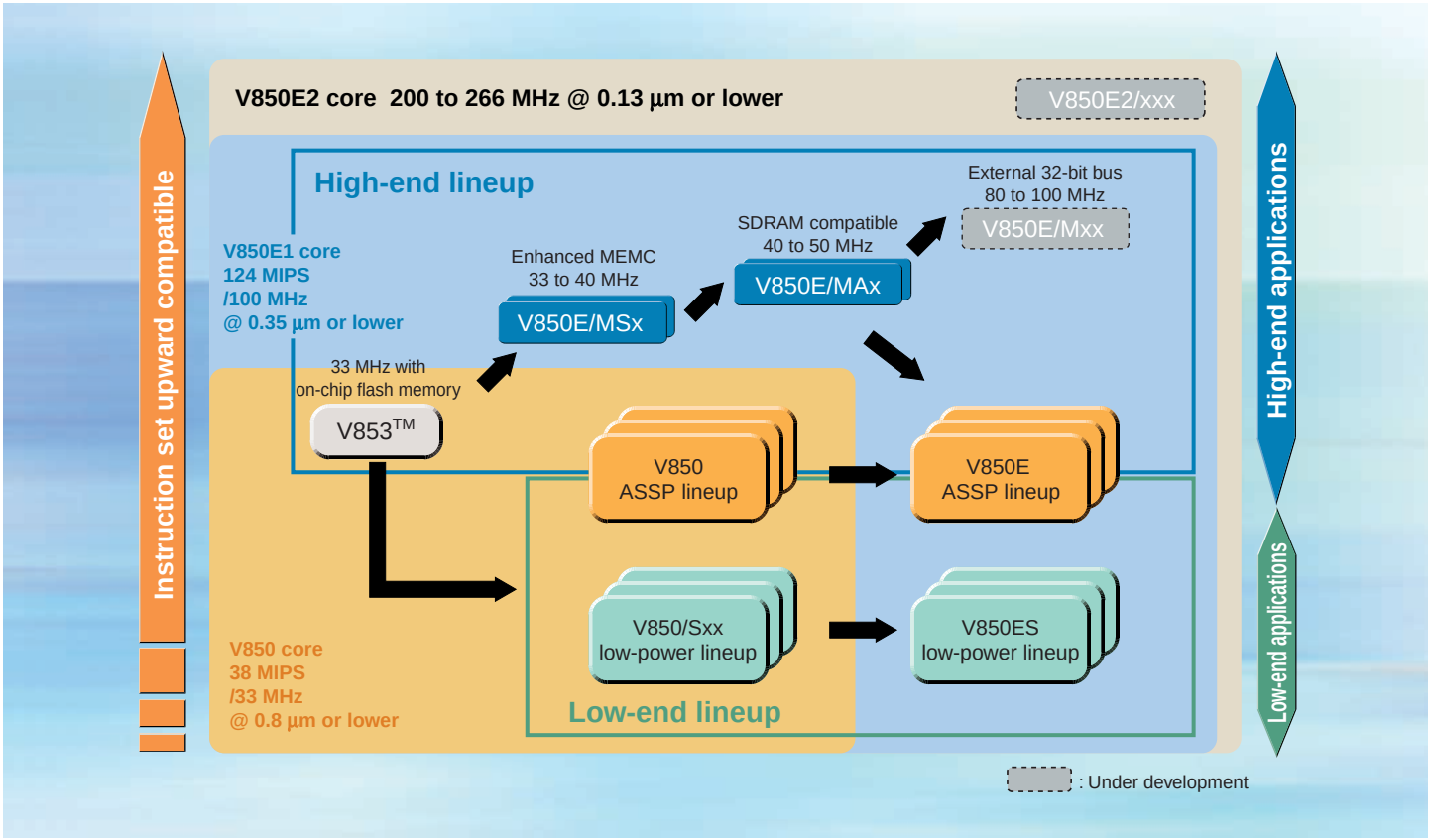
Car audio

Car AV centers

V850 POSITION



V850 ROADMAP



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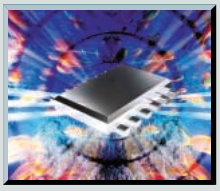
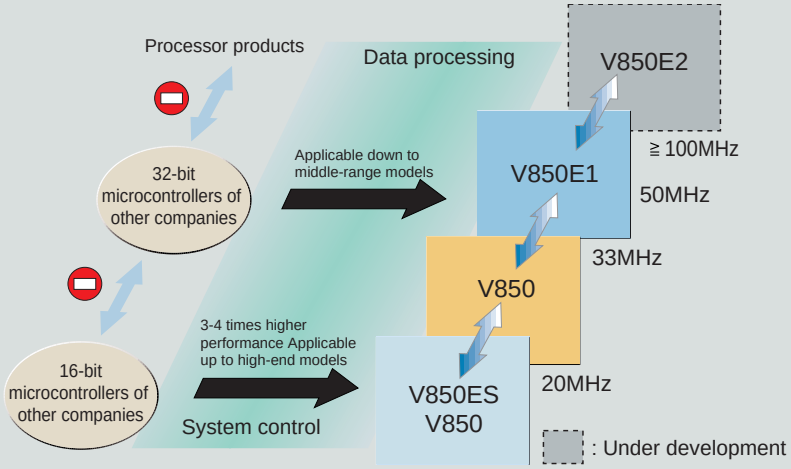
5KEYS V850



High Performance

Scalable coverage of 20 MHz to over 100 MHz

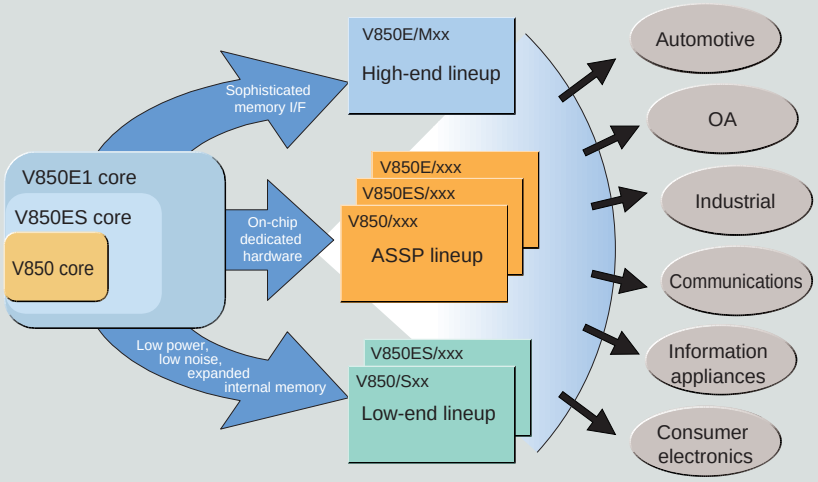
- 3 to 4 times higher performance at same frequency compared to 16-bit microcontrollers
- V850, V850ES, and V850E1 cores are upward compatible at object level.
- V850 Series covers a broad range from middle to high-end market with a single instruction set



Extensive Product Lineup

From low-end/high-end general-purpose products all the way to ASSP lineup

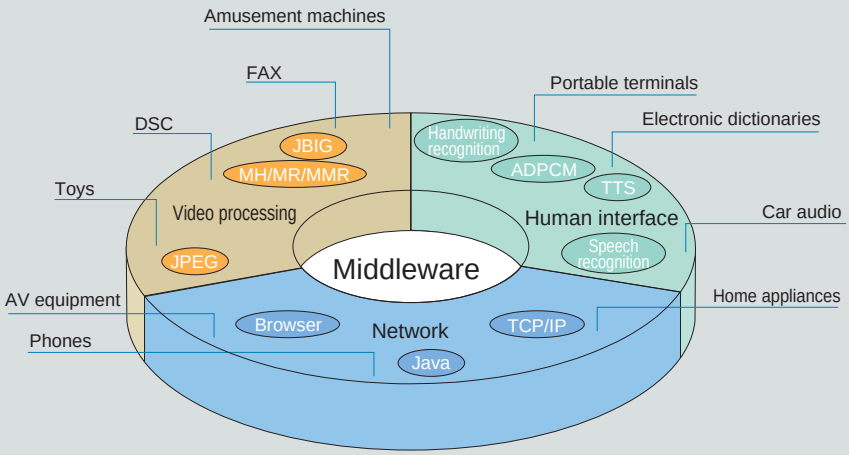
- Low-end lineup designed for 8/16-bit market (V850ES, V850/Sxx)
- High-end lineup with on-chip MEMC, DMA, that pursues high performance (V850E)
- ASSP lineup with on-chip dedicated hardware optimized for various fields (V850E, V850ES, V850/Sxx)

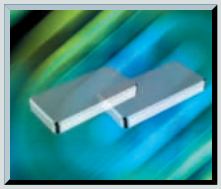


Additional Functions

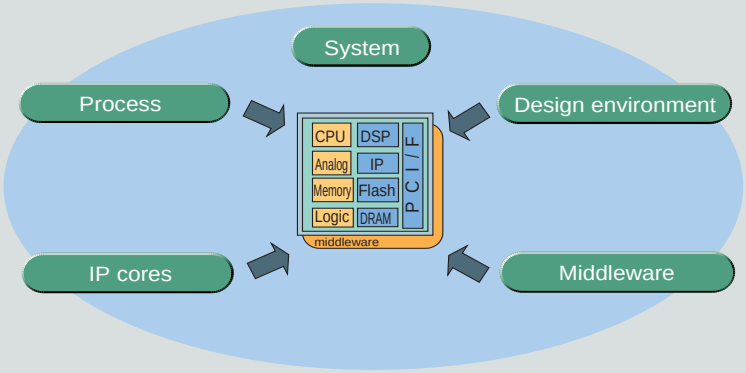
Enriched middleware lineup

- Rich lineup of middleware related to video, audio, networks, etc., optimized for the V850
- Realization of peripheral functions through V850 + middleware combination
  →Shorter development time, lower system cost





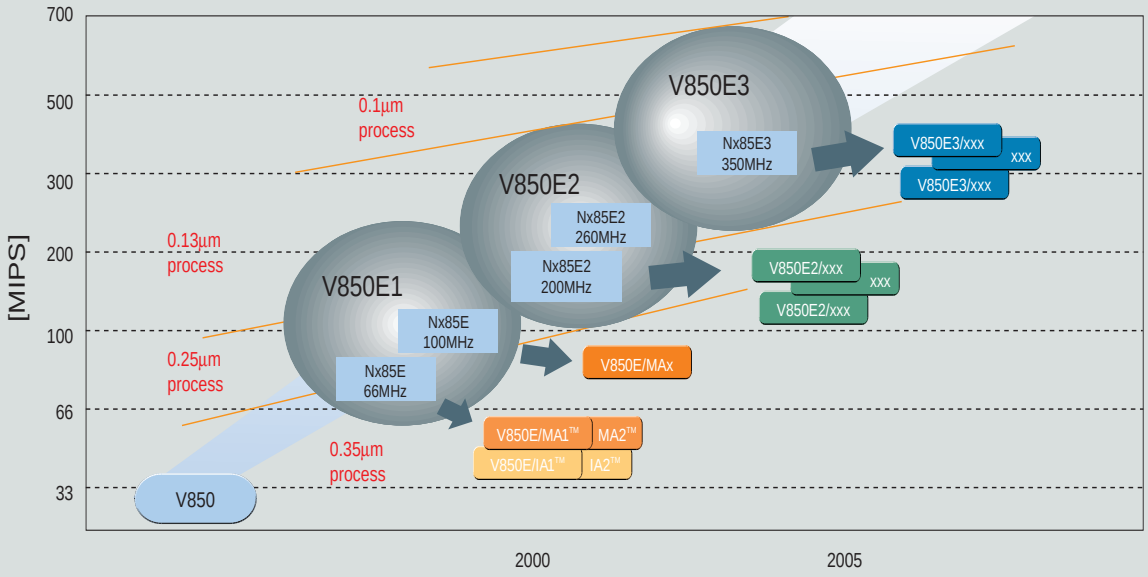
System Integration



High-performance CPU cores

- By meeting the five conditions consisting of leading-edge process technology, high-performance CPU cores, a rich lineup of IP cores, a top-down design environment, and a flexible application environment, the V850 Series offers optimum system-on-chip solutions.

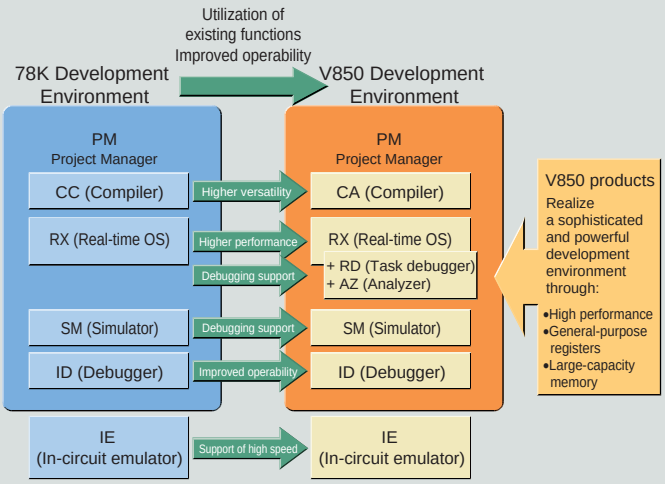
CPU Core Lineup



Accessible Development Environment

Rich lineup and high operability

- Inherits operability of 78K Series.
- Shorter software development TAT through superior operability and sophisticated development environment
- Easy C-language support through high-performance CPUs and real-time OS embedding possible



V850E Product Development Concept

Pursuit of high performance

High-performance CPU using V850E core

- 10% higher performance than V850 CPU at same frequency
- 10% to 20% higher code efficiency than V850 CPU through addition of C-compatible instructions
- Upward compatibility at object level with V850 CPU cores

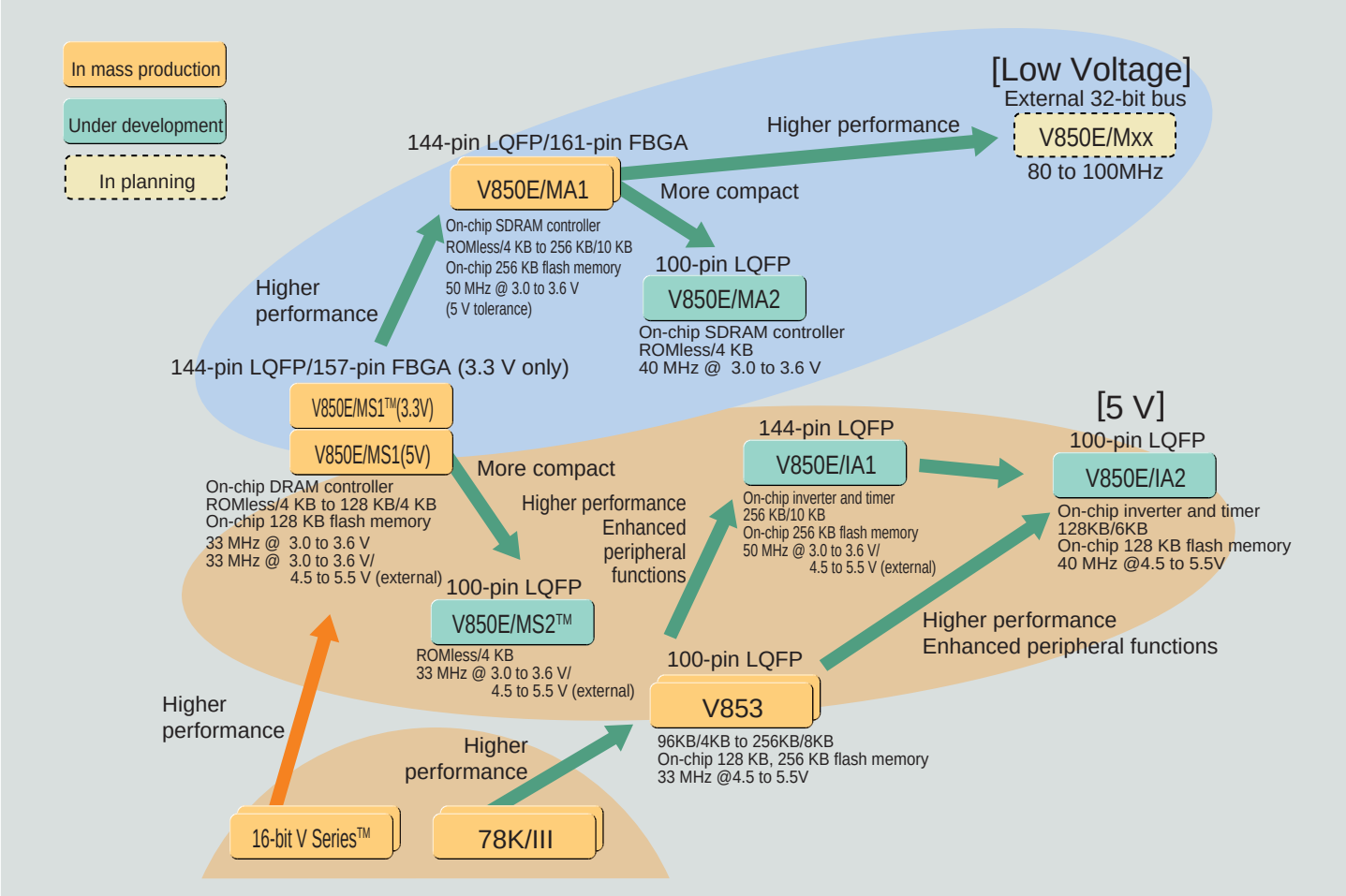
Enhanced external bus performance

On-chip direct interface for various memories

- SRAM, page ROM, EDO DRAM, synchronous DRAM, etc.

On-chip DMA controller

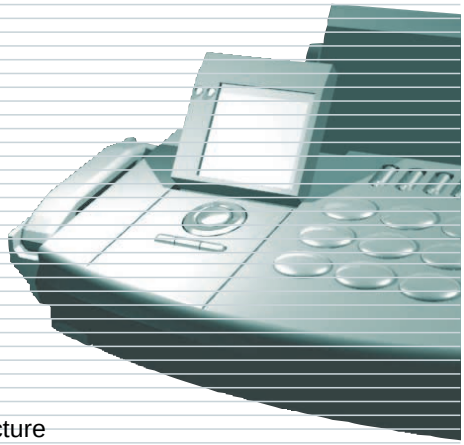
- Realization of voluminous data processing and high-performance control on one chip



V850E Product Features

V850E/MS1

- Performance of 43 MIPS @ 33 MHz
- On-chip memory controllers for EDO DRAM, etc.
- Lineup of products for 5 V systems and 3.3 V systems

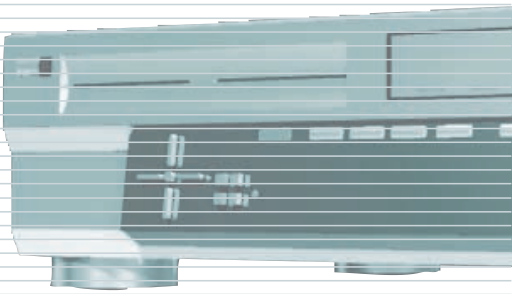


V850E/MS2

- Support of 5 V interface enables connection of existing external I/Os
- Contributes to higher cost performance of sets through use of V850E CPU architecture

V850E/MA1

- High performance of 62 MIPS @ 50 MHz
- On-chip memory controllers for SDRAM, etc.
- Various peripheral functions such as timer, serial interface, and A/D converter



V850E/MA2

- On-chip SDRAM controller
- Contributes to smaller applications, lighter weight, and higher cost performance through use of 14 × 14 mm, 100-pin package

V850E/IA1

- On-chip 3-phase sine wave PWM timer, 2-phase encoder input up/down counter, A/D converter, 2-system motor driving enabled through inverter control
  6-system serial I/F including FCAN for automotive LAN (Ver. 2.0 Part B compliant)

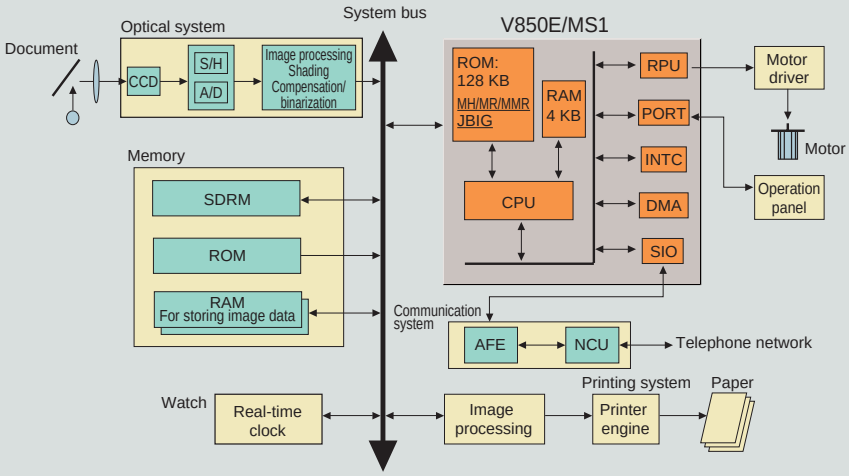
V850E/IA2

- 2-system motor driving enabled through on-chip peripheral functions almost the same as those of V850E/IA1
- System can be configured with single 5 V power supply thanks to on-chip regulator

V850E Product Application Examples

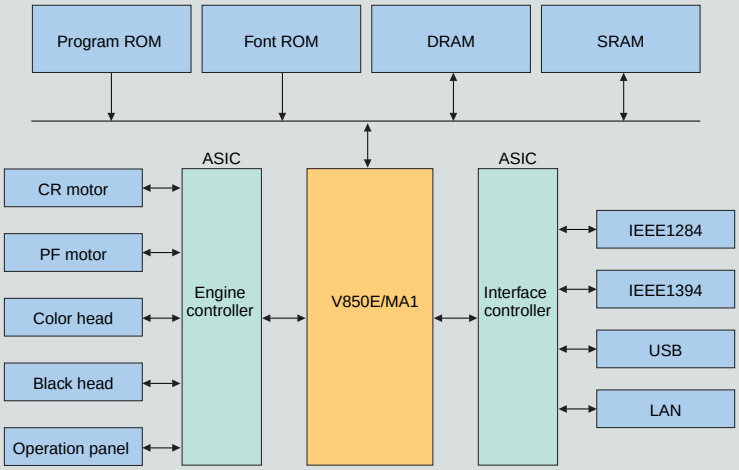
FAX

Application example using V850E/MS1



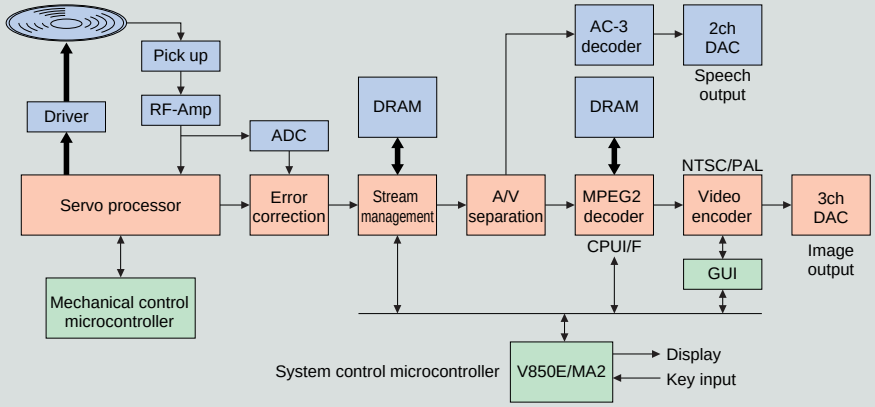
Printer

Application example using V850E/MA1



DVDPlayer

Application example using V850E/MA2



V850ES, V850/Sxx Product Development Concept

High Performance

- 3 to 4 times higher performance compared to 16-bit CISC microcontrollers
- Middleware support (JPEG, speech recognition, etc.)

Low noise & low power

- Optimum design for maximum operating frequency of 20 MHz
- Thorough EMI noise countermeasures

Low-voltage support

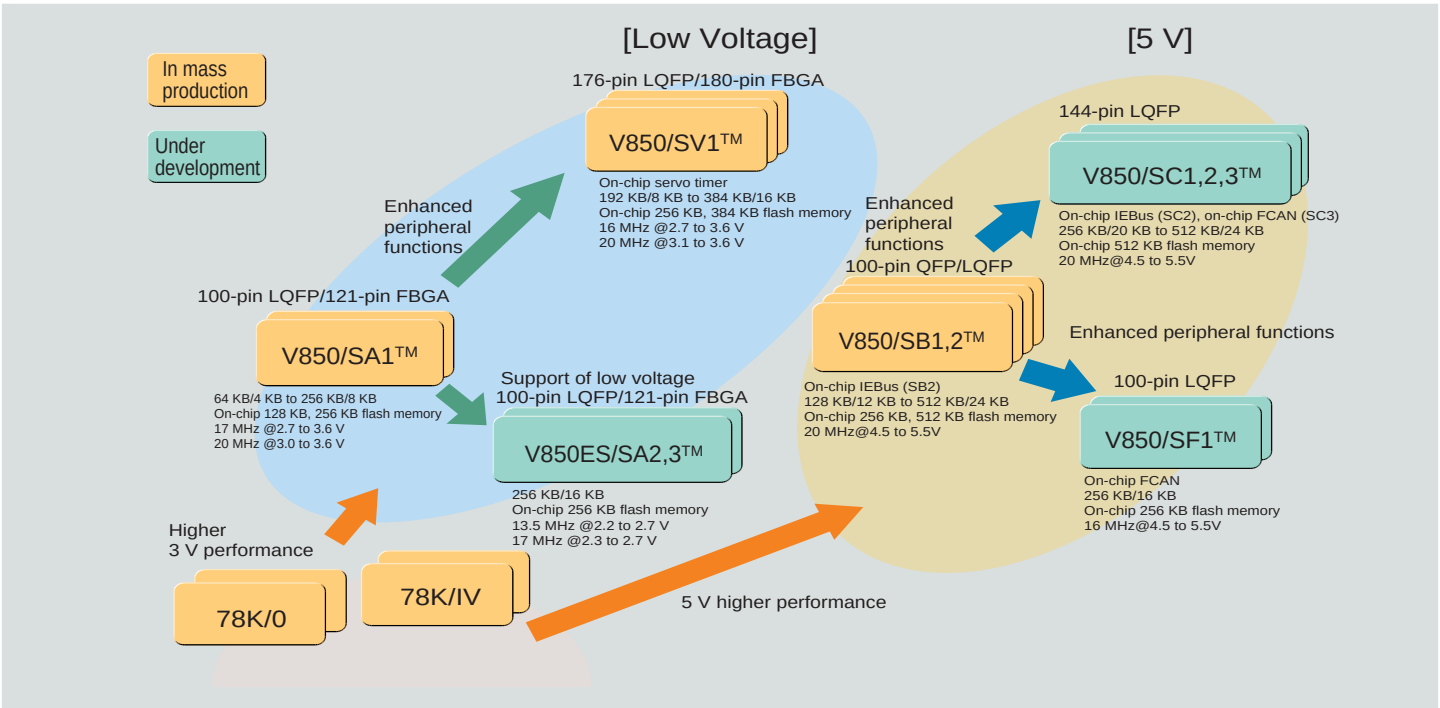
- Realization of 2.2 V low voltage operation (V850ES/SA2, SA3)

Variation in memory and I/O

- Various memory capacities (ROM: 64 KB to 512 KB, RAM: 4 KB to 24 KB)
- Various packages (100-pin to 180-pin)
- Various ASSPs (automotive bus support (IEBus™, CAN), servo timer, etc.)

Peripheral functions inherited from 78K Series

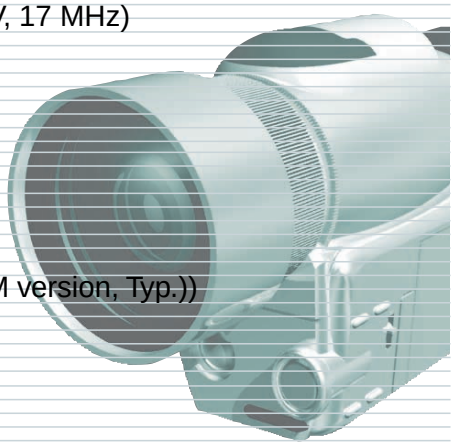
- Standard peripheral functions of 78K Series (timer, serial interface, etc.)
- Designed for 8/16-bit application market
- Pursuit of high cost performance



V850ES, V850/Sxx Product Features

V850ES/SA2, SA3

- Ultra-low power consumption/high-speed operation (30 mW @ 2.5 V, 17 MHz)
- Low-voltage operation of 2.2 V Min. (1.8 V under planning)
- On-chip single power supply flash memory
- On-chip V850ES core



V850/SA1

- Ultra-low power consumption (66 mW (20 MHz @ 3.3 V, mask ROM version, Typ.))
- Rich memory lineup (ROM 64 KB to 256 KB/RAM 4 KB to 8 KB)
- Support of CSP package (121-pin FBGA)

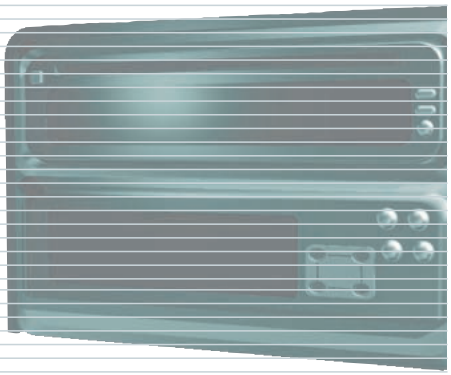
V850/SV1

- Various on-chip peripheral functions including servo timer
- Rich memory lineup (ROM 192 KB to 384 KB/RAM 8 KB to 16 KB)
- Support of high-pin-count CSP package (180-pin FBGA)
- ASSP lineup for DVC

V850/SB1, SB2

- Low EMI noise
- On-chip large-capacity memory (512 KB/24 KB Max.)
- Rich memory lineup (ROM 128 KB to 512 KB/RAM 12 KB to 24 KB)
- Automotive bus support (V850/SB2 only)

V850/SF1



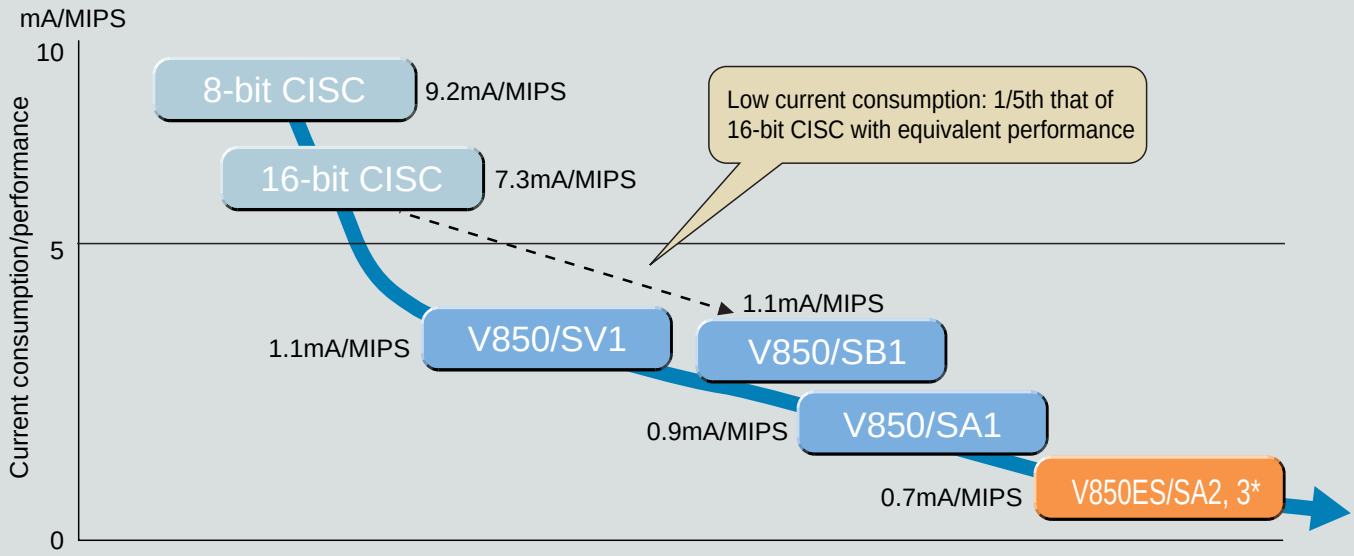
- Low EMI noise
- On-chip FCAN controller (2 ch Max.)
- ASSP lineup for car audio

V850/SC1, SC2, SC3

- Low EMI noise
- Enhanced peripheral functions for V850/SB1, SB2 (100-pin → 144-pin)
- Automotive bus support (IEBus, FCAN)

V850ES, V850/Sxx Product Features

◆ V850ES, V850/Sxx Series power performance ◆



*:Under development

◆ Smooth transition from CISC to RISC ◆

CISC-like use enabled

- Bit manipulation instructions (SET1, CLR1, NOT1, TST1)
- Multi-status flags
- 32-bit barrel shifter

On-chip standard peripheral functions of 78K Series

- Timers (8-bit, 16-bit)
- Serial interface (3-wire CSI, UART)
- Watchdog timer, etc.

High code efficiency

- Equals CISC code efficiency (1.0 to 1.2)
- High-level language (C language) programming supported

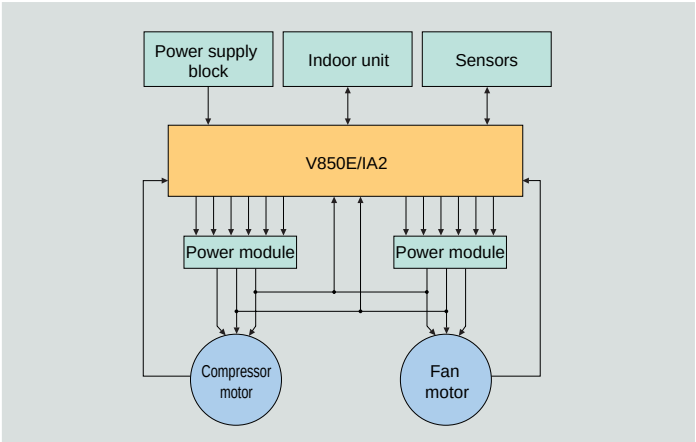
◆ Comparison of peripheral functions of 78K Series and V850/Sxx products ◆

	78K/0 Series	78K/IV Series	V850 Series				
	μPD78003x	μPD78421x	V850/SA1	V850/SB1,2	V850/SV1	V850/SF1	V850/SC1,2,3
16-bit timer	TM0	←	←	←	←	←	←
8-bit timer	TM5	←	←	←	←	←	–
Serial interface (CSI)	SIO3	←	←	←	←	←	←
Serial interface (UART)	UART0	←	UART3	←	←	←	←
I²C interface	IIC0	←	←	←	←	←	←
AD converter	ADCTL0	←	←	←	←	←	←
Real-time output	–	RT00	←	←	←	–	–
Watchdog timer	WDT	Separate specifications	WDT	←	←	←	←
Watch timer	WT	←	←	WTN0	←	←	←
Key return function	–	Separate specifications	–	KR0	←	←	←

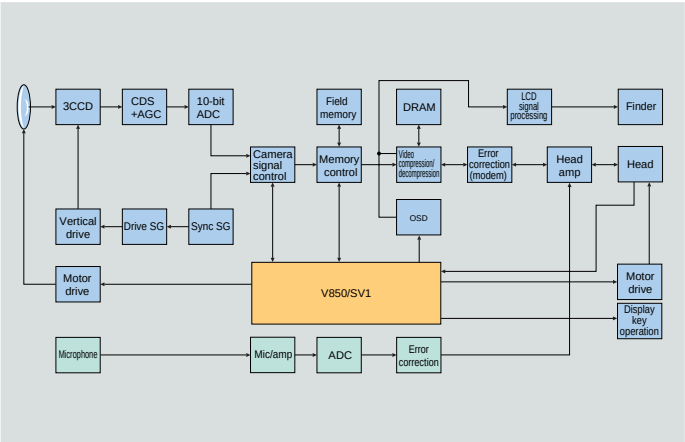
←:Listed on left
– :Not provided

V850 ASSP Lineup

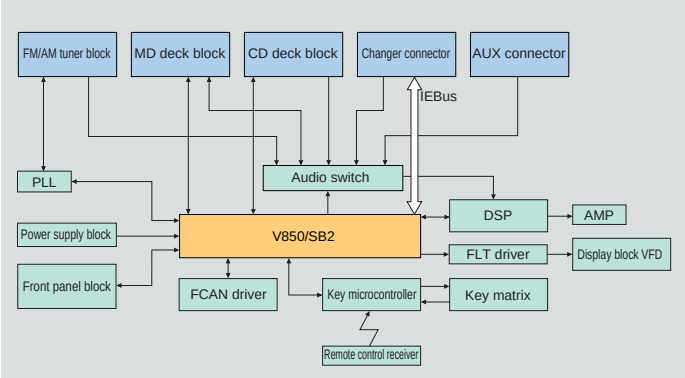
■V850E/IA2 inverter air conditioner application example



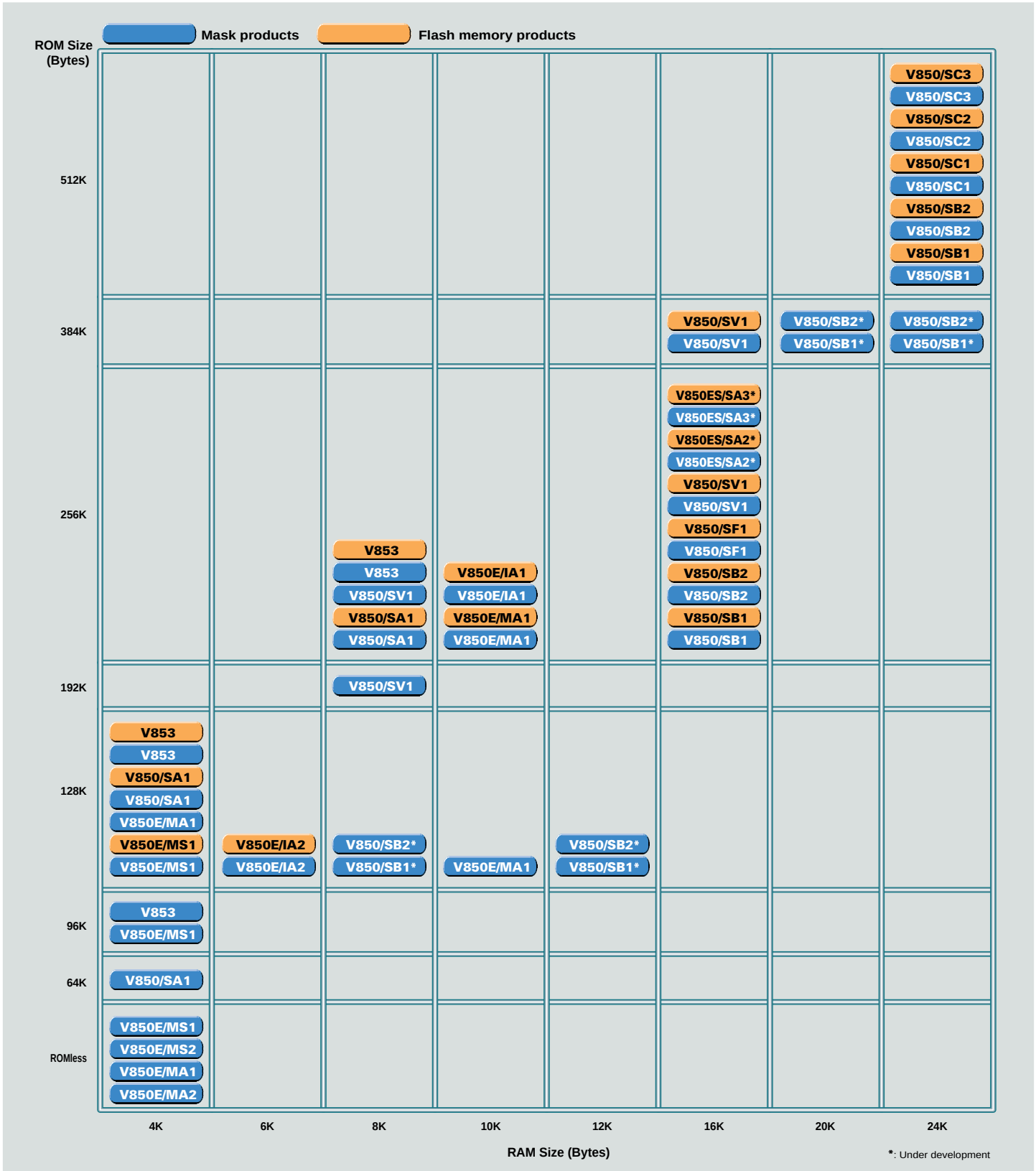
■V850/SV1 System Block Diagram (DVC)



■V850/SB2 System Block Diagram (Car Audio)



Memory Lineup



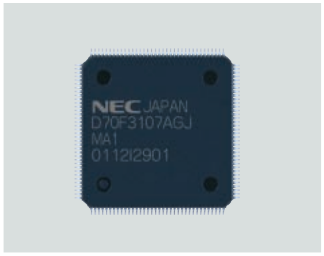
Package Lineup

Package Name	Applicable Products
100-pin plastic QFP (14 × 20 mm)	V850/SB1, SB2, SF1
100-pin plastic LQFP (14 × 14 mm)	V850E/MA2, MS2, IA2, V850ES/SA2, V850/SA1, SB1, SB2, SF1, V853
144-pin plastic LQFP (20 × 20 mm)	V850E/MA1, IA1, MS1, V850/SC1, SC2, SC3
176-pin plastic LQFP (24 × 24 mm)	V850/SV1
121-pin plastic FBGA (12 × 12 mm)	V850ES/SA3, V850/SA1
157-pin plastic FBGA (14 × 14 mm)	V850E/MS1
161-pin plastic FBGA (13 × 13 mm)	V850E/MA1
180-pin plastic FBGA (13 × 13 mm)	V850/SV1

● QFP package photos

100-pin plastic QFP
0.65 mm pitch, 14 × 20 mm, 3.0 mm thick

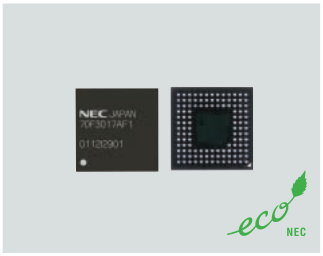
100-pin plastic LQFP
0.5 mm pitch, 14 × 14 mm, 1.4 mm thick



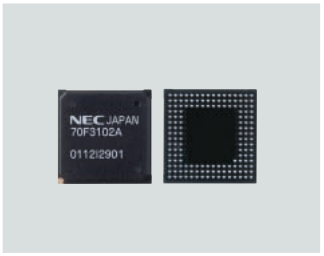
144-pin plastic LQFP
0.5 mm pitch, 20 × 20 mm, 1.4 mm thick

176-pin plastic LQFP
0.5 mm pitch, 24 × 24 mm, 1.4 mm thick

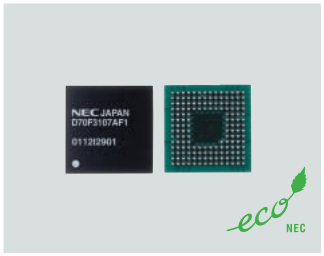
● FBGA package photos



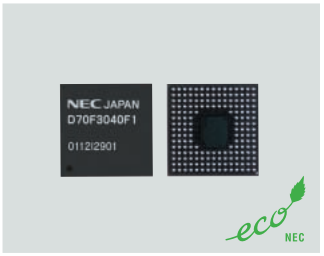
121-pin plastic FBGA
0.8 mm pitch, 12 × 12 mm, 1.48 mm thick



157-pin plastic FBGA
0.8 mm pitch, 14 × 14 mm, 1.31 mm thick



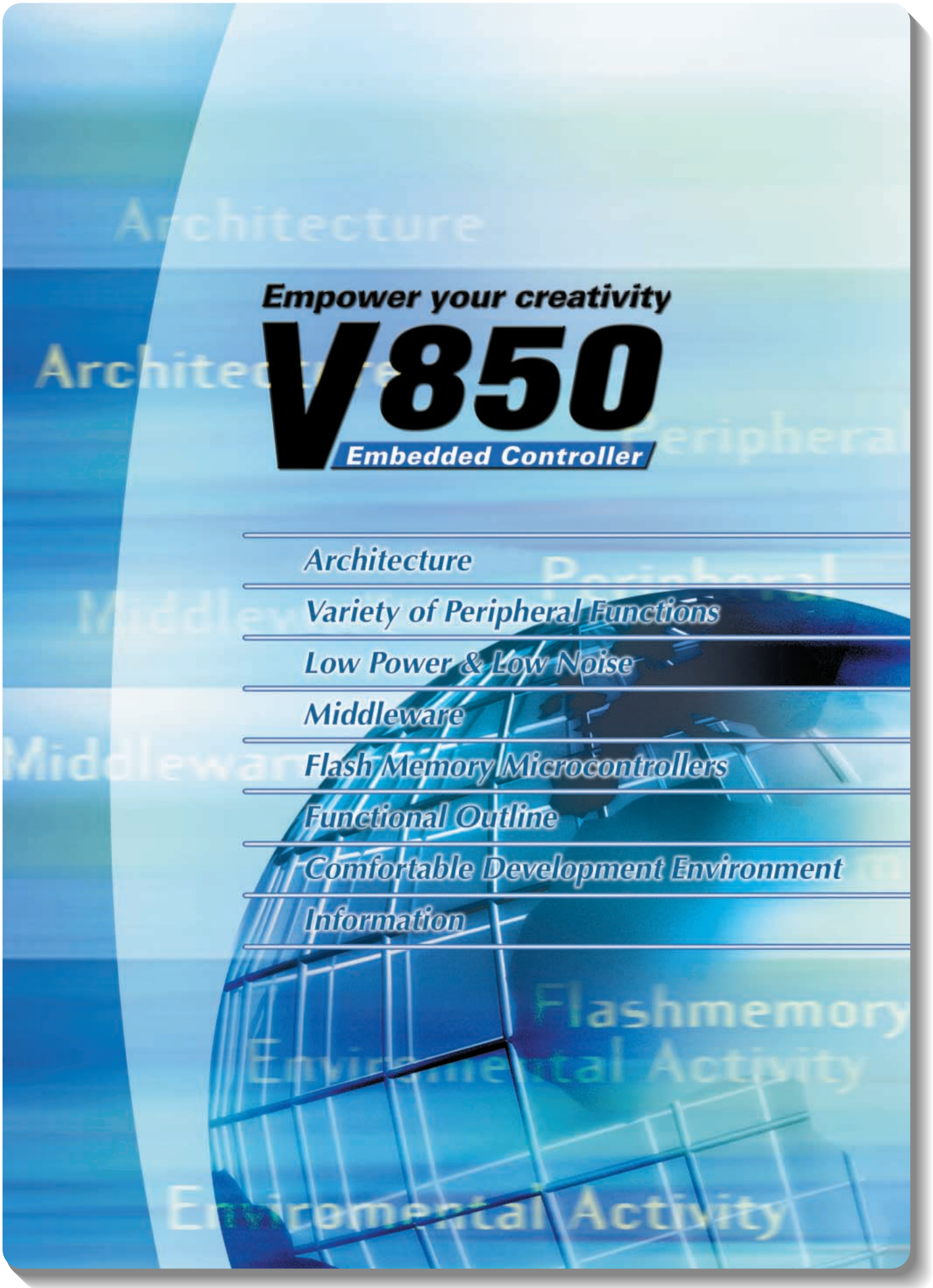
161-pin plastic FBGA
0.8 mm pitch, 13 × 13 mm, 1.48 mm thick



180-pin plastic FBGA
0.8 mm pitch, 13 × 13 mm, 1.48 mm thick

eco NEC

The Eco Symbol mark is applied to products that comply with NEC's environmental standard, which is one of the world's toughest. Such products are antimony-free and use smaller amounts of halogen, and are subject to product assessment and green procurement.


Empower your creativity
V850
Embedded Controller
Architecture
Variety of Peripheral Functions
Low Power & Low Noise
Middleware
Flash Memory Microcontrollers
Functional Outline
Comfortable Development Environment
Information

Architecture

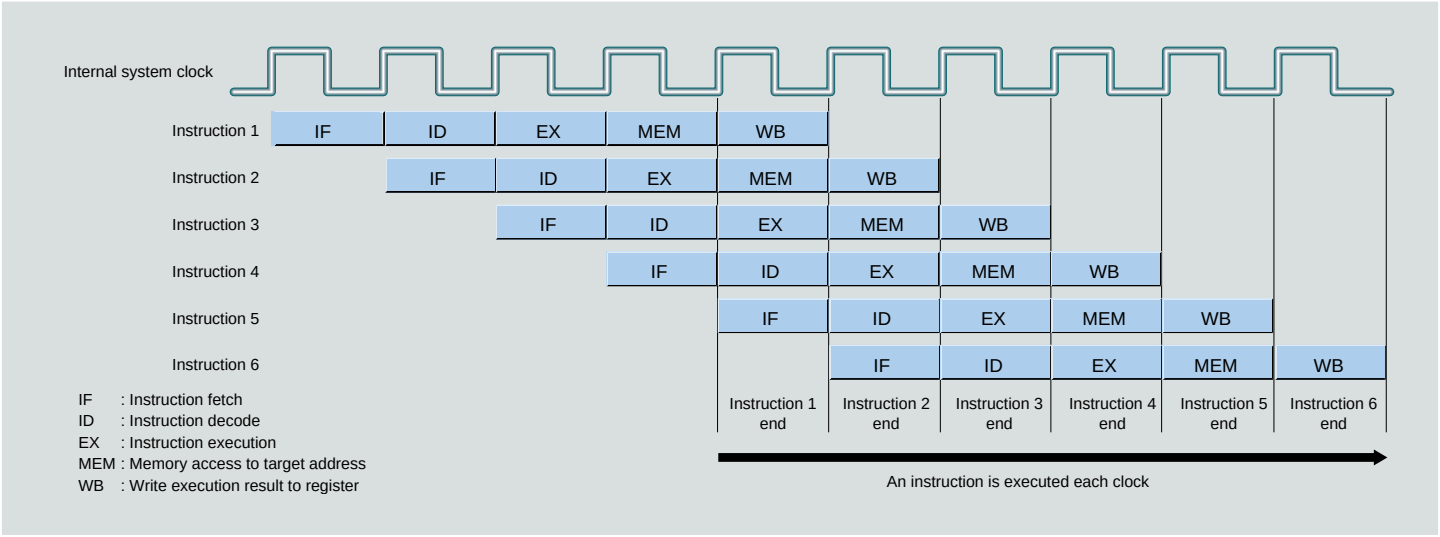
V850 Common Architecture

The V850 Series, which consists of single-chip RISC microcontrollers that use an architecture optimized for embedding, has the following features.

- 5-stage pipeline processing
- Harvard architecture
- 32 general-purpose registers
- Simple addressing
- 2-byte basic instruction set
- Support of CISC-like instructions
- Multi-status flags
- DSP function
- 32-bit barrel shifter

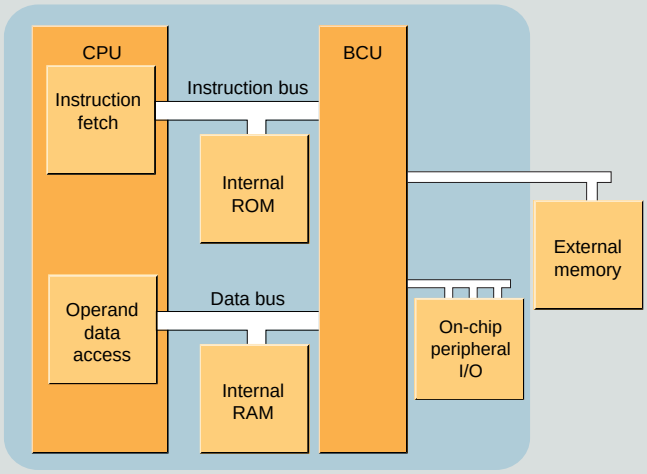
■5-stage pipeline processing

The V850 Series uses a 5-stage pipeline structure (5 stages from instruction fetch to writeback) that supports simultaneous processing of 5 instructions, thus enabling the execution of almost all instructions in just one clock.



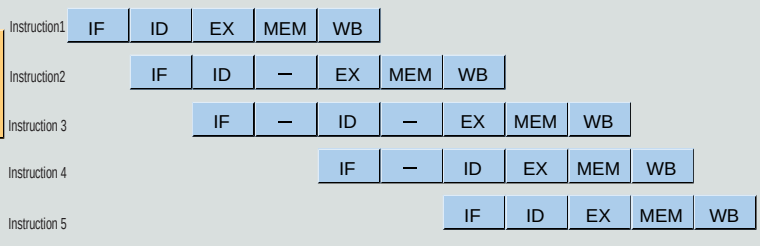
■Harvard architecture

The V850 Series uses the Harvard architecture, which is designed so that the instruction bus and data bus can operate completely independently from each other, thereby preventing pipeline operation problems and ensuring efficient instruction execution.



In the case of an architecture other than the Harvard architecture, the MEM stage of instruction 1 and the IF stage of instruction 4, and the MEM stage of instruction 2 and the IF stage of instruction 5 conflict, causing bus waits. This in turn causes the pipeline operation to become disordered and lowers the instruction execution speed.

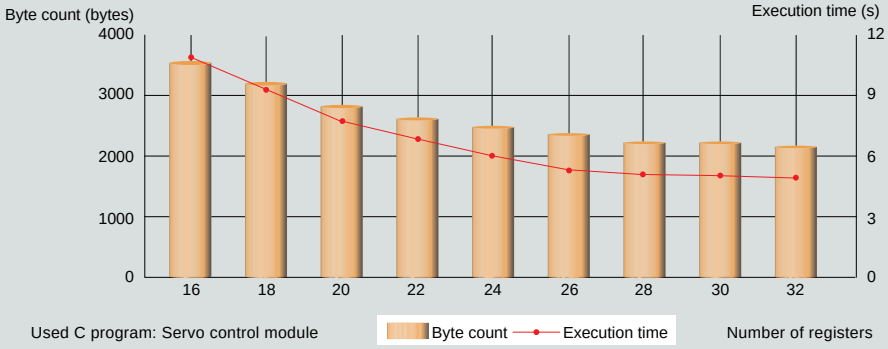
Pipeline Operation of Non-Harvard Architecture



■32 general-purpose registers

The V850 Series provides 32 general-purpose registers. Along with a hardware environment that is ideal for program execution, the development environment, including compilers, exploits these 32 registers to achieve program generation with superior code efficiency and execution performance.

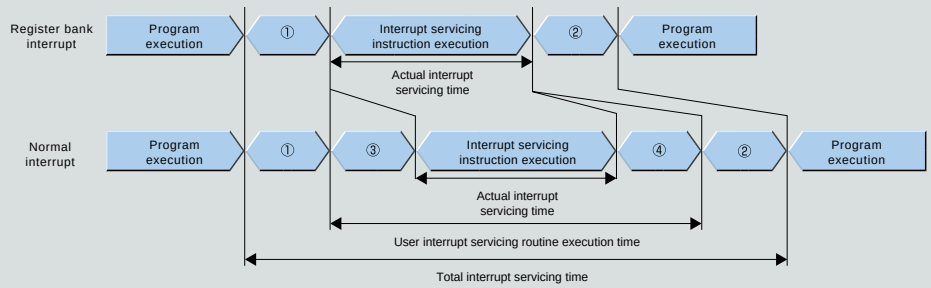
Comparison of Performance/Object Efficiency According to Number of Registers



For example, looking at the program execution time and code size changes when the number of registers used by the compiler is changed using the servo control module, we can see that the larger the number of registers, the better the program execution speed and the smaller the code size. However, from about 26 registers, the improvement in terms of execution speed and code size becomes smaller, and in the neighborhood of 32 registers, there are no more changes. This is why the V850 Series has been provided with 32 registers as the strict minimum requirement.

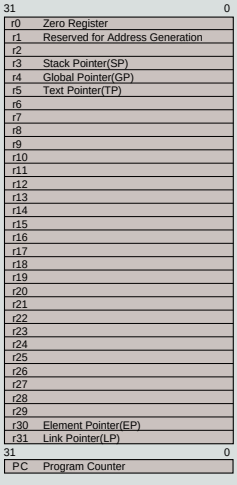
■Software register bank

The number of registers can be selected from among 22, 26, and 32 as a compiler option to efficiently execute application programs. Unused registers can be used as a software register bank for which save and restore processing is not required during interrupt servicing or task switching, which increases the processing speed.



① Save the program counter, etc., to a save register.
② Execute the interrupt restore instruction. Restore the program counter value, etc., from the save register.
③ Save general-purpose registers to stacks.
④ Restore general-purpose registers from stacks.

■General-purpose register configuration



Name	Application	Operation
r0	Zero register	Always holds "0"
r1	Assembler reservation	Used as working register for address generation
r2	Address/data variable register (If real-time OS being used does not use r2)	
r3	Stack pointer	Used for stack frame generation during function call
r4	Global pointer	Used when accessing global variables in the data area
r5	Text pointer	Used as register for specifying the beginning of the text area (program code allocation)
r6-r29	Address/data variable register	
r30	Element pointer	Used as base pointer for address generation during memory access
r31	Link pointer	Used during function call by compiler
PC	Program counter	Holds instruction addresses during program execution

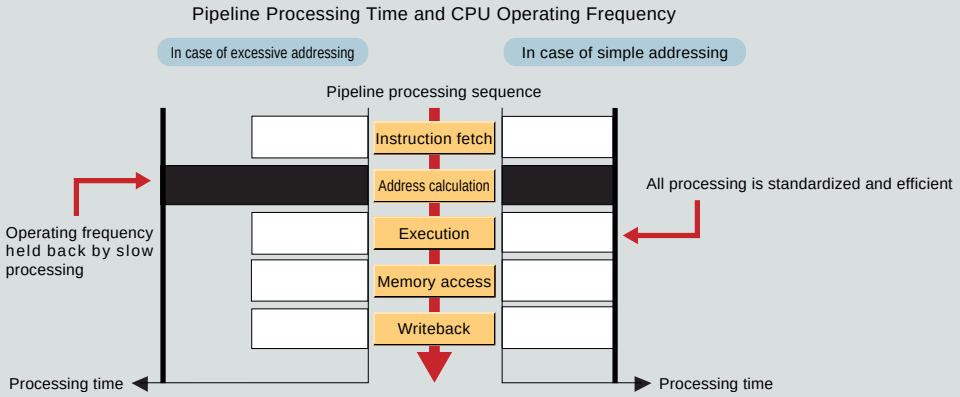
■System register configuration

	No.	System Register Name	Operand Specification LDSR	Operand Specification STSR	Application
	0	EIPC	○	○	Register for saving status during interrupt
	1	EIPSW	○	○	
	2	FEPC	○	○	Register for saving status during NMI
	3	FEPSW	○	○	
	4	ECR	×	○	Interrupt source register
	5	PSW	○	○	Program status word
Only supported by V850E1 CPU core products supported	16	CTPC	○	○	Register for saving status during CALLT execution
	17	CTPSW	○	○	
	18	DBPC	○	○	Register for saving status during exception/debug trap
	19	DBPSW	○	○	
	20	CTBP	○	○	CALLT base pointer
	6-15, 21-31	Reserved	×	×	

× : Access prohibited
○ : Access enabled
LDSR: Instruction to load general-purpose register contents to system register
STSR: Instruction to store system register contents to general-purpose register

■Simple addressing

The increased amount of address calculations in the CPU in the case of complex addressing causes disturbances in the pipeline operation. As a result, address calculation becomes a bottleneck for pipeline processing and raising the frequency to increase the performance becomes difficult. The V850 Series avoids this problem by supporting only simple addressing.



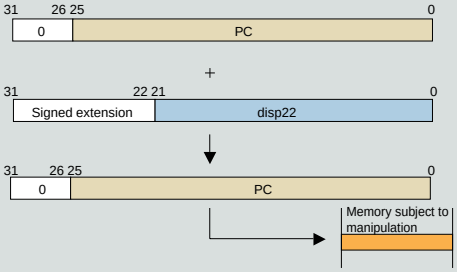
■Addressing mode

●Instruction addresses

•Relative addressing (PC dependent)

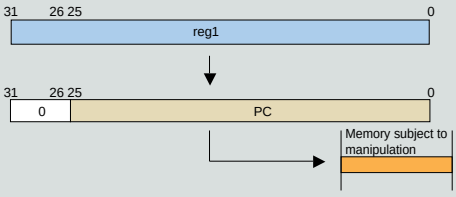
Add 9 signed bits or 22 signed bits of data of the instruction code to the program counter.

Example: 22-bit data



•Register addressing (register indirect)

Transfer the contents of the general-purpose register specified by the instruction (reg1) to the program counter (PC).



●Operand addresses

•Register addressing

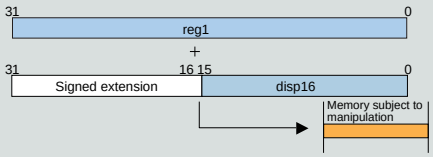
Addressing that accesses the general-purpose register specified by the general-purpose specification field or a system register as an operand.

•Immediate addressing

Addressing of 5-bit data or 16-bit data for manipulation in the instruction code.

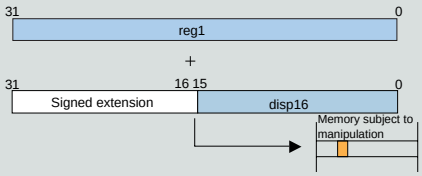
•Based addressing

Addressing that accesses memory, with the sum of the contents of the general-purpose register (reg1) and 16-bit displacement (disp16) as the operand address.



•Bit addressing

Addressing that accesses 1 bit of 1 byte of the memory space, with the sum of the contents of the general-purpose register (reg1) and 16-bit displacement (disp16) that has been sign extended to word length as the operand address.



■2-byte basic instruction set

The V850 Series employs a 2-byte instruction code to perform basic processing to enable compact program development equivalent to 16-bit CISC microcontrollers.

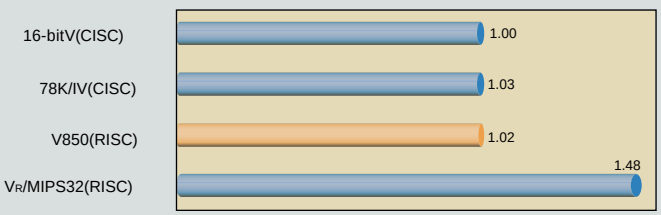
•Improved object efficiency through ROMization programming

Application of 2-byte instructions to all basic processing, consisting of load, store, arithmetic/logic operations, and branching.

•To realize ease of use, restrictions on 16-bit fixed-length instructions are partially removed through incorporation of 32-bit instructions.

•Bit manipulation instructions, etc.

Object Code Size Comparison
(Dhrystone 1.1/Large model)



■ CISC-like instructions for embedding (bit manipulation instructions)

The V850 Series supports bit manipulation instructions suitable for flag manipulation on I/O registers, which play a large role in embedding control.

- Improvement of operability of memory mapped I/Os for control purposes
- Manipulation of any 1 bit of byte data in the memory space
- Provision of test (tst1)/set (set1)/clear (clr1)/invert (not1)
- Effective for reducing object size and execution time since flags can be manipulated in 1-bit units with 1 instruction

Example: Setting (1) bit 6 of ASIM00 register

Item \ Bit Manipulation Instruction	When Used	When Used	
Coding example	set1 6, ASIM00[r0]	ld.b ASIM00[r0], r20 ori 0x0040, r20, r20 st.b r20, ASIM00[r0]	add -4, sp st.w r20, 0[sp]] Save r20 ld.b ASIM00[r0], r20 ori 0x0040, r20, r20 st.b r20, ASIM00[r0] ld.w 0[sp], r20 add 4, sp] Restore r20
Object size	4 bytes	12 bytes	24 bytes
Execution time	4 clocks	4 clocks	8 clocks

■ Multi-status flags

In the V850 Series, calculation results are reflected in registers as status flags. As a result, delay branching such as can be seen in the RISC microcontrollers of other manufacturers does not occur and programs can be coded with the same feel as CISC microcontrollers.

- Easy recording with assembler
- Improved object efficiency and execution speed

ZERO : Zero processing
PLUS : Positive processing
MINUS : Negative processing

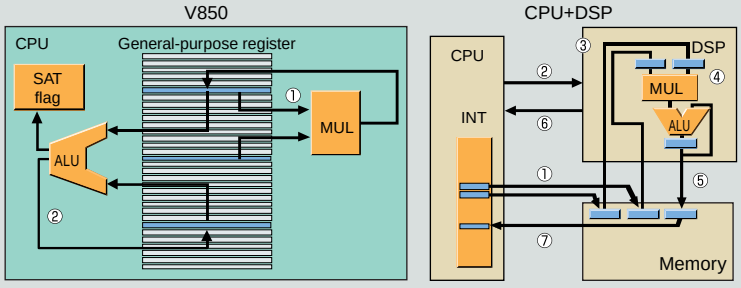
Example: Program that branches to positive/negative/zero according to register contents

CISC Microcontroller	V850	Other Manufacturer's RISC Microcontroller
cmp ax, 0 jz ZERO jgt PLUS jmp MINUS	cmp 0, r10 bz ZERO bgt PLUS br MINUS	cmp/eq #0, r10 bt ZERO cmp/pl r10 bt PLUS bra MINUS nop ;For delay branching

■ DSP function

The V850 Series provides a DSP function for executing high-speed calculations and product-sum operations indispensable for digital signal processing such as image and speech processing.

- Direct data handling via general-purpose registers
- Realization of digital signal processing through general-purpose CPU
- High-speed 16-bit (V850 CPU), 32-bit (V850E1 CPU) multiply/sum-of-products
  (Multiply: 1 to 2 clocks, sum-of-products: 3 clocks)
- Effective for filter operations and matrix operations for feedback calculations in speed, position, and other servo control.

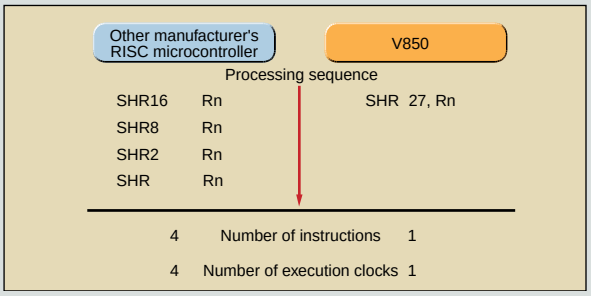


■ 32-bit barrel shifter

V850 Series can realize bit manipulations frequently used during signed data and image data processing in 1 instruction per clock.

- Shifting of any number of bits (0 to 31) executable in 1 instruction per clock
  Improved execution speed/object efficiency
  Effective for extracting arbitrary bit lengths of image data and signed data (extracting code during MH/MR/MMR encoding, etc.)

Example: 27-bit logical right shift



Strengths of V850E1 and V850ES Cores

The V850E1 and V850ES cores are CPU cores that enhance the functions of the V850 core.

■ V850E1 core

- ●Higher performance and improved operating frequency of 50 to 100 MHz
- ●Improved external memory access function
- ●Improved code efficiency (10 to 15% higher than V850 core)
  - •Addition of C language compatible instructions (Switch instruction, CALLT instruction, etc.)
- ●High performance high-end lineup (V850E products), system-on-chip core lineup

■ V850ES core

- ●Next-generation CPU core of low-end lineup
- ●Support of lower voltage for V850/Sxx products
- ●Improved code efficiency through use of same architecture as V850E1
  (10 to 15% higher than V850 core)

Function \ CPU Core	V850	V850ES	V850E1
Maximum operating frequency	20/33 MHz	20 MHz	50→100MHz
Maximum program memory space	16 MB	16 MB	64 MB
Maximum data memory space	16 MB	16 MB	256 MB
Higher performance	Use of 5-stage pipeline Use of Harvard architecture	Improvement of pipeline • Non-blocking load/store Parallel execution of instructions (during instruction execution in internal ROM) • Addition of branch/load pipes • Shift to 3-operand manipulations in 1 slot	
Higher code efficiency	Use of 2-byte instructions Use of CISC instructions	Addition of C language compatible instructions (Addition of Switch instruction, Callt instruction, data conversion instruction, Prepare/Dispose instruction)	
Multiplier	16 × 16 bit→32 bit	16 × 16 bit→32 bit (32-bit multiply instruction support)	32 × 32 bit→64 bit
Interrupt responsiveness	11 to 18 clocks	4 to 10 clocks	

Employment as ASIC CPU Cores

◆ **Smooth transition to ASIC microcontroller development using V850E1 CPU cores**

1. Introduction to market with short TAT through use of standard V850E1 products
2. Optimization of system through switch to ASIC

◆ **Easy securing of compatibility from traditional systems made into ASICs through use of same device development methods for both standard products and ASIC microcontrollers**

◆ **Development of CPU cores bearing in mind shift to ASIC**

➢ Software debugging support

Release of CPU core that supports on-chip debugging through full-function in-circuit emulator, JTAG method (N-Wire ICE) and on-chip debugging with trace function

➢ Internal system bus configuration

Independent high-speed 32-bit synchronous system bus and 16-bit asynchronous bus for low-speed peripheral function macro connection, realizing both high-speed processing, low-power consumption and easy design

➢ Provision of large assortment of peripheral function macros

Cache memory, memory controller, ROM/RAM, USB, etc.

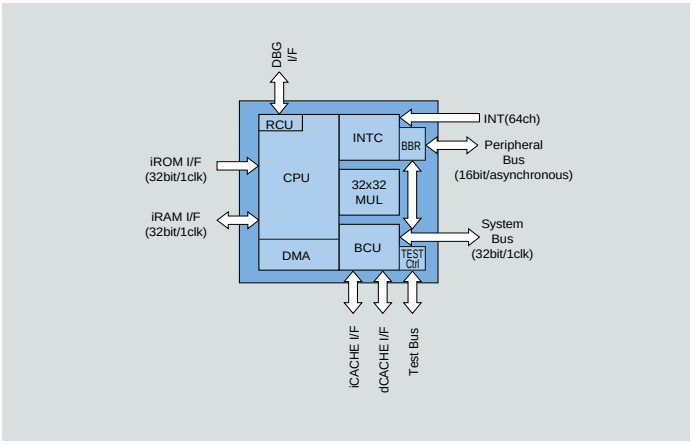
◆ **Covering required performance and power consumption through support of a large variety of processes**

Process	Cell-based IC family
0.35μm	CB-9VX
0.25μm	CB-10VX
0.13μm	CB-12

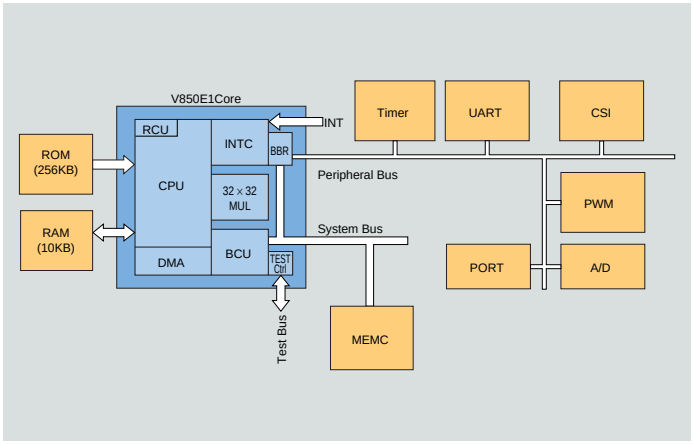
■V850E1 core

- Realization of excellent performance/power ratio of 827 MIPS/W for 100 MHz Max. (at 2.5 V operation)
- Improved object efficiency
- A flexible and high-performance bus system can be configured through independent buses such as a high-speed system bus that enables 400 MB/s data transfer and a low-speed peripheral macro connection bus.
- Support of on-chip debugging function

■V850E1 core



■V850E/MA1 block configuration



■V850E1, V850ES architecture

The V850E1 and V850ES cores achieve high performance and higher code efficiency through the implementation of the following improvements to the V850 CPU core.

Non-blocking load/store

- Improved bus use efficiency
- Shorter interrupt insensitivity period

Addition of branch/load pipes

- 2-clock branching
- Parallel execution of instructions

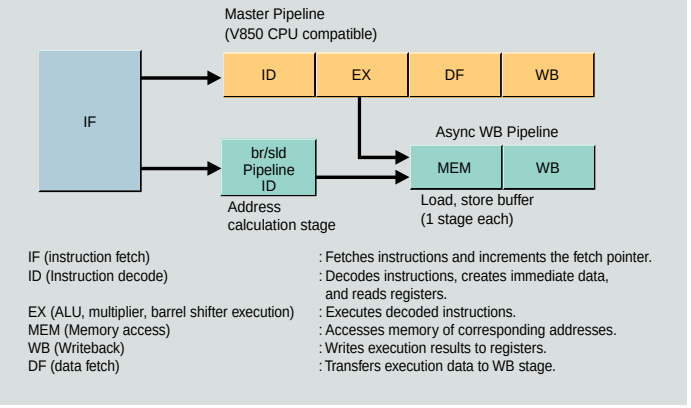
Shift to 3-operand manipulations in 1 slot

- Improved absolute performance
- Example: Synchronous processing of mov + add

Addition of high-level language-compatible instructions

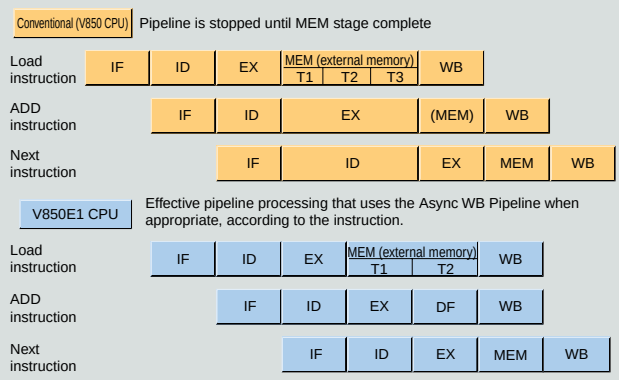
- Improved code efficiency
- 10 to 15% improvement in object efficiency mainly when C compiler used

●Pipeline configuration



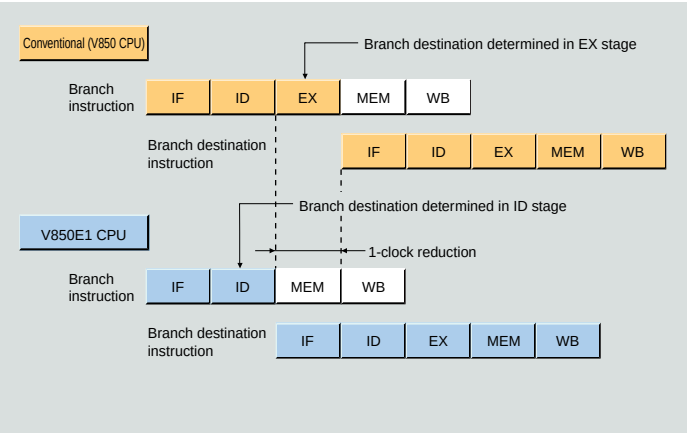
IF (instruction fetch) : Fetches instructions and increments the fetch pointer.
ID (Instruction decode) : Decodes instructions, creates immediate data, and reads registers.
EX (ALU, multiplier, barrel shifter execution) : Executes decoded instructions.
MEM (Memory access) : Accesses memory of corresponding addresses.
WB (Writeback) : Writes execution results to registers.
DF (data fetch) : Transfers execution data to WB stage.

●Non-blocking load/store

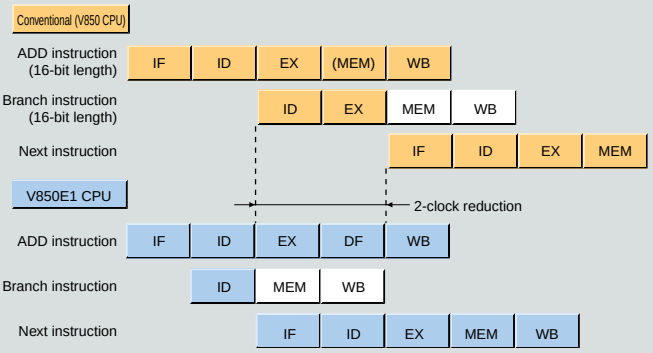


●Addition of branch/load pipes

•Pipeline operation with branch instruction

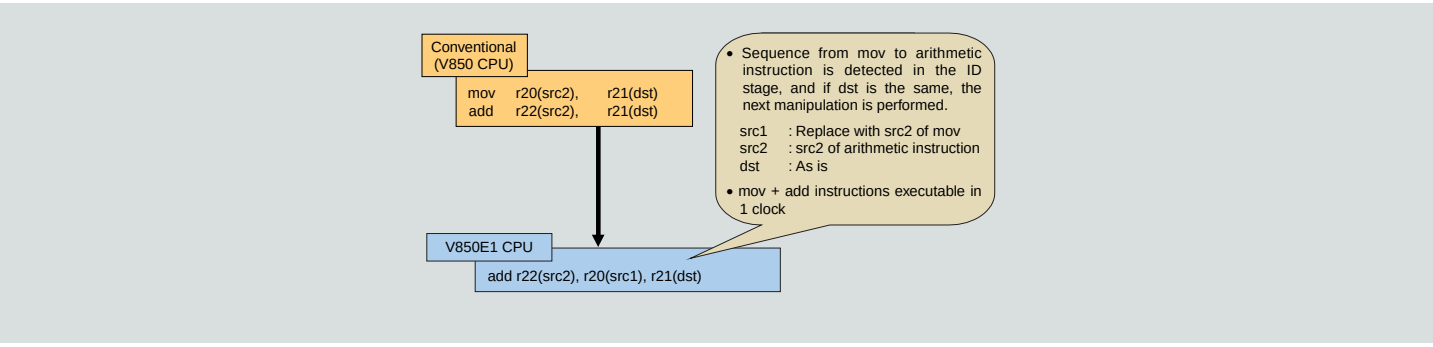


•Parallel instruction execution (when executed by internal ROM)



* The next branch instruction code is also fetched due to the internal 32-bit bus.

●Shift to 3-operand manipulations in 1 slot



● Addition of high-level language compatible instructions

The V850E1 and V850ES cores have enhanced the instruction set of the V850 core as follows.

◆ switch (2 bytes)
- C language switch statement processing converted into instruction

◆ callt (2 bytes)/ctret (4 bytes)
- Table-reference branching
- Reducing size of call code that frequently appears

◆ Data conversion instructions (2 bytes)
- char, short type cast executed with 1 instruction
- sxh, sxb, zxb, and zxh instructions

◆ prepare/dispose (4 bytes)
- Function start/end processing executed in 1 instruction

◆ unsigned Load
- Reduction of unsigned manipulation code

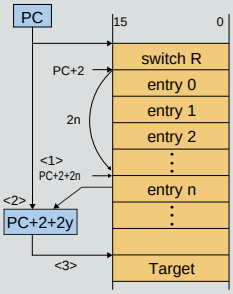
◆ mov imm32, reg (6 bytes/2 clocks)
- Reduction of address setting code

◆ mul/mulu (4 bytes)
- Reduction of array address calculation
- Improvement of sum-of-products performance

◆ Other
- Bit manipulation (register indirect bit specification)
- cmov (Conditional Move), divide (div/divu/divhu)
- sasf, endian conversion

switch R (table-reference branching)

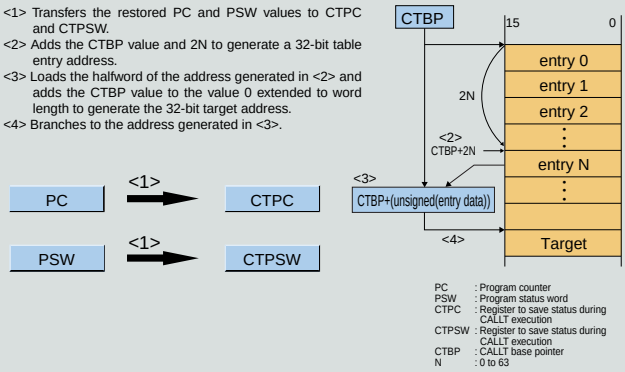
<1> Adds the table start address and double the register value.
<2> Sign extends halfword entry data indicated by the address generated in <1> to word length, doubles it, and adds the table start address to generate a 32-bit address.
<3> Branches to target address generated in <2>.



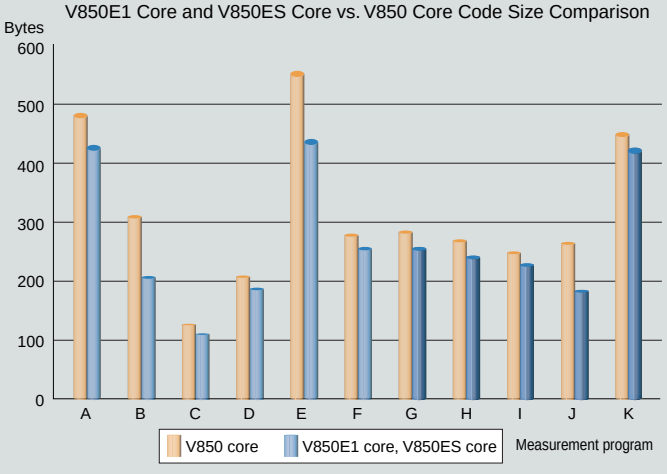
Item \ CPU	V850E1	V850
Coding example	switch r10	movhi hi (L267), zero, r9 movea lo (L267), r9, r9 shl 1, r10 add r9, r10 ld.h 0[r10], r10 add r9, r10 jmp [r10]
Object size	2 bytes	22 bytes
Execution time	5 clocks	9 clocks

callt N (Table-reference subroutine calling)

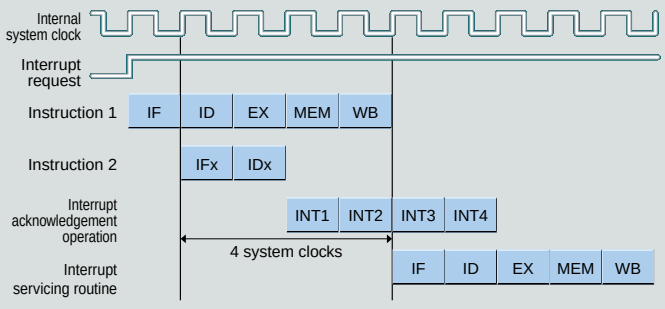
<1> Transfers the restored PC and PSW values to CTPC and CTPSW.
<2> Adds the CTBP value and 2N to generate a 32-bit table entry address.
<3> Loads the halfword of the address generated in <2> and adds the CTBP value to the value 0 extended to word length to generate the 32-bit target address.
<4> Branches to the address generated in <3>.



V850E1 Core and V850ES Core vs. V850 Core Code Size Comparison



Interrupt Response Time



System registers for saving the PC and PSW are provided and high-speed branching to the interrupt program is performed, except under the following conditions.
- In IDLE/STOP mode
- In case of consecutive interrupt request non-sample instructions
- During external bus access
- During access to the interrupt control register

Remark INT1 to INT4 : Interrupt acknowledgement processing
IFx : Invalid instruction fetch
IDx : Invalid instruction decode

Middleware Performance

■Measurement conditions

●Common

CPU : V850 core (33 MHz)
Measurement results are frequency-converted values (50 MHz).
Bus width : 16 bits
Number of waits : 1
(The basic bus cycle is 3 clocks, so 1 bus cycle = 4 clocks.)
Compiler : CA850
Tool : V850 in-circuit emulator (IE) (product of NEC)

●MH/MR/MMR

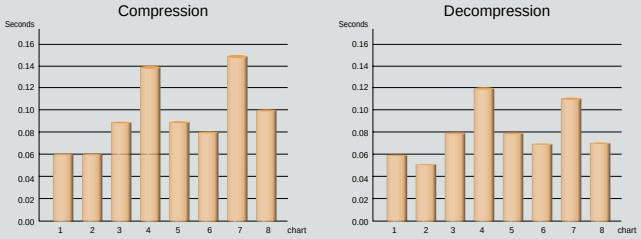
- Internal ROM : Program
- External memory (SRAM) : Encoding/decoding table, change point table, stacks (including I/O parameters)

●JBIG

- Internal ROM : Program (including probability assumption table (1 KB))
- External memory (SRAM) : Learning table, stacks (including I/O parameters)

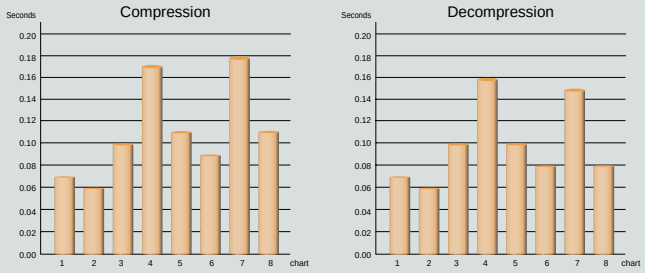
V850 MH Method — A4 100 dpi

	chart1	chart2	chart3	chart4	chart5	chart6	chart7	chart8
Compression	0.06s	0.06s	0.09s	0.14s	0.09s	0.08s	0.15s	0.10s
Decompression	0.06s	0.05s	0.08s	0.12s	0.08s	0.07s	0.11s	0.07s



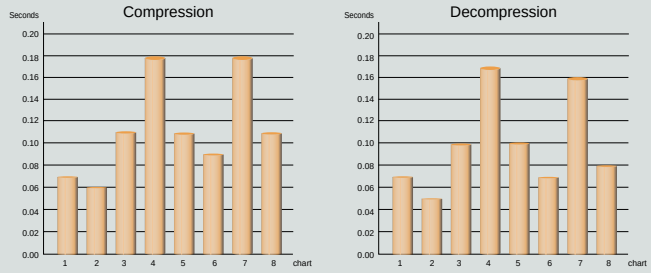
V850 MR (K = 4) Method — A4 100 dpi

	chart1	chart2	chart3	chart4	chart5	chart6	chart7	chart8
Compression	0.07s	0.06s	0.10s	0.17s	0.11s	0.09s	0.18s	0.11s
Decompression	0.07s	0.06s	0.10s	0.16s	0.10s	0.08s	0.15s	0.08s



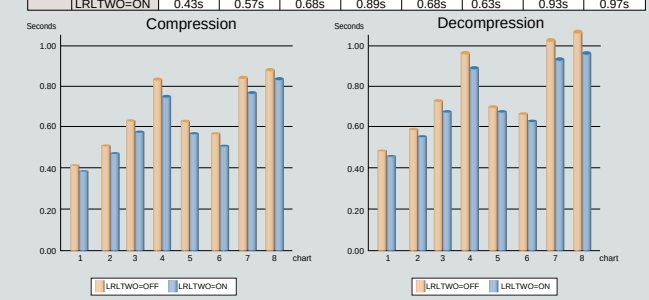
V850 MMR Method — A4 100 dpi

	chart1	chart2	chart3	chart4	chart5	chart6	chart7	chart8
Compression	0.07s	0.06s	0.11s	0.18s	0.11s	0.09s	0.18s	0.11s
Decompression	0.07s	0.05s	0.10s	0.17s	0.10s	0.07s	0.16s	0.08s



V850 JBIG Method — A4 100 dpi
(Layer=Lowest, TPBON=ON, AT=default)

		chart1	chart2	chart3	chart4	chart5	chart6	chart7	chart8
Compression	LRLTWO=OFF	0.41s	0.52s	0.63s	0.84s	0.62s	0.57s	0.85s	0.90s
	LRLTWO=ON	0.38s	0.48s	0.58s	0.76s	0.57s	0.52s	0.78s	0.83s
Decompression	LRLTWO=OFF	0.46s	0.59s	0.73s	0.96s	0.72s	0.67s	1.02s	1.04s
	LRLTWO=ON	0.43s	0.57s	0.68s	0.89s	0.68s	0.63s	0.93s	0.97s



●JPEG

Internal ROM : Program
Internal RAM : Stack, work area (one part)
External memory (SRAM) : Data and remaining work area
Data I/O : RGB

V850 JPEG Method

Sample ratio	Processing Time			
	QVGA(320×240×24)		VGA(640×480×24)	
	Compression	Decompression	Compression	Decompression
4 : 1 : 1 (Quality75)	0.27s	0.21s	1.09s	0.85s
4 : 2 : 2 (Quality75)	0.33s	0.26s	1.33s	1.04s

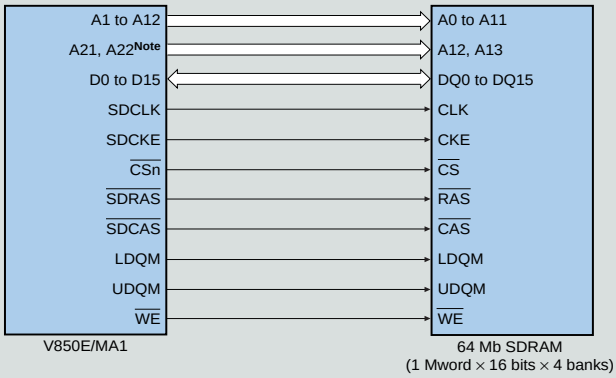
Variety of Peripheral Functions

Memory Access Functions

■SDRAM controller

Products: V850E/MA1, MA2

- ◆ SDRAM connectable without external circuit
- ◆ CAS latency: 2, 3 supported
- ◆ CBR refresh, CBR self refresh supported

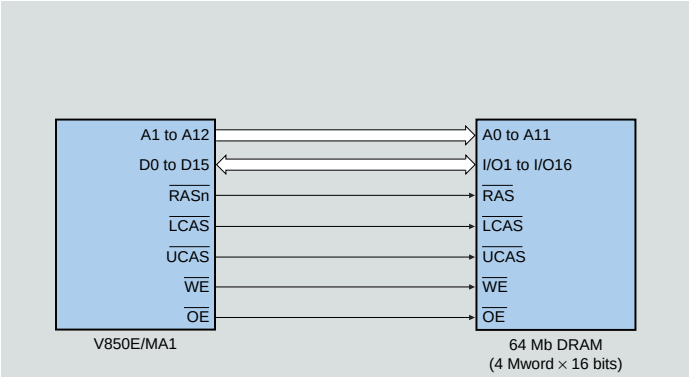


Note The address signal used differs depending on the SDRAM product.

■DRAM controller

Products: V850E/MS1, MS2, MA1

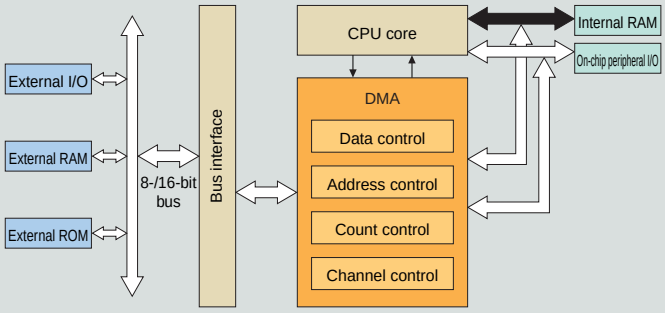
- ◆ EDO DRAM directly connectable without external circuit
- ◆ 2CAS type DRAM supported
- ◆ CBR refresh, CBR self refresh supported



■DMA controller (provided in V850E products)

Products: V850E/MA1, MA2, MS1, MS2, IA1, IA2

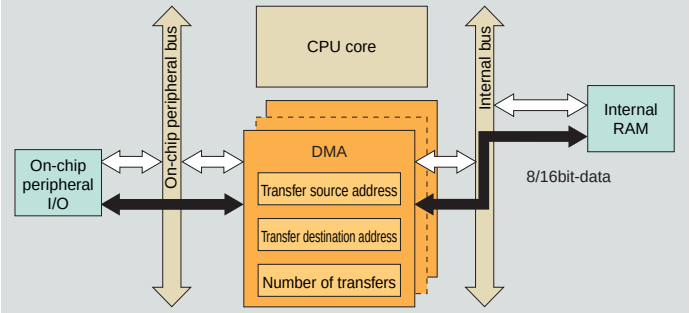
- ◆ Transfer targets: Memory-peripheral I/O, memory-memory
- ◆ Single, single step, block transfer
- ◆ 8-/16-bit data units
- ◆ Transfer type: 1-cycle transfer, 2-cycle transfer
- ◆ Number of transfers: 65,536 Max.



■DMA controller (provided in V850/Sxx products)

Products: V850/SA1, SB1, SB2, SV1, SF1, SC1, SC2, SC3

- ◆Transfer targets: Internal RAM-on-chip peripheral I/O
- ◆Single transfer
- ◆ 8-/16-bit data units
- ◆Transfer clock: 4 clocks Min.
- ◆Number of transfers: 256 Max.

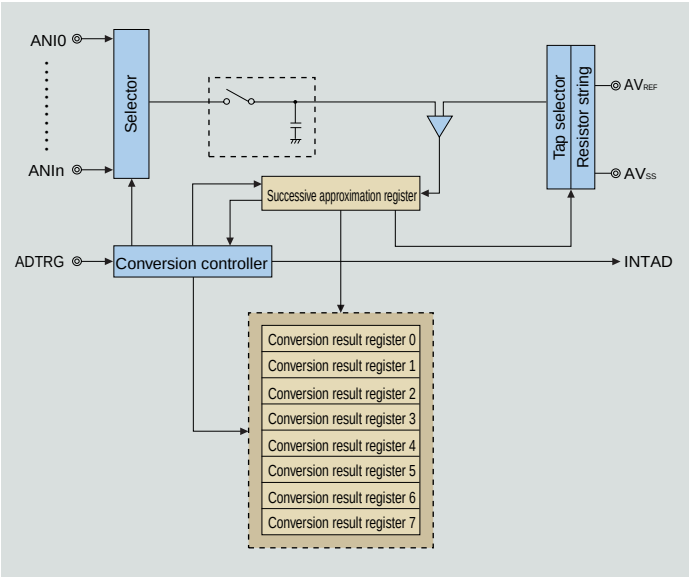


A/D Converters

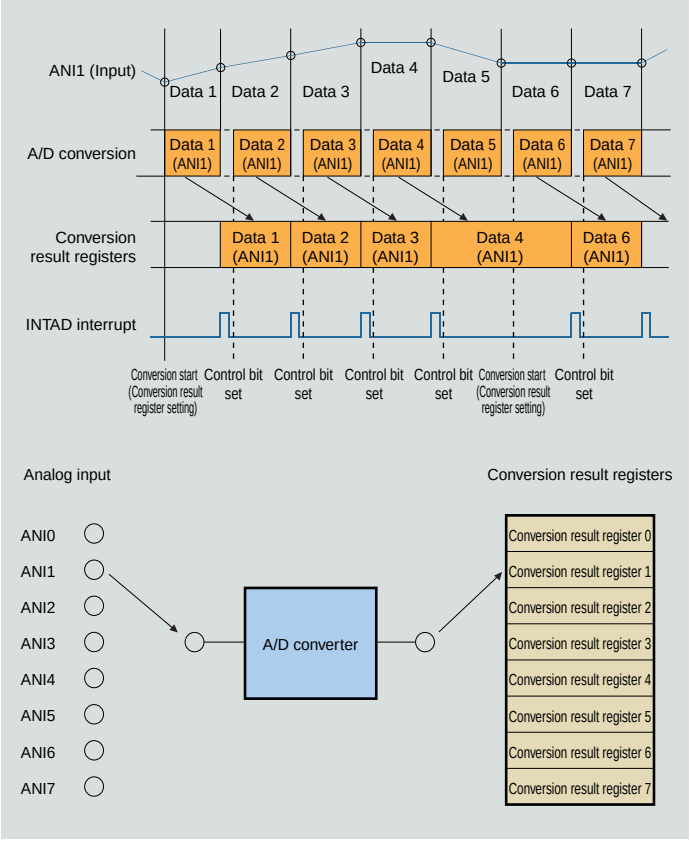
■Multi-stage buffer type

Products: V853, V850/SV1, V850E/MA1, IA1, IA2, MS1

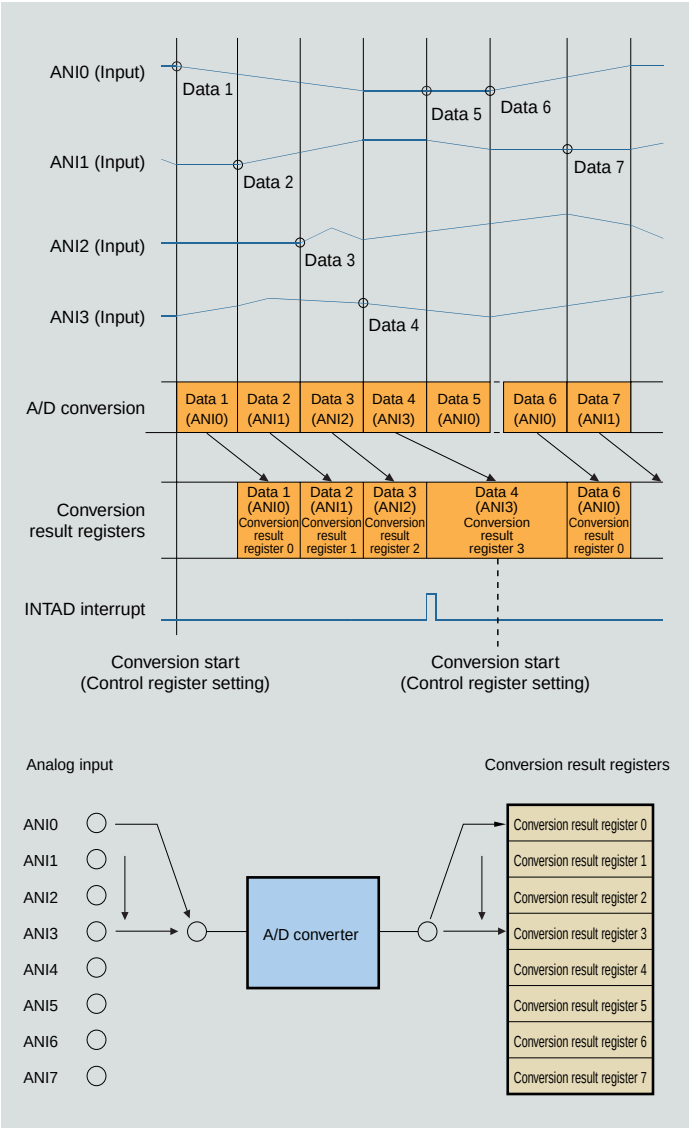
- ◆ Conversion can be started by both software and hardware
- ◆ Eight conversion result registers are incorporated
- ◆ Select/scan modes can be switched



■Select mode operation



■Scan mode

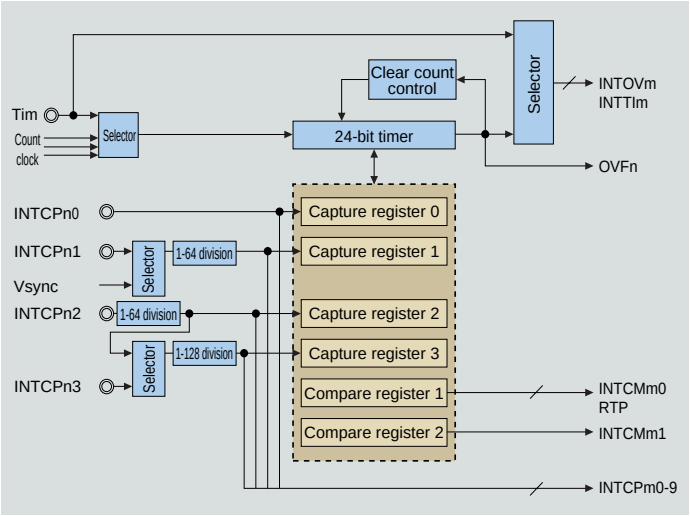


Timer/Counter Functions

■24-bit servo timer

Product: V850/SV1

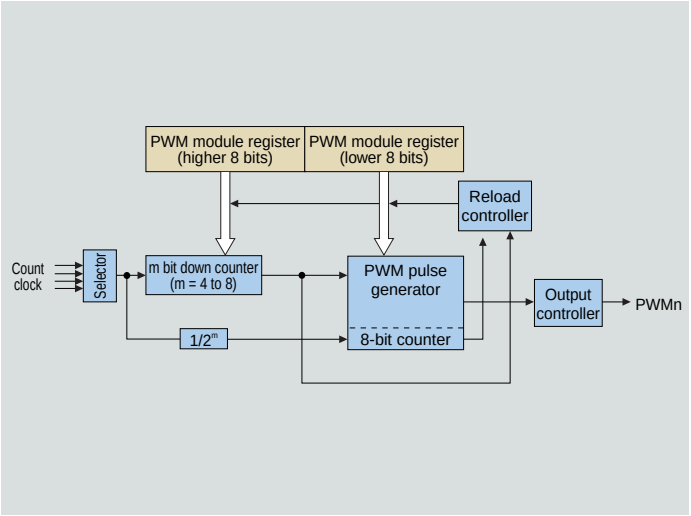
- ◆ 24-bit timer unit for servo control
- ◆ Capture registers: 4
  Compare registers: 2
- ◆ External input detector with 1-64/1-128 divider



■PWM

Product: V850/SV1

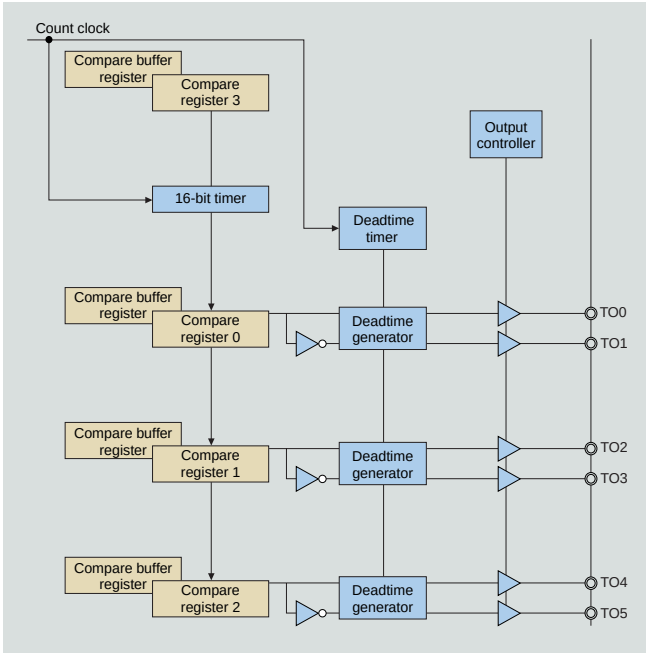
- ◆ 12- to 16-bit PWM output
- ◆ Main pulse + additional pulse configuration
  Main pulse: 4/5/6/7/8 bits
  Additional pulse: 8 bits
- ◆ Active level of PWM output pulse selectable



■3-phase inverter control timer

Products: V850E/IA1, IA2

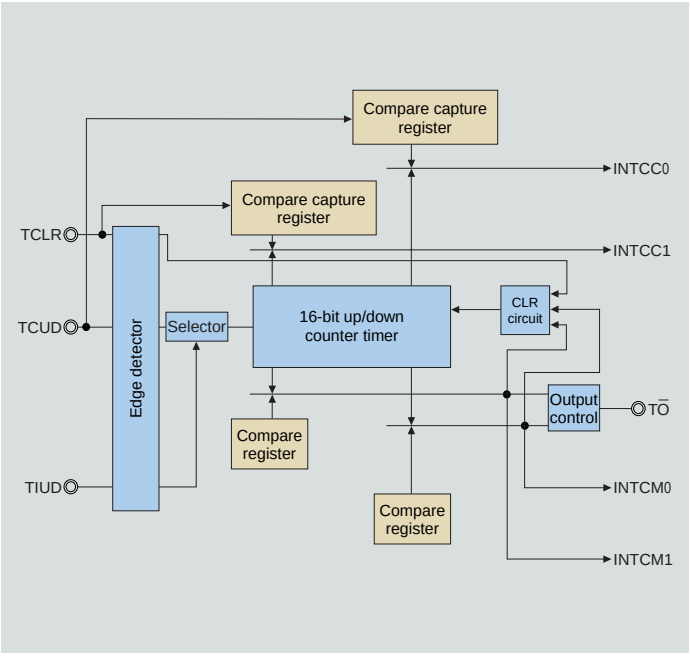
- ◆ 3-phase PWM output function
  Symmetric triangular wave, asymmetric triangular wave, sawtooth wave
- ◆ Interrupt culling function
  Culling rate: 1/1, 1/2, 1/3, 1/4, 1/8, 1/16
- ◆ 3-phase PWM forcible output stop function
- ◆ Real-time output function



■Up/down counter

Products: V850E/IA1, IA2

- ◆ 16-bit 2-phase encoder input supported
- ◆ Compare registers: 2
- ◆ Capture/compare registers: 2

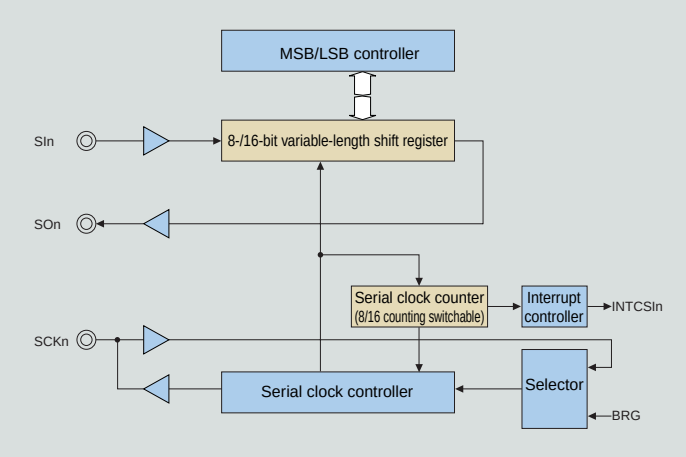


Serial Interface

■Variable-length serial interface

Products: V850/SB1, SB2, SV1, SF1, SC1, SC2, SC3

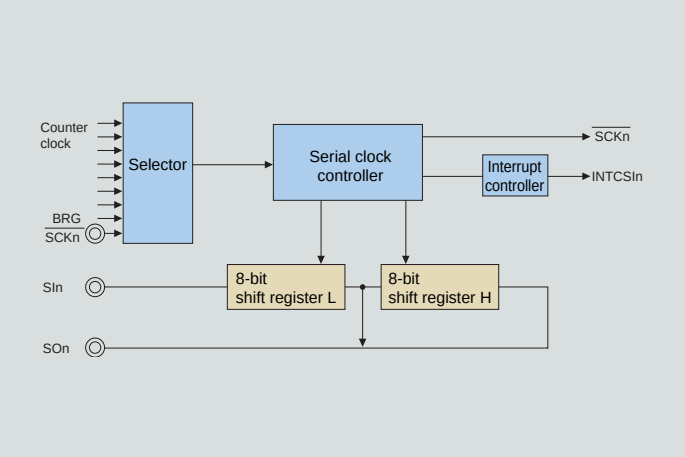
- ◆ 3-wire serial I/O
- ◆ Data length switchable between 8 bits and 16 bits
- ◆ Start bit switchable between MSB and LSB



■8-/16-bit serial interface

Products: V850/SC1, SC2, SC3, V850E/IA1, IA2

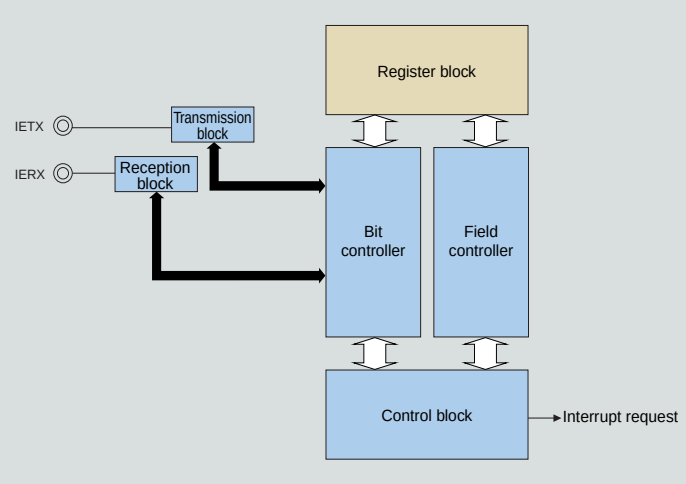
- ◆ 3-wire serial I/O
- ◆ Data length switchable between 8 bits and 16 bits
- ◆ Start bit switchable between MSB and LSB



■IEBus controller

Products: V850/SB2, SC2

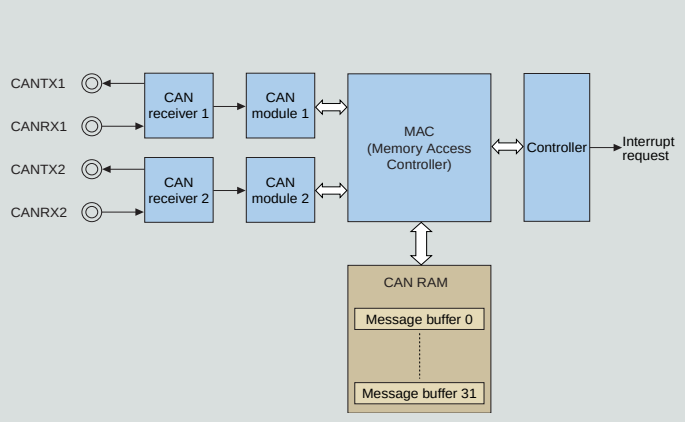
- ◆ Supports communication mode 1
- ◆ Maximum number of transfer bytes: 32 bytes/frame
- ◆ Maximum transfer speed: Approx. 17 Kbps



■CAN

Products: V850E/IA1, V850/SF1, SC3

- ◆ CAN protocol Ver. 2.0 Part B
  (Transmission/reception of standard and extended frames)
- ◆ Maximum transfer rate: 1 Mbps
- ◆ 32 message buffers



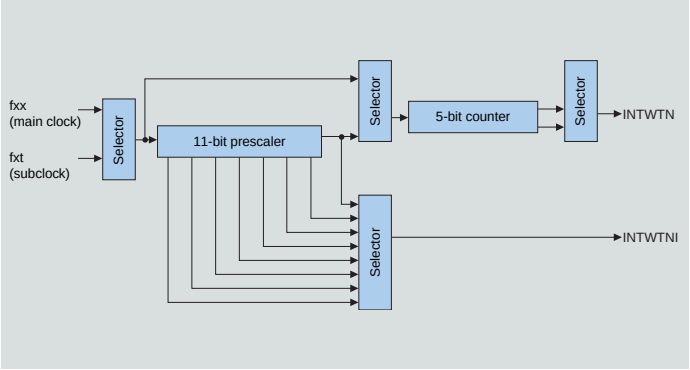
Note The number of channels differs depending on the product.

Distinctive Peripheral Functions of V850

■Watch timer

Products: V850/SB1, SB2, SV1, SC1, SC2, SC3

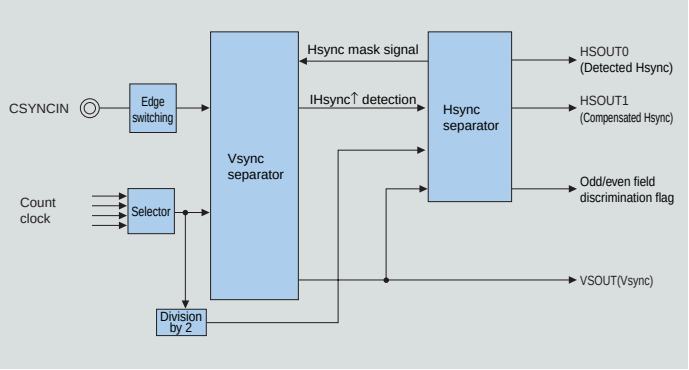
- ◆ 0.5-second interrupt generation using watch timer function
- ◆ Interval timer supported



■Hsync/Vsync separator

Product: V850/SV1

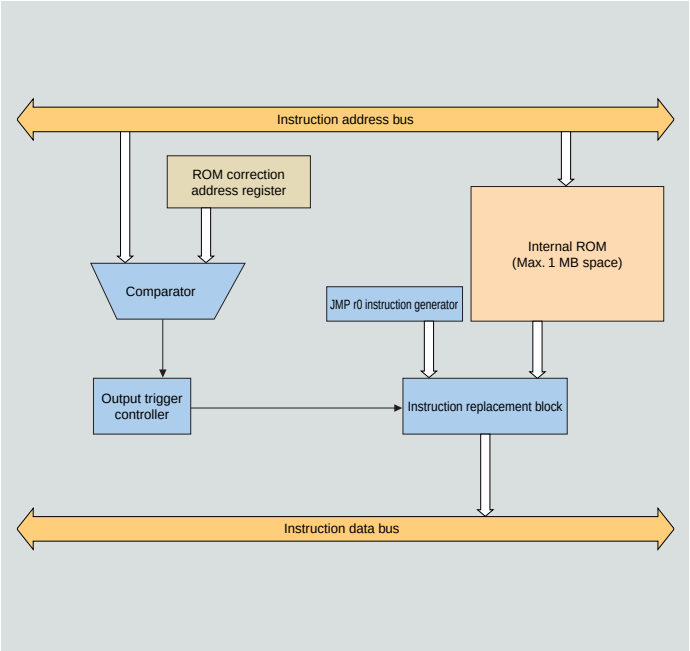
- ◆ Separation of Vsync (vertical) signal and Hsync (horizontal) signal from decoding sync signal of VCR
- ◆ Odd/even field discrimination



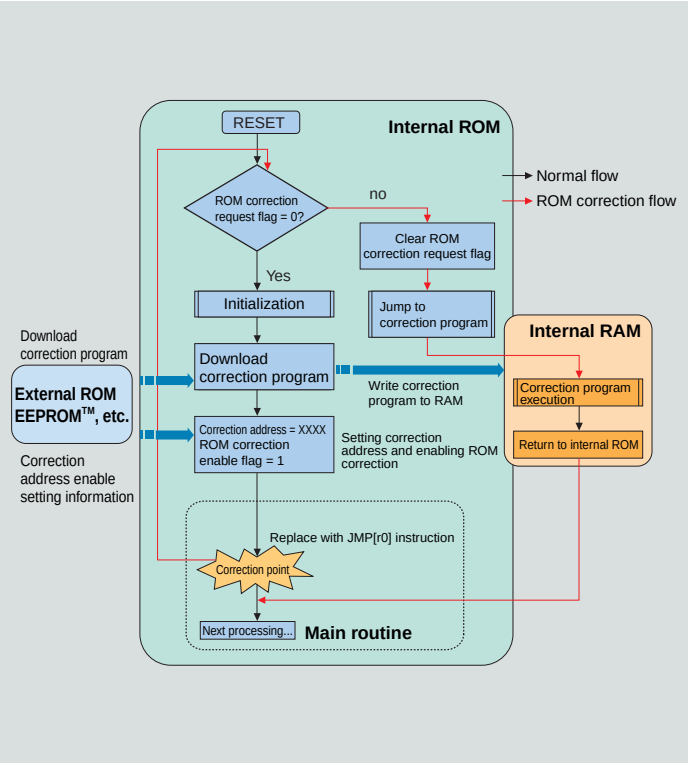
■ROM correction function

Products: V850/SB1, SB2, SV1, SF1, SC1, SC2, SC3

- ◆ Substitutes JMP r0 instruction for instruction of address to be corrected and branches to 0000H
- ◆ Program can be modified following creation of mask ROM
- ◆ Correction addresses: 4 points



■ROM correction operation



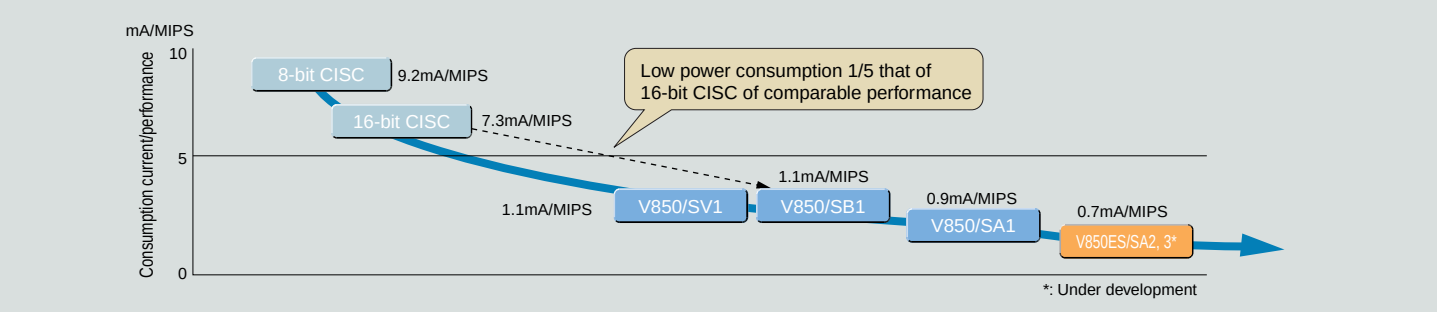
Low Power & Low Noise

Low Power Consumption Measures

Low-power-consuming, high-speed microcontrollers are required for portable devices and battery-operated devices such as DVCs and cellular phones. The V850 Series incorporates various functions to lower the power consumption.

■Superior power performance

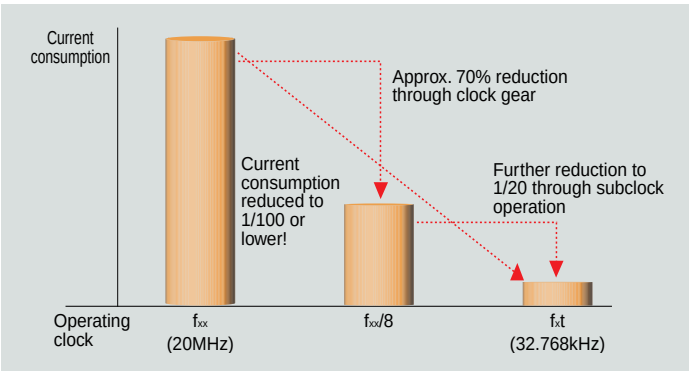
The V850ES and V850/Sxx products feature a thorough power-saving design that realizes a superb power/performance ratio of 1.1 to 0.7 mA/MIPS. As a result, these products realize a low consumption current only one fifth that of a 16-bit CISC microcontroller of comparable performance. By featuring such extremely high power performance, these products enable the simultaneous realization of lower power consumption and more sophisticated functions in various systems.



■Clock gear function

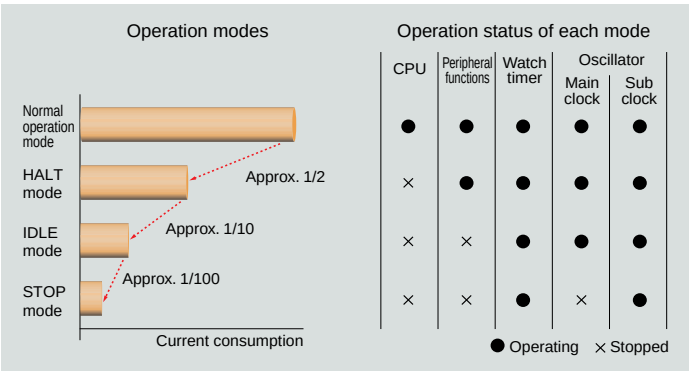
The V850/Sxx products come with two oscillators: a main clock and a subclock. 1/1/, 1/2, 1/4, or 1/8 of the main clock or the subclock[Note] can be selected as the CPU operating clock, making it possible to minimize the power consumption according to the system's operating status.

Note Not selectable in V850/SV1



■Standby mode

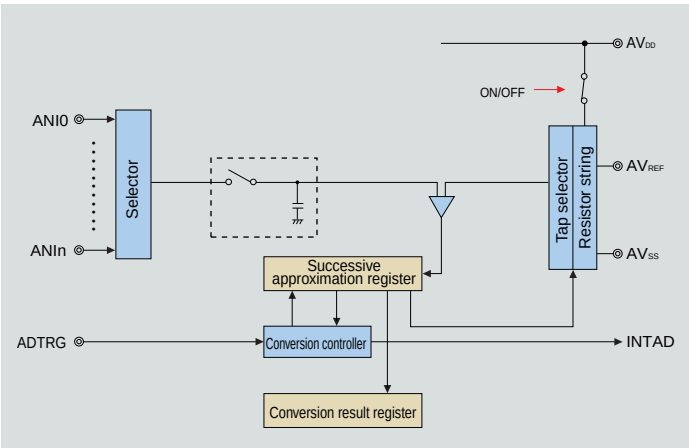
An efficient low-power-consumption system can be realized by using the three standby modes, STOP, IDLE, and HALT, according to the usage purpose.



■Function to cut voltage between A/D converter V_{REF} and resistor string

Voltage application to the A/D converter's resistor string can be switched on and off. The power consumption can be minimized by switching off voltage application to the resistor string when the A/D converter is not used.

- Main products:
  V850/SB1, SB2, SC1, SC2, SC3, SF1



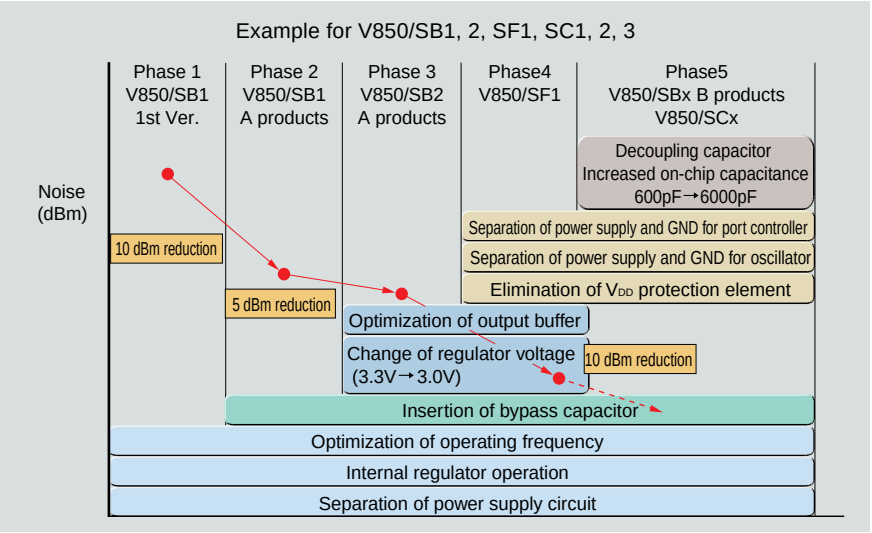
EMI Countermeasures

Minimizing the influence of electromagnetic interference (EMI) from the microcontroller in AV equipment such as car audio systems is a major requirement, making the reduction of EMI one of the highest technological priorities for microcontroller manufacturers. Various EMI countermeasures are implemented in the V850 Series.

■EMI countermeasures for individual chip

Noise reduction measures focussing on the following three points are implemented as noise countermeasures in individual V850 Series chips.

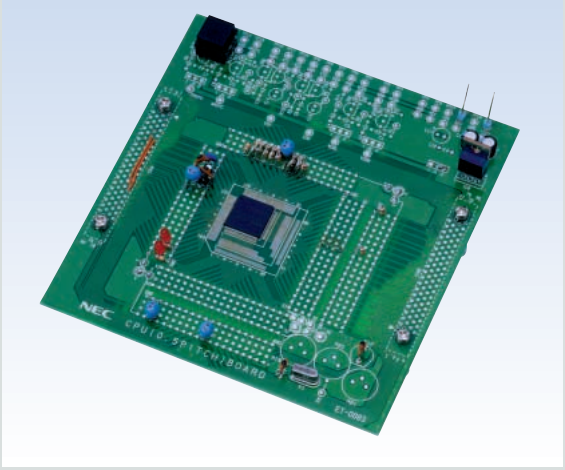
- ◆ Reduction of noise generation
  - • Use of low-voltage internal logic power supply
  - • Optimization of oscillator
- ◆ Reduction of noise propagation
  - • Separation of internal logic sound source and power supply of pins
  - • Reduction of cross talk between different power supply wires
- ◆ Confining of noise inside
  - • On-chip decoupling capacitor between power supply and GND inside microcontroller
  - • Separation of power supply and GND for oscillator



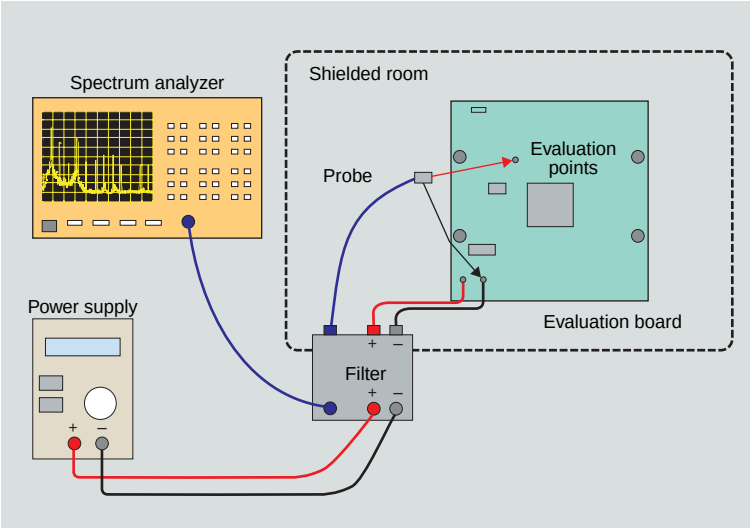
■Standardization of evaluation methods (1/2)

There are no rules regarding the EMI measurement testing method for individual microcontrollers. NEC aims to standardize evaluation circuit constants through the use of a standalone EMI evaluation board and evaluate products in a measuring environment that uses a shielded room and power supply filters. This approach enables the evaluation of different products (8-bit and 16-bit NEC CISC microcontrollers, etc.) in the same environment.

●Standalone EMI evaluation board



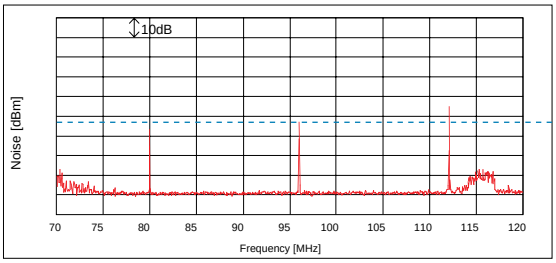
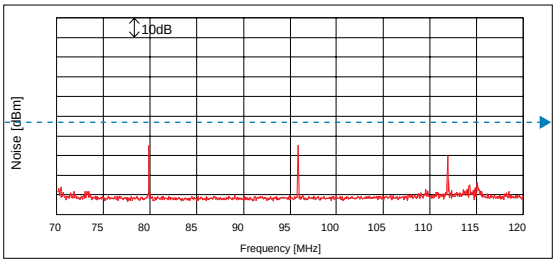
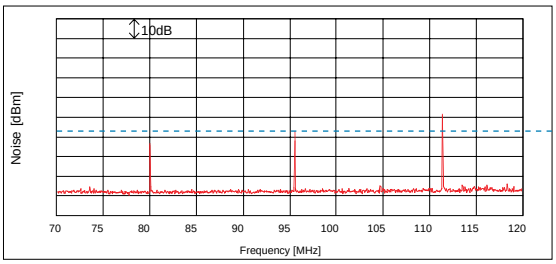
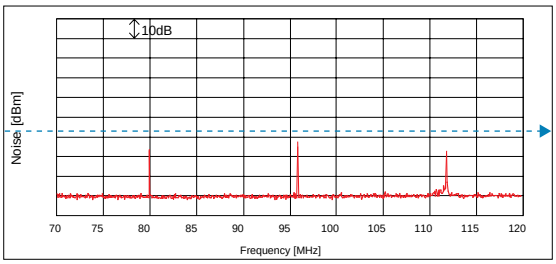
●Standalone EMI evaluation board measurement environment



■Standardization of evaluation methods (2/2)

●EMI evaluation results

A comparison of the EMI evaluation results for Phase 2 products (V850/SB1 A products) and Phase 4 products (V850/SF1) is shown below.

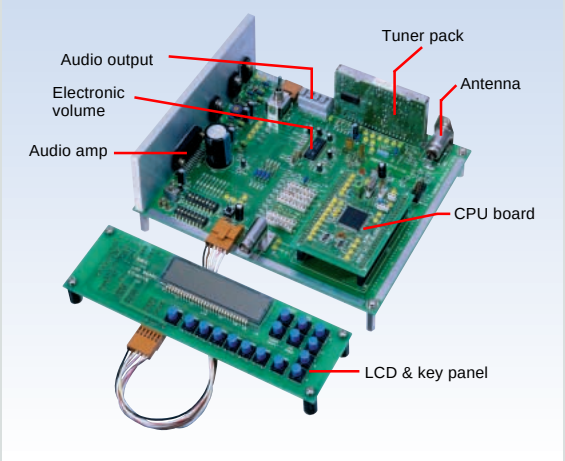
Product Name / Measurement Point	Phase 2 (V850/SB1 A Products)	Phase 4 (V850/SF1)
V_{DD}		
Port		

Remark Oscillation frequency = 16 MHz

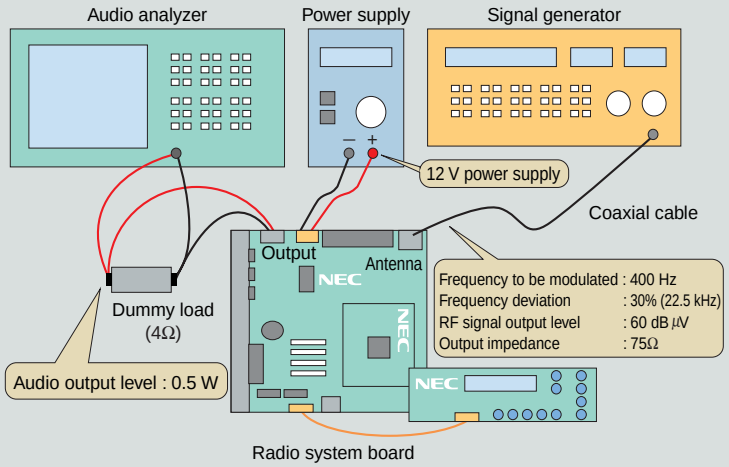
■Evaluation of characteristics using radio system board (1/2)

In addition to EMI measurement using a standalone EMI evaluation board, NEC has also established an evaluation method employing set evaluation criteria using a radio system board. Since the evaluation results obtained with the radio evaluation board match the evaluation method established by the customer, the influence of EMI can be judged directly.

●Radio system board

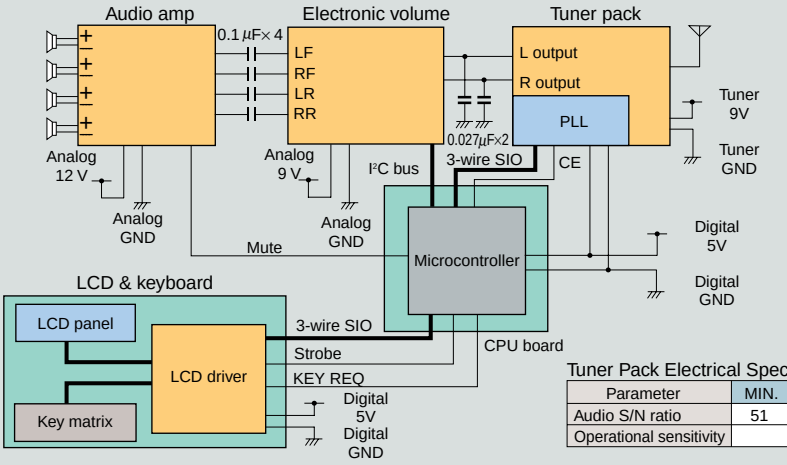


●Radio system board measurement environment



■Evaluation of characteristics using radio system board (2/2)

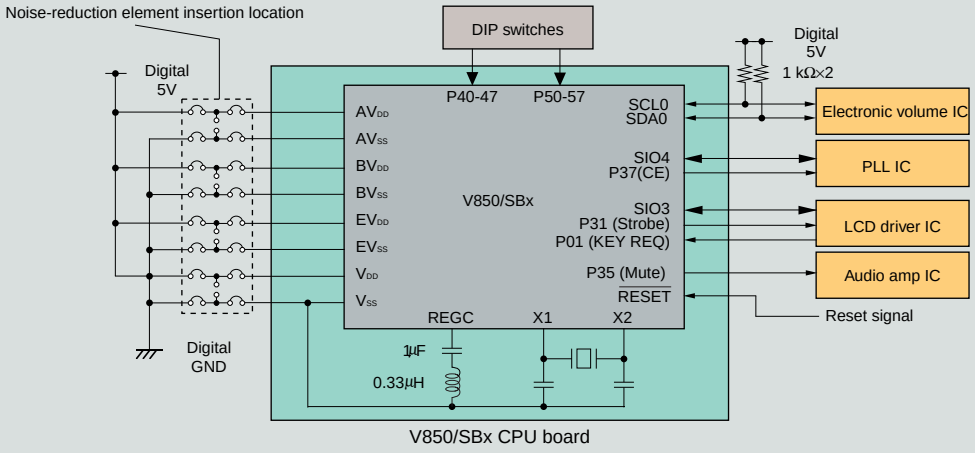
●Radio system board block diagram



Tuner Pack Electrical Specifications

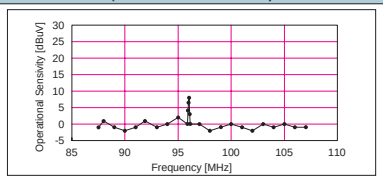
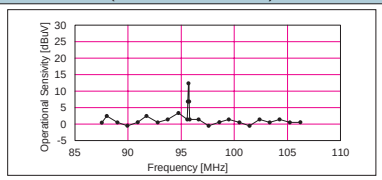
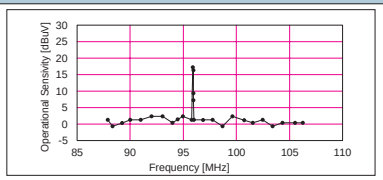
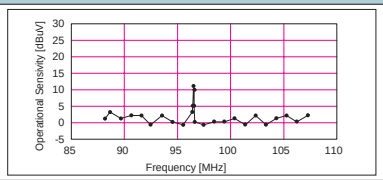
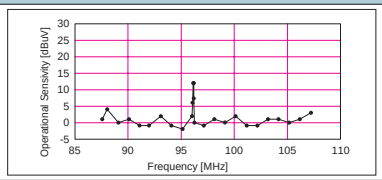
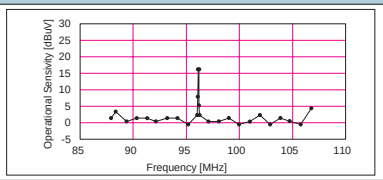
Parameter	MIN.	TYP.	MAX.	Unit
Audio S/N ratio	51	58		dB
Operational sensitivity		6	10	dBμV

●CPU board block diagram



●Results of characteristics evaluation using radio system board

The EMI reduction efficiency can be ascertained with a radio system board in the same way as standalone microcontroller evaluation.

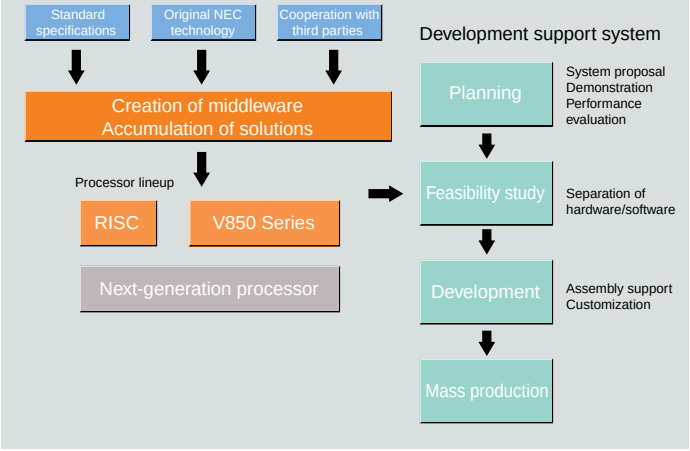
Product Name	Phase 5 (V850/SB1 B Products)	Phase 3 (V850/SB2 A Products)	16-Bit Microcontroller from Other Company
f_{XX}=12MHz			
Product Name	**Phase 4 (V850/SF1)**	**Phase 2 (V850/SB1 A Products)**	**16-Bit Microcontroller from Other Company**
f_{XX}=16MHz			

Remark fxx : Oscillation frequency

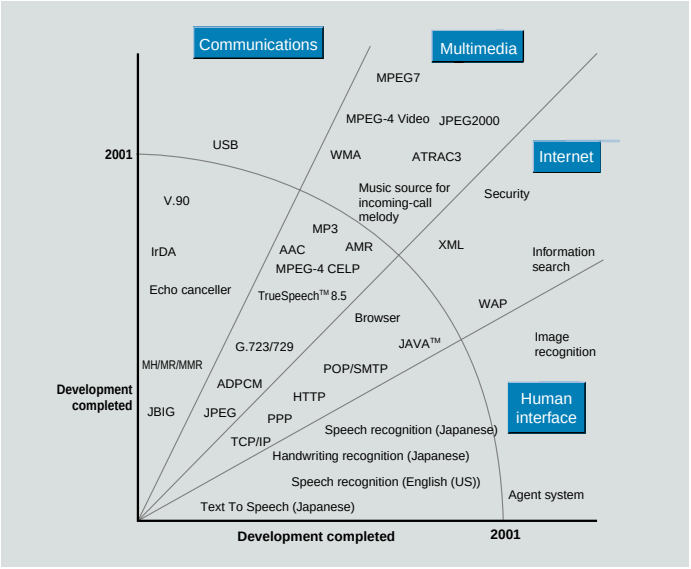
Middleware

Middleware Development System

NEC is developing a range of middleware products suitable to processors for various systems. NEC middleware is realized by original NEC technology, superior third-party technology, and established standards.



Middleware Development



JPEG

- **Conforms to JPEG international standard**

  Conforms to DCT baseline process (non-reverse coding)

- **Versatile compression and decompression processing**

  <Compression functions>

  - User-customizable VRAM input module
  - User-specified Huffman and quantization tables
  - APPn marker insertion
  - Compression suspend function

  <Decompressing processing>

  - User-customizable VRAM output module
  - Support of various JPEG markers (DRI, RSTn, DNL)
  - Decompressing suspend function

JPEG Performance

CPU	Sample Ratio	Processing Time			
		QVGA (320×240×24)		VGA (640×480×24)	
		Compression	Decompression	Compression	Decompression
V850E/MS1 (33MHz)[Note]	4:1:1 (Quality75)	0.32s	0.24s	1.3s	0.97s

Note Programs are placed in internal ROM, and stack and work areas (one part) are placed in internal RAM. Data and the remaining work area are placed in external RAM.

Memory

ROM		RAM	
Compression	Decompression	Compression	Decompression
10KB	7.5KB	5KB	10KB

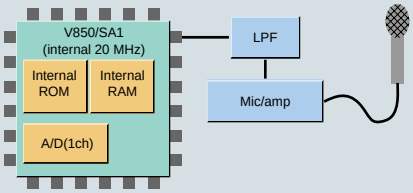
V850 Series Speech Recognition

The V850 Series uses internal memory and peripheral I/Os to realize speech recognition on one chip. This makes this series ideal for applications that require speech recognition in sets with large constraints, such as games and home appliances.

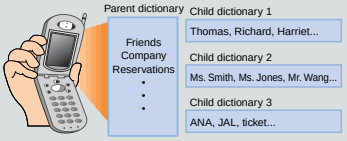
- **Speech recognition realized using just the internal memory and peripheral I/Os of V850 Series**
- **Increased number of recognized words**

  Number of recognized words: 30 (for V850/SA1, 20 MHz)

V850 Series
Speech recognition system
configuration example



Increased number of recognized words



Memory Capacity

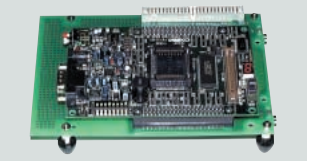
ROM/RAM	Description	Capacity
ROM	Program	Approx. 25 KB
	Table	Approx. 62 KB
	Recognition dictionary (in case of 20 words)	Approx. 0.8 KB [Note1]
RAM	Work area (in case of 20 words)	Approx. 4.0 KB [Note2]
	Stack area	Approx. 0.4 KB

Notes 1. Figure using average of 5 letters per word to calculate standard dictionary size.
2. The variable work area is proportional to the number of recognized words.

- **Speech recognition evaluation system**

  In introducing speech recognition, NEC has provided an environment that allows easy evaluation.

  For details about this system or how to purchase it, contact NEC.



Handwriting Recognition (Japanese Only)

- **Easy to use because of flexibility regarding stroke order and count**
  Pattern matching method based on "non-linear normalization matching method"
  Conversion of pen-drawn lines into image
- **High recognition rate, high-speed recognition**
  Recognition of 95% or higher in 0.1 s (V85x: 25 MHz)
- **Support of up to JIS No. 2 standard**
  JIS No. 1 Standard: Approx. 3,400 characters, JIS No. 2 Standard: Approx. 800 characters
- **New characters can be added (pictographs, etc., can be freely added)**
  A dictionary can be created from character data using a dictionary compilation tool.

ROM/RAM	Description	Capacity
ROM	Program	Approx. 60 KB
	Dictionary data (approx. 4,200 characters)	Approx. 450 KB
	Data	Approx. 60 KB
RAM	Work area	Approx. 32 KB
	Stack area	Approx. 2 KB

Text to Speech (TTS) (For Japanese Text)

- **Speech synthesized from Japanese Kana and Kanji texts (SJIS code)**
- **Versatile speech synthesis**
  Synthesis of male and female voices (2 types)
  Various parameters such as intonation and reading speed can be adjusted.
- **TTS rhythm data (pitch, phoneme duration) can be designed (Support of Speech Designer)**
  TTS using natural rhythm possible (synthesis of more natural sounding speech)
- **Support of characters with special readings (character readings can be set using the user dictionary)**
- **Synthesis speed (V853: 25 MHz)**
  Speech: Between 1.9 s[Note] and 3 s; Text analysis: 163 ms; speech generation: 1,709 ms
  Note Varies depending on the input character string.

ROM/RAM	Description	Capacity
ROM	Program data	Approx. 103 KB
	Dictionary data (approx. 80,000 words)	Approx. 1.2 MB
	Phoneme data	Approx. 670 KB to 1.4 MB
RAM	Work area	Approx. 160 KB
	Stack area	Approx. 256 KB
	Speech output buffer	Approx. 8 KB × n blocks

Middleware Product List

Middleware list

Category	Middleware		V850 Series
Image	MH/MR/MMR		◎
	JBIG		◎
	JPEG		◎
Speech	Text To Speech	Japanese	◎
	Speech CODEC	G.726 (ADPCM)	◎
Recognition	Speech recognition	Japanese (small vocabulary)	◎
	Speech recognition	English (US) (small vocabulary)	○
	Handwriting recognition	Japanese (input frame required)	◎
Internet	Browser		◎
	TCP/IP		◎
Drivers	IrDA protocol stack		◎
	USB		△
	IEEE1394		○
	PCMCIA/CF card		○
	PC-compatible file system		○
Other	Font		◎

Remarks 1. ◎: Development completed; ○: Under development; △: In planning
2. Third-party products included.
3. For details about middleware products, refer to the following
http://www.ic.nec.co.jp/apsoft/english/middle_top.html

Middleware performance

Middleware	Performance	Power(MIPS)	ROM	RAM
MH/MR/MMR	MH Chart1 : Enc0.12s/Dec0.08s	—	64 KB	200 bytes
JBIG	Chart1 : Enc0.73s/Dec0.83s	—	21 KB	2.6 KB
JPEG	QVGA × 24 : Enc0.32s/Dec0.24s	—	17.5 KB	15 KB
G.726(ADPCM)	32Kbps, 16Kbps	Enc8/Dec8.2	9 KB	80 bytes
Speech recognition (small vocabulary)	0.4s	19 (20 words)	82 KB	3.5 KB
		63 (100 words)		(15 words)
Handwriting recognition (Japanese, input frame required)	0.1s/character	14	570 KB	34 KB
IrDA protocol stack	—	—	60 KB	16 KB

Flash Memory Microcontrollers

Features

To answer the need for shorter development time and maintenance after shipping, NEC offers microcontrollers with on-chip flash memory available in a large range of capacities from 128 KB to 512 KB as part of the V850 Series. NEC's flash memory microcontrollers offer the following features.

- ◆ Support of batch rewrite of entire memory and rewrite in area units
- ◆ Flash memory programming with self-rewrite in area units
- ◆ Support of on-board programming through serial communication using a flash memory programmer
- ◆ Erase/write voltage: 2.5 V, 7.8 V, 10.3 V

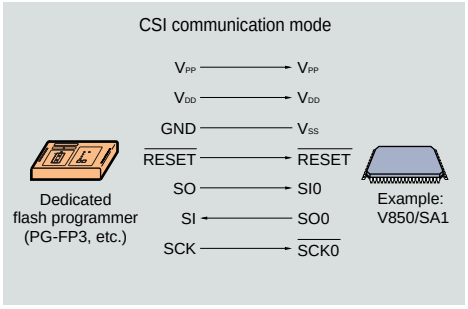
Flash Memory Size (Bytes)	128K		256K			384K	512K
RAM Size (Bytes)	4K	6K	8K	10K	16K	16K	24K
V850E/MA1				○			
V850E/IA1				○			
V850E/IA2		○					
V850E/MS1	○						
V853	○		○				
V850/SA1	○		○				
V850/SV1					○	○	
V850/SB1					○		○
V850/SB2					○		○
V850/SF1					○		
V850/SC1							○
V850/SC2							○
V850/SC3							○
V850ES/SA2*					○		
V850ES/SA3*					○		

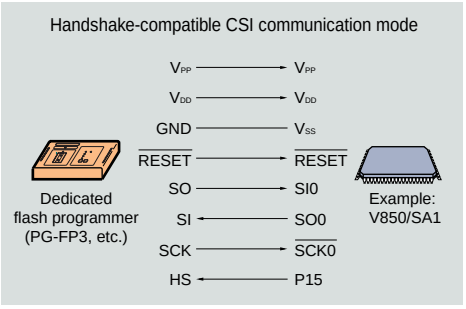
* : Under development

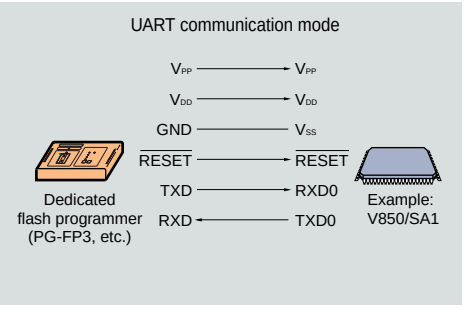
Rewrite Mode

The V850 Series supports a programmer rewrite mode that uses serial communication supporting on-board programming, as well as a self-programming mode that rewrites flash memory with user programs, to enable continuous use from development to maintenance.

■Programmer rewrite mode

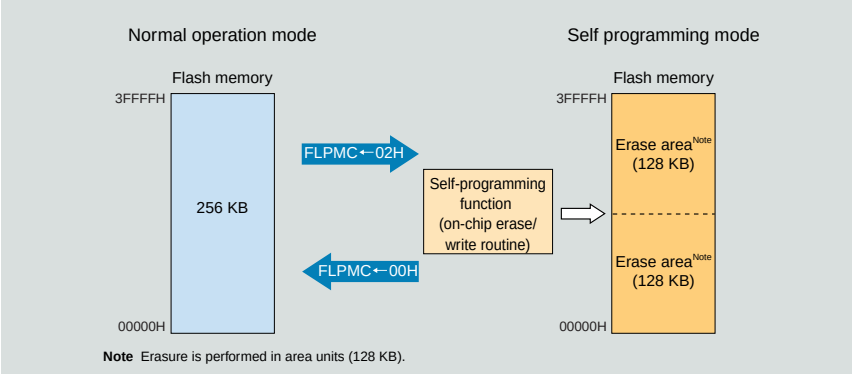






■Self-Programming Mode

Flash memory can be erased and rewritten by calling a self-programming function (device-internal processing) using a self-programming interface, from a program placed in an area other than the flash memory. The self-programming function is called by switching from the normal operation mode to the self-programming mode using the flash programming mode control register (FLPMC).



Note Erasure is performed in area units (128 KB).

Specifications

Part No.	Flash Memory Capacity	Power Supply Voltage	Max. Operating Frequency	Package	Rewrite Voltage		Rewrite Mode	W/E Count
					V_{DD}	V_{PP}		
V850E/MA1	256 KB	3.0 to 3.6 V	50 MHz	144-pin LQFP (20 × 20mm)	3.3 V	7.8 V	CSI, HS-compatible CSI	100
				161-pin FBGA (13 × 13mm)				
V850E/IA1	256 KB	3.0 to 3.6 V (Internal unit)	50 MHz	144-pin LQFP (20 × 20mm)	3.3 V	7.8 V	CSI, UART, HS-compatible CSI	100
		4.5 to 5.5 V (External pin)						
V850E/MS1	128 KB	3.0 to 3.6 V	33 MHz	144-pin LQFP (20 × 20mm)	3.3 V	7.8 V	CSI, UART, HS-compatible CSI	100
				157-pin FBGA (14 × 14mm)				
	128 KB	3.0 to 3.6 V (Internal unit)		144-pin LQFP (20 × 20mm)				
		4.5 to 5.5 V (External pin)						
V853	128 KB	4.5 to 5.5 V	33 MHz	100-pin LQFP (14 × 14mm)	5 V	10.3 V	CSI, UART, HS-compatible CSI	20
	256 KB			100-pin LQFP (14 × 14mm)				
V850/SA1	128 KB	3.0 to 3.6 V	20 MHz	100-pin LQFP (14 × 14mm)	3.3 V	7.8 V	CSI, UART, HS-compatible CSI	100
	256 KB			100-pin LQFP (14 × 14mm)				
				121-pin FBGA (12 × 12mm)				
V850/SV1	256 KB	3.1 to 3.6 V	20 MHz	176-pin LQFP (24 × 24mm)	3.3 V	7.8 V	CSI, UART, HS-compatible CSI	100
				180-pin FBGA (13 × 13mm)				
	384 KB			180-pin FBGA (13 × 13mm)				
V850/SB1	256 KB	4.0 to 5.5 V	20 MHz	100-pin LQFP (14 × 14mm)	3.3 V	7.8 V	CSI, UART, HS-compatible CSI	100
				100-pin QFP (14 × 20mm)				
	512 KB			100-pin QFP (14 × 20mm)				
V850/SB2	256 KB	4.0 to 5.5 V	13 MHz	100-pin LQFP (14 × 14mm)	3.3 V	7.8 V	CSI, UART, HS-compatible CSI	100
				100-pin QFP (14 × 20mm)				
	512 KB			100-pin QFP (14 × 20mm)				
V850/SF1	256 KB	4.0 to 5.5 V	16 MHz	100-pin LQFP (14 × 14mm)	3.3 V	7.8 V	CSI, UART, HS-compatible CSI	100
				100-pin QFP (14 × 20mm)				
V850/SC1, SC2, SC3	512 KB	4.0 to 5.5 V	20 MHz	144-pin LQFP (20 × 20mm)	3.3 V	7.8 V	CSI, UART, HS-compatible CSI	100
V850ES/SA2*	256 KB	2.3 to 2.7 V	17 MHz	100-pin LQFP (14 × 14mm)	2.5 V	2.5 V	CSI, UART	100
V850ES/SA3*	256 KB	2.3 to 2.7 V	17 MHz	121-pin FBGA (12 × 12mm)	2.5 V	2.5 V	CSI, UART	100

* : Under Development

Flash Memory Programmers

■NEC flash memory programmer (PG-FP3)

[Features]

- ◆ Supports write to all NEC microcontrollers with dual-power supply flash memory
- ◆ Device-specific information required for writing can be automatically set with parameter files.
- ◆ Supports both on-board writing and program adapter writing.
- ◆ Easy-to-carry A5 size
- ◆ Simple operation either on standalone basis or with a dedicated application (Flashpro III) on Windows™ 95, 98, 2000, or Windows NT™ Ver. 4.0

  <Standalone>

  Executed in one of the following modes: PROMLOAD, ERASE, PROGRAM, VERIFY, E.P.V.

  <On Windows>

  Operated via GUI screen.

■Third-party flash memory programmers (1/2)

●Programming system Y1000-8

[Manufacturer/Marketing] Wave Technology Co., Ltd.

[Target Devices] V850E/MA1, V850/SV1

[Features]

- ◆ Gang programmer enabling simultaneous programming and verification of up to 8 devices
- ◆ Enables reading of master data directly from floppy disk to internal memory.
- ◆ Data dump display and editing functions
- ◆ Master data storable on internal hard disk
- ◆ Emphasizes simple and comfortable operation via touch panel and workability via PASS/FAIL display, check-sum display, and task count display supporting sockets

[Additional information]

TEL: +81-3-5304-1885

FAX: +81-3-5304-1886

E-mail: sales@y1000.com

Website: http://www.y1000.com/en/index.html

●Flashpro III FL-PR3

[Manufacturer/Marketing] Naito Densei Machida Mfg. Co., Ltd.

[Target Devices] V850 Series

[Features]

- ◆ Supports writing to all NEC microcontrollers with dual-power supply flash memory
- ◆ Device-specific information required for writing can be automatically set with parameter files.
- ◆ Supports both on-board writing and program adapter writing.
- ◆ Easy-to-carry A5 size
- ◆ Simple operation either on standalone basis or with a dedicated application (Flashpro III) on Windows 95, 98, 2000, or Windows NT Ver. 4.0

[Additional Information]

FAX: +81-45-475-4091

E-mail: info@ndk-m.co.jp

Website: http://www.ndk-m.co.jp/eng/index.html

■Third-party flash memory programmers (2/2)

●NET IMPRESS

[Manufacturer/Marketing] Yokogawa Digital Computer Corporation
[Target Devices] V850E/IA1, V850/SB1 (μPD70F3033A)
[Features]
This in-circuit programmer for flash memory microcontrollers (NET IMPRESS) is used to program the microcontrollers with on-chip flash memory of each company, which have various writing specifications, while solder mounted on the user system board.
This programmer comes in four models (AF220, AF210, AF120, AF110) to be used according to the intended application field.

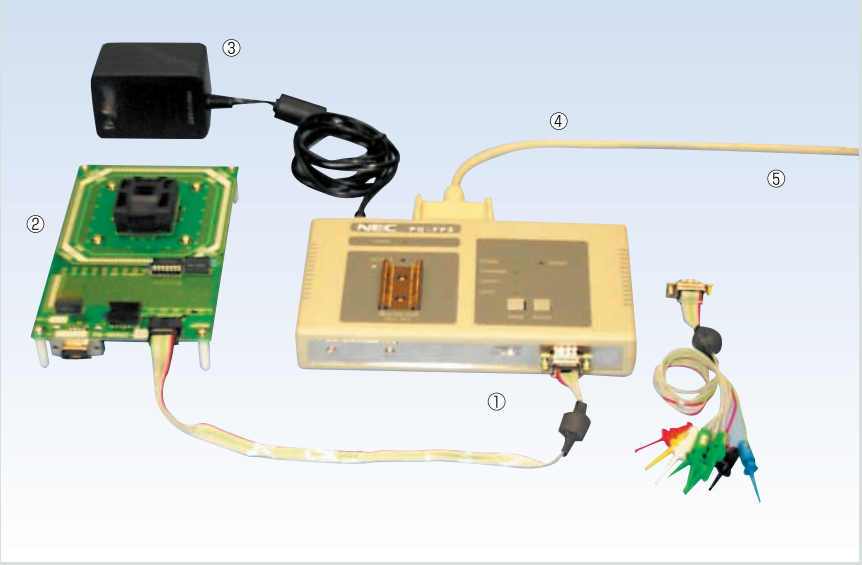
- ◆ One control module is the key to this product's versatility.
  Microcontrollers of the same family are supported by changing parameters, and microcontrollers of different families are supported by purchasing the license for the descriptor part.
- ◆ Can be used on standalone basis as well as via a host machine.
- ◆ Rich lineup of freeware

[Additional Information]
TEL : Japan +81-42-333-6224
U.S.A +408-244-1932
Europe +44-1256-811998
FAX : Japan +81-42-352-6109
U.S.A +408-244-1881
Europe +44-1256-811761
E-mail : info@advice.ydc.co.jp
Website : http://www.ydc.co.jp/micom/index_E.htm

Flash Memory Programmers

NEC's flash memory programmer (PG-FP3) supports all NEC microcontrollers with dual-power-supply on-chip flash memory. The PG-FP3 stores the device-specific information required for rewriting in a parameter file and the rewriting environment for each microcontroller can be automatically set by downloading this file. After the parameter file is downloaded, the PG-FP3 can be used on a standalone basis. Combined with a program adapter (FA series (manufactured by Naito Densei Machida Mfg. Co., Ltd.)), this programmer can be used to write single microcontrollers. On-board writing is also possible using a target cable.
An example of the rewriting environment when using the program adapter is described below.

●Example of rewriting environment



① Flash memory programmer (PG-FP3)
② Target system
③ Power supply unit
④ Host machine interface (RS-232-C)
⑤ To host machine

Cautions 1. Install the control software of the PG-FP3 and the parameter file of the target device in the host machine.
• PG-FP3 control software: Provided with PG-FP3
• Parameter files: Distributed via online delivery
2. In addition to using the program adapter, rewriting can also be done on-board on the target system.

Functional Outline

(1/11)

Item		V850E/MA1					V850E/MA2
		μPD703103A	μPD703105A	μPD703106A	μPD703107A	μPD70F3107A	μPD703108
CPU core		V850E1					V850E1
CPU performance (Dhrystone)		—	62MIPS (@ 50 MHz)				—
Internal ROM		None	128 KB (Mask ROM)		256 KB (mask ROM)	256 KB (flash memory)	None
Internal RAM		4 KB		10 KB			4 KB
External bus interface	Address bus	26 bits					25 bits
	Data bus	16 bits					16 bits
	Programmable waits	0 to 7					0 to 7
Interrupt sources		External: 25 (17)[Note] Internal: 33					External: 8 (4)[Note] Internal: 23
DSP function	32×32→64	0.02 to 0.04μs (@ 50 MHz)					0.025 to 0.05μs (@ 40 MHz)
	32×32+32→32	0.06μs (@ 50 MHz)					0.075μs (@ 40 MHz)
	16×16→32	—					—
	16×16+32→32	—					—
Timer/counter (RPU)		16-bit timer/event counter × 4 ch 16-bit interval timer × 4 ch					16-bit timer/event counter × 2 ch 16-bit interval timer × 4 ch
Serial interface (SIO)	CSI	1 ch					—
	CSI/I²C	—					—
	CSI/UART	2 ch					2 ch
	UART	1 ch					—
	Dedicated BRG	3 ch					2 ch
A/D converter		8 ch (10-bit resolution)					4 ch (10-bit resolution)
DMA controller		4 ch					4 ch
Real-time output port		—					—
Ports	I/O	106					74
	Input	9					5
Other peripheral I/O functions		Memory access control function (SDRAM, SRAM, EDO DRAM, page ROM, etc., directly connectable) PWM: 2 ch (8/9/10/12-bit resolution)					Memory access control function (SDRAM, SRAM, page ROM, etc., directly connectable)
Power save function		HALT, IDLE, STOP					HALT, IDLE, STOP
Operating frequency		4 to 50 MHz					4 to 40 MHz
Power supply voltage		3.0 to 3.6 V					3.0 to 3.6 V
Power consumption (Typ.)		540mW (@ 3.3 V, 50 MHz)					376mW (@ 3.3 V, 40 MHz)
Package		144-pin plastic LQFP (20 × 20 mm)		144-pin plastic LQFP (20 × 20 mm) 161-pin plastic FGBA (13 × 13 mm)			100-pin plastic LQFP (14 × 14 mm)

Note Number of external interrupts that can be used to release STOP mode

Item		V850E/IA1		V850E/IA2	
		μPD703116	μPD70F3116	μPD703114	μPD70F3114
CPU core		V850E1		V850E1	
CPU performance (Dhrystone)		62MIPS (@ 50 MHz)		50MIPS (@ 40 MHz)	
Internal ROM		256 KB (mask ROM)	256 KB (flash memory)	128 KB (mask ROM)	128 KB (flash memory)
Internal RAM		10 KB		6 KB	
External bus interface	Address bus	24 bits		22 bits	
	Data bus	16 bits		16 bits	
	Programmable waits	0 to 7		0 to 7	
Interrupt sources		External: 20 (14)[Note] Internal: 46		External: 16 (12)[Note] External: 42	
DSP function	32×32→64	0.02 to 0.04μs (@ 50 MHz)		0.025 to 0.05μs (@ 40 MHz)	
	32×32+32→32	0.06μs (@ 50 MHz)		0.075μs (@ 40 MHz)	
	16×16→32	—		—	
	16×16+32→32	—		—	
Timer/counter (RPU)		16-bit 3-phase sine wave PWM timer × 2 ch 16-bit encoder counter/timer × 2 ch 16-bit timer/counter × 2 ch 16-bit timer/event counter × 1 ch 16-bit interval timer × 1 ch		16-bit 3-phase sine wave PWM timer × 2 ch 16-bit encoder counter/timer × 1 ch 16-bit timer/counter × 2 ch 16-bit timer/event counter × 1 ch 16-bit interval timer × 1 ch	
Serial interface (SIO)	CSI	2 ch		1 ch	
	CSI/I^2C	—		—	
	CSI/UART	—		1 ch	
	UART	3 ch		1 ch	
	Dedicated BRG	4 ch		3 ch	
A/D converter		8 ch (10-bit resolution), 2 units		6 ch (10-bit resolution): A/D converter 0, 8 ch (10-bit resolution): A/D converter 1	
DMA controller		4 ch		4 ch	
Real-time output port		—		—	
Ports	I/O	75		47	
	Input	8		6	
Other peripheral I/O functions		Memory access control function (SRAM, ROM connectable)		Memory access control function (SRAM, ROM connectable)	
Power save function		HALT, IDLE, STOP		HALT, IDLE, STOP	
Operating frequency		4 to 50 MHz		4 to 40 MHz	
Power supply voltage		Internal unit: 3.3 V, A/D converter: 5 V, external pin: 5 V		5 V (Internal unit: 3.3 V, A/D converter: 5 V, external pin: 5 V) (On-chip regulator)	
Power consumption (Typ.)		630 mW (For internal unit: 3.3 V, external pin: 5 V, 50 MHz)		440mW	
Package		144-pin plastic LQFP (20 × 20 mm)		100-pin plastic LQFP (14 × 14 mm)	

Note Number of external interrupts that can be used to release STOP mode

(3/11)

Item		V850E/MS1				
		μPD703100-40	μPD703100-33	μPD703101-33	μPD703102-33	μPD70F3102-33
CPU core		V850E				
CPU performance (Dhrystone)		—		43 MIPS (@ 33 MHz)		
Internal ROM		None		96 KB (mask ROM)	128 KB (mask ROM)	128 KB (flash memory)
Internal RAM		4 KB				
External bus interface	Address bus	24 bits				
	Data bus	16 bits				
	Programmable waits	0 to 7				
Interrupt sources		External: 25 (1)[Note] Internal: 47				
DSP function	32×32→64	0.025 to 0.05μs (@ 40 MHz)	0.03 to 0.06μs (@ 33 MHz)			
	32×32+32→32	0.075μs (@ 40 MHz)	0.09μs (@ 33 MHz)			
	16×16→32	—				
	16×16+32→32	—				
Timer/counter (RPU)		16-bit timer/event counter × 6 ch 16-bit interval timer × 2 ch				
Serial interface (SIO)	CSI	2 ch				
	CSI/I²C	—				
	CSI/UART	2 ch				
	UART	—				
	Dedicated BRG	3 ch				
A/D converter		8 ch (10-bit resolution)				
DMA controller		4 ch				
Real-time output port		—				
Ports	I/O	114				
	Input	9				
Other peripheral I/O functions		Memory access control function (EDO DRAM, SRAM, page ROM, etc., directly connectable)				
Power save function		HALT, IDLE, STOP				
Operating frequency		2 to 40 MHz	2 to 33 MHz			
Power supply voltage		Internal unit: 3.3 V, A/D converter: 5 V External pin: 5 V				
Power consumption (Typ.)		540mW (@ 40 MHz)	430mW (@ 33 MHz)			
Package		144-pin plastic LQFP (20 × 20 mm)				

Note Number of external interrupts that can be used to release STOP mode

(4/11)

Item		V850E/MS1					V850E/MS2
		μPD703100A-40	μPD703100A-33	μPD703101A-33	μPD703102A-33	μPD70F3102A-33	μPD703130
CPU core		V850E					V850E
CPU performance (Dhrystone)		—		43MIPS (@ 33 MHz)			—
Internal ROM		None		96 KB (mask ROM)	128 KB (mask ROM)	128 KB (flash memory)	None
Internal RAM		4 KB					4 KB
External bus interface	Address bus	24 bits					24 bits
	Data bus	16 bits					16 bits
	Programmable waits	0 to 7					0 to 7
Interrupt sources		External: 25 (1)[Note] Internal: 47					External: 10 (1)[Note] Internal: 35
DSP function	32×32→64	0.025 to 0.05μs (@ 40 MHz)	0.03 to 0.06μs (@ 33 MHz)				0.03 to 0.06μs (@ 33 MHz)
	32×32+32→32	0.075μs (@ 40 MHz)	0.09μs (@ 33 MHz)				0.09μs (@ 33 MHz)
	16×16→32	—					—
	16×16+32→32	—					—
Timer/counter (RPU)		16-bit timer/event counter × 6 ch 16-bit interval timer × 2 ch					16-bit timer/ event counter × 4 ch 16-bit interval timer × 2 ch
Serial interface (SIO)	CSI	2 ch					—
	CSI/I²C	—					—
	CSI/UART	2 ch					2 ch
	UART	—					—
	Dedicated BRG	3 ch					2 ch
A/D converter		8 ch (10-bit resolution)					4 ch (10-bit resolution)
DMA controller		4 ch					4 ch
Real-time output port		—					—
Ports	I/O	114					76
	Input	9					5
Other peripheral I/O functions		Memory access control function (EDO DRAM, SRAM, page ROM, etc., directly connectable)					Memory access control function (EDO DRAM, SRAM, page ROM, etc., directly connectable)
Power save function		HALT, IDLE, STOP					HALT, IDLE, STOP
Operating frequency		2 to 40MHz	2 to 33MHz				10 to 33MHz
Power supply voltage		Internal unit: 3.3 V, A/D converter: 3.3 V External pin: 3.3 V					Internal unit: 3.3 V, A/D converter: 5 V External pin: 5 V
Power consumption (Typ.)		330mW (@ 40 MHz)	270mW (@ 33 MHz)				381mW (@ 33 MHz)
Package		144-pin plastic LQFP (20 × 20 mm)	144-pin plastic LQFP (20 × 20 mm) 157-pin plastic FBGA (14 × 14 mm)				100-pin plastic LQFP (14 × 14 mm)

Note Number of external interrupts that can be used to release STOP mode

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Item		V850ES/SA2		V850ES/SA3	
		μPD703201/ μPD703201Y	μPD70F3201/ μPD70F3201Y	μPD703204/ μPD703204Y	μPD70F3204/ μPD70F3204Y
CPU core		V850ES			
CPU performance (Dhrystone)		21 MIPS (@ 17 MHz)/16 MIPS (@ 13.5 MHz)			
Internal ROM		256 KB (mask ROM)	256 KB (flash memory)	256 KB (mask ROM)	256 KB (flash memory)
Internal RAM		16 KB			
External bus interface	Address bus	22 bits		24 bits	
	Data bus	8/16 bits			
	Programmable waits	0 to 7			
Interrupt sources		External: 8 (8)[Note 1] Internal 30 (Y products: 31)		External: 8 (8)[Note 1] Internal: 31 (Y products: 32)	
DSP function	32×32→64	0.24 to 0.29μs (@ 17 MHz)			
	32×32+32→32	0.35μs (@ 17 MHz)			
	16×16→32	0.06 to 0.12μs (@ 17 MHz)			
	16×16+32→32	0.18μs (@ 17 MHz)			
Timer/counter (RPU)		16-bit timer/event counter × 2 ch 8-bit timer/event counter × 4 ch (usable as 16-bit timer/event counter × 2 ch)			
Serial interface (SIO)	CSI	2 ch		3 ch	
	CSI/I²C[Note 2]	1 ch		1 ch	
	CSI/UART	1 ch		1 ch	
	UART	1 ch		1 ch	
	Dedicated BRG	2 ch (UART-dedicated)		2 ch	
A/D converter		12 ch (10-bit resolution)		16 ch (10-bit resolution)	
DMA controller		4 ch			
Real-time output port		—			
Ports	I/O	68		84	
	Input	14		18	
Other peripheral I/O functions		Real-time counter (for watch): 1 ch Watchdog timer: 1 ch			
Power save function		HALT, IDLE, STOP			
Operating frequency		When using main clock: 2 to 17 MHz (@ 2.4 V)/2 to 13.5 MHz (@ 2.3 V) When using subclock: 32.768 kHz (only real-time counter operating)			
Power supply voltage		2.3 to 2.7 V (@ 17 MHz)/2.2 to 2.7 V (@ 13.5 MHz)			
Power consumption (Typ.)		When using main clock: 30 mW* (@ 2.5 V, 17 MHz)			
Package		100-pin plastic LQFP (14 × 14 mm)		121-pin plastic FBGA (12 × 12 mm)	

Notes1. Number of external interrupts that can be used to release STOP mode

2. Only Y products have an on-chip I²C bus interface.
CSI/I²C : μPD703201Y, 703204Y, 70F3201Y, 70F3204Y
CSI : μPD703201, 703204, 70F3201, 70F3204

Remark Values with * are target values.

(6/11)

Item		V850/SA1						
		μPD703014A/ μPD703014AY	μPD703014B/ μPD703014BY	μPD703015A/ μPD703015AY	μPD703015B/ μPD703015BY	μPD70F3015B/ μPD70F3015BY	μPD703017A/ μPD703017AY	μPD70F3017A/ μPD70F3017AY
CPU core		V850						
CPU performance (Dhrystone)		23MIPS (@ 20 MHz)/19MIPS (@ 17 MHz)						
Internal ROM		64 KB (mask ROM)		128 KB (mask ROM)		128 KB (flash memory)	256 KB (mask ROM)	256 KB (flash memory)
Internal RAM		4 KB					8 KB	
External bus interface	Address bus	22 bits						
	Data bus	16 bits						
	Programmable waits	0 to 3						
Interrupt sources		External: 9 (6)[Note 1] Internal: 22						
DSP function	32×32→64	—						
	32×32+32→32	—						
	16×16→32	0.05 to 0.10μs (@ 20 MHz)						
	16×16+32→32	0.15μs (@ 20 MHz)						
Timer/counter (RPU)		16-bit timer/event counter × 2 ch 8-bit timer/event counter × 4 ch (usable as 16-bit timer/event counter × 2 ch)						
Serial interface (SIO)	CSI	1 ch						
	CSI/I^2C[Note 2]	1 ch						
	CSI/UART	1 ch						
	UART	1 ch						
	Dedicated BRG	2 ch (UART-dedicated)						
A/D converter		12 ch (10-bit resolution)						
DMA controller		3 ch (only for internal RAM⟷on-chip peripheral I/O)						
Real-time output port		8-bit × 1 ch or 4-bit × 2 ch						
Ports	I/O	72						
	Input	13						
Other peripheral I/O functions		Watch timer: 1 ch Watchdog timer: 1 ch						
Power save function		HALT, IDLE, STOP						
Operating frequency		Using main clock: 2 to 20 MHz (@ 3.3 V)/2 to 17 MHz (@ 3 V) Using subclock: 32.768 kHz						
Power supply voltage		3.0 to 3.6 V (@ 20 MHz)/2.7 to 3.6 V (@ 17 MHz)						
Power consumption (Typ.)		Using main clock: 66 mW (@ 3.3 V, 20 MHz)/56 mW (@ 3.3 V, 17 MHz)				Using main clock: 105 mW(@ 3.3 V, 20 MHz)/ 99 mW (@ 3.3 V, 17 MHz)	Using main clock: 66 mW (@ 3.3 V, 20 MHz)/ 56 mW (@ 3.3 V, 17 MHz)	Using main clock: 105 mW (@ 3.3 V, 20 MHz)/ 99 mW (@ 3.3 V, 17 MHz)
Package		100-pin plastic LQFP (14 × 14 mm)[Note 3] 121-pin plastic FBGA (12 × 12 mm)[Note 4]						

Notes1. Number of external interrupts that can be used to release STOP mode

2. Only Y products have an on-chip I^2C bus interface.
CSI/I^2C : μPD703014AY, 703014BY, 703015AY, 703015BY, 703017AY, 70F3015BY, 70F3017AY
CSI : μPD703014A, 703014B, 703015A, 703015B, 703017A, 70F3015B, 70F3017A

3. μPD703014B, 703014BY, 703015B, 703015BY, 703017A, 703017AY, 70F3015B, 70F3015BY, 70F3017A, 70F3017AY

4. μPD703014A, 703014AY, 703015A, 703015AY, 703017A, 703017AY, 70F3017A, 70F3017AY

Caution The maximum operating frequency of the I^2C bus interface is 17 MHz.

Item		V850/SV1					
		μPD703041/ μPD703041Y	μPD703039/ μPD703039Y	μPD703040/ μPD703040Y	μPD70F3040/ μPD70F3040Y	μPD703038/ μPD703038Y	μPD70F3038/ μPD70F3038Y
CPU core		V850					
CPU performance (Dhrystone)		23 MIPS (@ 20 MHz)/18 MIPS (@ 16 MHz)					
Internal ROM		192 KB (mask ROM)	256 KB (mask ROM)		256 KB (flash memory)	384 KB (mask ROM)	384 KB (flash memory)
Internal RAM		8 KB		16 KB			
External bus interface	Address bus	22 bits					
	Data bus	16 bits					
	Programmable waits	0 to 3					
Interrupt sources		External: 9 (6)[Note 1] Internal: 43 (Y products: 44)					
DSP function	32×32 →64	—					
	32×32+32→32	—					
	16×16 →32	0.05 to 0.10μs (@ 20 MHz)					
	16×16+32→32	0.15μs (@ 20 MHz)					
Timer/counter (RPU)		24-bit timer/event counter × 2 ch 16-bit timer/event counter × 2 ch 8-bit timer/event counter × 8 ch (usable as 16-bit timer/event counter × 4 ch)					
Serial interface (SIO)	CSI	1 ch					
	CSI/I^2C[Note 2]	2 ch					
	CSI/UART	2 ch					
	UART	—					
	Dedicated BRG	3 ch					
A/D converter		16 ch (10-bit resolution)					
DMA controller		6 ch (only for internal RAM⟷on-chip peripheral I/O)					
Real-time output port		8-bit × 2 ch or 4-bit × 4 ch					
Ports	I/O	135					
	Input	16					
Other peripheral I/O functions		Vsync/Hsync separator					
		Watch timer: 1 ch Watchdog timer: 1 ch PWM: 4 ch (12 to 16-bit resolution)					
Power save function		HALT, IDLE, STOP					
Operating frequency		4 to 20 MHz (@ 3.3 V)/4 to 16 MHz (@ 3 V)					
Power supply voltage		3.1 to 3.6 V (@ 20 MHz)/2.7 to 3.6 V (@ 16 MHz)					
Power consumption (Typ.)		82 mW (@ 3.3 V, 20 MHz)/72 mW (@ 3.3 V, 16 MHz)			148 mW (@ 3.3 V, 20 MHz)/ 132 mW (@ 3.3 V, 16 MHz)	82 mW (@ 3.3 V, 20 MHz) 72 mW (@ 3.3 V. 16 MHz)	148 mW (@ 3.3 V, 20 MHz) 132 mW (@ 3.3 V, 16 MHz)
Package		176-pin plastic LQFP (24 × 24 mm)	176-pin plastic LQFP (24 × 24 mm) 180-pin plastic FBGA (13 × 13 mm)			180-pin plastic FBGA (13 × 13 mm)	

Notes1. Number of external interrupts that can be used to release STOP mode

2. Only Y products have an on-chip I^2C bus interface.

CSI/I^2C : μPD703038Y, 703039Y, 703040Y, 703041Y, 70F3038Y, 70F3040Y

CSI : μPD703038, 703039, 703040, 703041, 70F3038, 70F3040

Caution The maximum operating frequency of the I^2C bus interface is 17 MHz.

Item		V850/SC1	V850/SC2	V850/SC3		V850/SC1, V850/SC2, V850/SC3
		μPD703068Y	μPD703069Y	μPD703088Y	μPD703089Y	μPD70F3089Y
CPU core		V850	V850	V850		V850
CPU performance (Dhrystone)		23MIPS (@ 20 MHz)	21MIPS (@ 19 MHz)	18MIPS (@ 16 MHz)		23MIPS (@ 20 MHz)
Internal ROM		512 KB (mask ROM)	512 KB (mask ROM)	512 KB (mask ROM)		512 KB (flash memory)
Internal RAM		24 KB	24 KB	24 KB		24 KB
External bus interface	Address bus	22 bits	22 bits	22 bits		22 bits
	Data bus	16 bits	16 bits	16 bits		16 bits
	Programmable waits	0 to 3	0 to 3	0 to 3		0 to 3
Interrupt sources		External: 12 (9)[Note] Internal: 39	External: 12 (9)[Note] Internal: 41	External: 12 (9)[Note] Internal: 43	External: 12 (9)[Note] Internal: 46	External: 12 (9)[Note] Internal: 46
DSP function	32×32→64	—	—	—		—
	32×32+32→32	—	—	—		—
	16×16→32	0.05 to 0.10μs (@ 20 MHz)	0.053 to 0.106μs (@ 19 MHz)	0.06 to 0.12μs (@ 16 MHz)		0.05 to 0.10μs (@ 20 MHz)
	16×16+32→32	0.15μs (@ 20 MHz)	0.159μs (@ 19 MHz)	0.18μs (@ 16 MHz)		0.15μs (@ 20 MHz)
Timer/counter (RPU)		16-bit timer/ event counter × 10 ch	16-bit timer/ event counter × 10 ch	16-bit timer/event counter × 10 ch		16-bit timer/ event counter × 10 ch
Serial interface (SIO)	CSI	2 ch	2 ch	2 ch		2 ch
	CSI/I^2C	2 ch	2 ch	2 ch		2 ch
	CSI/UART	2 ch	2 ch	2 ch		2 ch
	UART	2 ch	2 ch	2 ch		2 ch
	Dedicated BRG	5 ch	5 ch	5 ch		5 ch
A/D converter		12 ch (10-bit resolution)	12 ch (10-bit resolution)	12 ch (10-bit resolution)		12 ch (10-bit resolution)
DMA controller		6 ch (only for internal RAM ⟷ on-chip peripheral I/O)	6 ch (only for internal RAM ⟷ on-chip peripheral I/O)	6 ch (only for internal RAM⟷on-chip peripheral I/O)		6 ch (only for internal RAM ⟷ on-chip peripheral I/O)
Real-time output port		—	—	—		—
Ports	I/O	112	112	112		112
	Input	12	12	12		12
Other peripheral I/O functions		—	IEBus (simple version): 1 ch	FCAN : 1 ch	FCAN : 2 ch	IEBus (simple version): 1 ch/FCAN: 2 ch
		Watch timer: 1 ch Watchdog timer: 1 ch	Watch timer: 1 ch Watchdog timer: 1 ch	Watch timer: 1 ch Watchdog timer: 1 ch		Watch timer: 1 ch Watchdog timer: 1 ch
Power save function		HALT, IDLE, STOP	HALT, IDLE, STOP	HALT, IDLE, STOP		HALT, IDLE, STOP
Operating frequency		Using main clock: 4 to 20 MHz (@ 5 V) Using subclock: 32.768 kHz	Using main clock: 4 to 19 MHz (@ 5 V) Using subclock: 32.768 kHz	Using main clock: 4 to 16 MHz (@ 5 V) Using subclock: 32.768 kHz		Using main clock: 4 to 20 MHz (@ 5 V) Using subclock: 32.768 kHz
Power supply voltage		3.5 to 5.5 V (A/D converter: 4.5 to 5.5 V)	3.5 to 5.5 V (A/D converter: 4.5 to 5.5 V)	3.5 to 5.5 V (A/D converter: 4.5 to 5.5 V)		4.0 to 5.5 V (A/D converter: 4.5 to 5.5 V)
Power consumption (Typ.)		Using main clock: 125 mW* (@ 5 V, 20 MHz)	Using main clock: 120 mW* (@ 5 V, 19 MHz)	Using main clock: 110 mW* (@ 5 V, 16 MHz)		Using main clock: 150 mW* (@ 5 V, 20 MHz)
Package		144-pin plastic LQFP (20 × 20 mm)	144-pin plastic LQFP (20 × 20 mm)	144-pin plastic LQFP (20 × 20 mm)		144-pin plastic LQFP (20 × 20 mm)

Note Number of external interrupts that can be used to release STOP mode
Remark Values with * are target values.

Item		V850/SF1			V850/SB1					
		μPD703078Y	μPD703079Y	μPD70F3079Y	μPD703031A/ μPD703031AY	μPD703033A/ μPD703033AY	μPD70F3033A/ μPD70F3033AY	μPD703030A/ μPD703030AY	μPD703032A/ μPD703032AY	μPD70F3032A/ μPD70F3032AY
CPU core		V850			V850					
CPU performance (Dhrystone)		18MIPS (@ 16 MHz)			23MIPS (@ 20 MHz)					
Internal ROM		256 KB (mask ROM)		256 KB (flash memory)	128 KB (mask ROM)	256 KB (mask ROM)	256 KB (flash memory)	384 KB (mask ROM)	512 KB (mask ROM)	512 KB (flash memory)
Internal RAM		16 KB			12 KB	16 KB		20 KB	24 KB	
External bus interface	Address bus	22 bits			22 bits					
	Data bus	16 bits			16 bits					
	Programmable waits	0 to 3			0 to 3					
Interrupt sources		External: 9 (6)[Note 1] Internal: 32		External: 9 (6)[Note 1] Internal: 35	External: 9 (6)[Note 1] Internal: 30 (Y products: 31)					
DSP function	32×32→64	—			—					
	32×32+32→32	—			—					
	16×16→32	0.06 to 0.12μs (@ 16 MHz)			0.05 to 0.10μs (@ 20 MHz)					
	16×16+32→32	0.18μs (@ 16 MHz)			0.15μs (@ 20 MHz)					
Timer/counter (RPU)		16-bit timer/event counter × 8 ch			16-bit timer/event counter × 2 ch 8-bit timer/event counter × 4 ch (usable as 16-bit timer/event counter × 2 ch) 8-bit timer × 2 ch (usable as 16-bit timer × 1 ch)					
Serial interface (SIO)	CSI	1 ch			1 ch					
	CSI/I²C[Note 2]	1 ch			2 ch					
	CSI/UART	2 ch			2 ch					
	UART	—			—					
	Dedicated BRG	3 ch			3 ch					
A/D converter		12 ch (10-bit resolution)			12 ch (10-bit resolution)					
DMA controller		6 ch (only for internal RAM←→on-chip peripheral I/O)			6 ch (only for internal RAM←→on-chip peripheral I/O)					
Real-time output port		—			8 bits × 1 or 4 bits × 2					
Ports	I/O	72			71					
	Input	12			12					
Other peripheral I/O functions		FCAN : 1 ch	FCAN : 2 ch		—					
		Watch timer : 1 ch Watchdog timer : 1 ch			Watch timer: 1 ch Watchdog timer: 1 ch					
Power save function		HALT, IDLE, STOP			HALT, IDLE, STOP					
Operating frequency		Using main clock: 4 to 16 MHz (@ 5 V) Using subclock: 32.768 kHz			Using main clock: 2 to 20 MHz (@ 5 V) Using subclock: 32.768 kHz					
Power supply voltage		4.0 to 5.5 V (A/D converter: 4.5 to 5.5 V) (@ 16 MHz)			4.0 to 5.5 V (A/D converter: 4.5 to 5.5 V)					
Power consumption (Typ.)		Using main clock: 75 mW (mask ROM)/ 125 mW (flash memory)(@ 5 V, 16 MHz)			Using main clock: 125 mW (@ 5 V, 20 MHz)	Using main clock: 165 mW (@ 5 V, 20 MHz)		Using main clock: 125 mW (@ 5 V, 20 MHz)	Using main clock: 165 mW (@ 5 V, 20 MHz)	
Package		100-pin plastic LQFP (14 × 14 mm) 100-pin plastic QFP (14 × 20 mm)			100-pin plastic LQFP (14 × 14 mm) 100-pin plastic QFP (14 × 20 mm)			100-pin plastic QFP (14 × 20 mm)		

Notes1. Number of external interrupts that can be used to release STOP mode

2. Only Y products have an on-chip I²C bus interface.
CSI/I²C : μPD703030AY, 703031AY, 703032AY, 703033AY, 703078Y, 703079Y, 70F3032AY, 70F3033AY, 70F3079Y
CSI : μPD703030A, 703031A, 703032A, 703033A, 70F3032A, 70F3033A

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Item		V850/SB2					
		μPD703034A/ μPD703034AY	μPD703035A/ μPD703035AY	μPD70F3035A/ μPD70F3035AY	μPD703036A/ μPD703036AY	μPD703037A/ μPD703037AY	μPD70F3037A/ μPD70F3037AY
CPU core		V850					
CPU performance (Dhrystone)		15MIPS (@ 13 MHz)					
Internal ROM		128 KB (mask ROM)	256 KB (mask ROM)	256 KB (flash memory)	384 KB (mask ROM)	512 KB (mask ROM)	512 KB (flash memory)
Internal RAM		12 KB	16 KB		20 KB	24 KB	
External bus interface	Address bus	22 bits					
	Data bus	16 bits					
	Programmable waits	0 to 3					
Interrupt sources		External: 9 (6)Note 1 Internal: 32 (Y products: 33)					
DSP function	32×32→64	—					
	32×32+32→32	—					
	16×16→32	0.077 to 0.154μs (@ 13 MHz)					
	16×16+32→32	0.231μs (@ 13 MHz)					
Timer/counter (RPU)		16-bit timer/event counter × 2 ch 8-bit timer/event counter × 4 ch (usable as 16-bit timer/event counter × 2 ch) 8-bit timer × 2 ch (usable as 16-bit timer × 1 ch)					
Serial interface (SIO)	CSI	1 ch					
	CSI/I²CNote 2	2 ch					
	CSI/UART	2 ch					
	UART	—					
	Dedicated BRG	3 ch					
A/D converter		12 ch (10-bit resolution)					
DMA controller		6 ch (only for internal RAM←→on-chip peripheral I/O)					
Real-time output port		8 bits × 1 or 4 bits × 2					
Ports	I/O	71					
	Input	12					
Other peripheral I/O functions		IEBus (simple version)					
		Watch timer: 1 ch Watchdog timer: 1 ch					
Power save function		HALT, IDLE, STOP					
Operating frequency		Using main clock: 2 to 13 MHz (@ 5 V) Using subclock: 32.768 kHz					
Power supply voltage		4.0 to 5.5 V (A/D converter: 4.5 to 5.5 V)					
Power consumption (Typ.)		Using main clock: 75 mW (@ 5 V, 13 MHz)		Using main clock: 125 mW (@ 5 V, 13 MHz)	Using main clock: 75 mW (@ 5 V, 13 MHz)		Using main clock: 125 mW (@ 5 V, 13 MHz)
Package		100-pin plastic LQFP (14 × 14 mm) 100-pin plastic QFP (14 × 20 mm)			100-pin plastic QFP (14 × 20 mm)		

Notes1. Number of external interrupts that can be used to release STOP mode

2. Only Y products have an on-chip I²C bus interface.

CSI/I²C : μPD703034AY, 703035AY, 703036AY, 703037AY, 70F3035AY, 70F3037AY

CSI : μPD703034A, 703035A, 703036A, 703037A, 70F3035A, 70F3037A

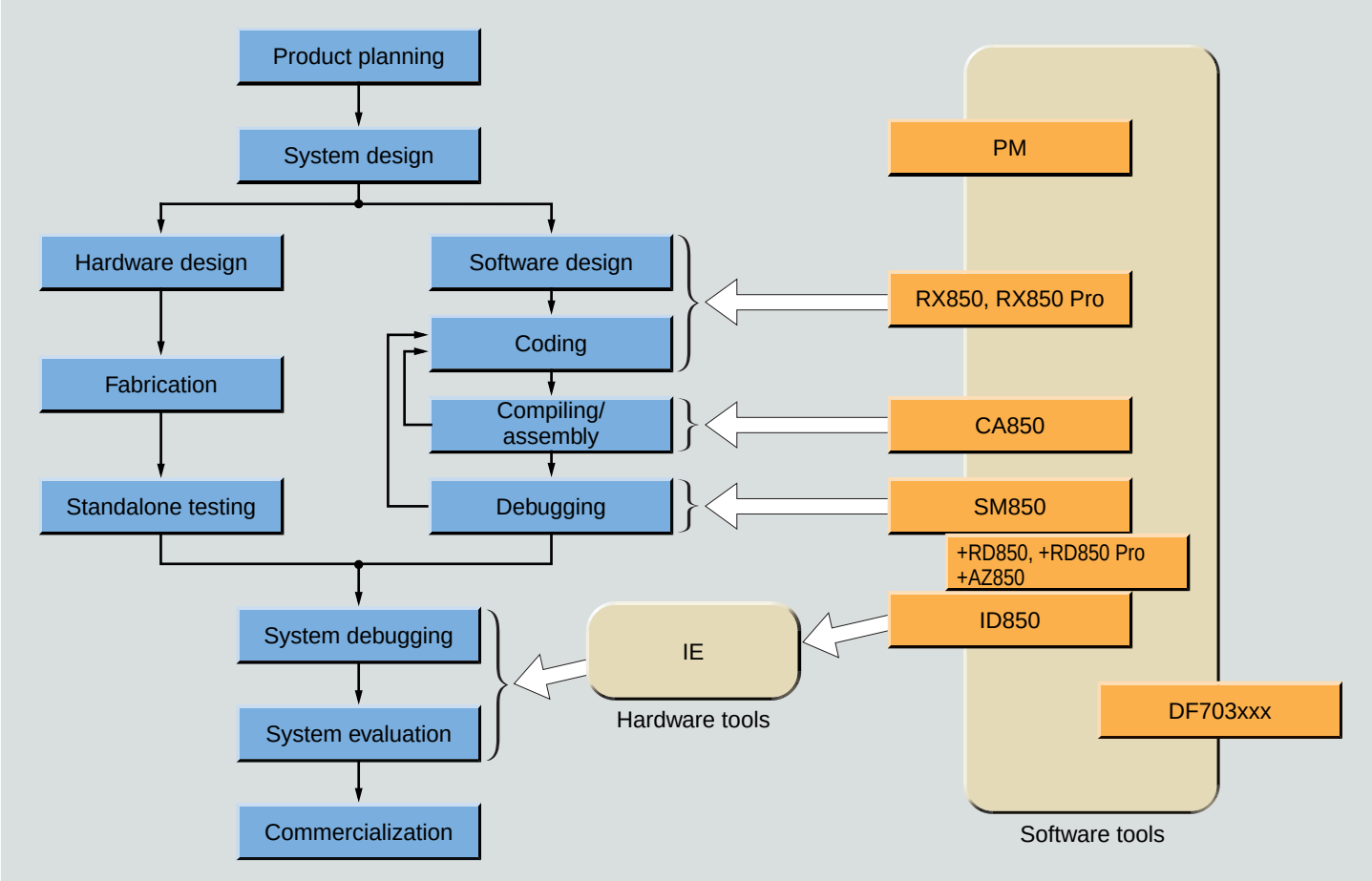
(11/11)

Item		V853				
		μPD703003A	μPD703004A	μPD703025A	μPD70F3003A	μPD70F3025A
CPU core		V850				
CPU performance (Dhrystone)		38MIPS (@ 33 MHz)				
Internal ROM		128 KB (mask ROM)	96 KB (mask ROM)	256 KB (mask ROM)	128 KB (flash memory)	256 KB (flash memory)
Internal RAM		4 KB		8 KB	4 KB	8 KB
External bus interface	Address bus	20 bits				
	Data bus	16 bits				
	Programmable waits	0 to 3				
Interrupt sources		External: 17 (1)[Note] Internal: 32				
DSP function	32×32→64	—				
	32×32+32→32	—				
	16×16→32	0.03 to 0.06μs (@ 33 MHz)				
	16×16+32→32	0.09μs (@ 33 MHz)				
Timer/counter (RPU)		16-bit timer/event counter × 4 ch 16-bit timer × 1 ch				
Serial interface (SIO)	CSI	2 ch				
	CSI/I^2C	—				
	CSI/UART	2 ch				
	UART	—				
	Dedicated BRG	3 ch				
A/D converter		8 ch (10-bit resolution)				
DMA controller		—				
Real-time output port		—				
Ports	I/O	67				
	Input	8				
Other peripheral I/O functions		PWM: 2 ch (8/9/10/12-bit resolution) D/A converter: 2 ch				
Power save function		HALT, IDLE, STOP				
Operating frequency		5 to 33 MHz (@ 5 V)				
Power supply voltage		4.5 to 5.5V				
Power consumption (Typ.)		365 mW (@ 5 V, 33 MHz)		450 mW (@ 5V, 33 MHz)	425 mW (@ 5 V, 33 MHz)	480 mW (@ 5 V, 33 MHz)
Package		100-pin plastic LQFP (14 × 14 mm)				

Note Number of external interrupts that can be used to release STOP mode

Comfortable Development Environment

Development Flow



Development Tools (1/3)

■Software tools

Product Name	
Software package	SP850
C compiler	CA850[Note 1]
Device file	DF703xxx[Note 1]
Project Manager	PM[Notes 1, 2]
Integrated debugger	ID850[Note 1]
System simulator	SM850[Note 1]
Real-time OS	RX850, RX850 Pro
Task debugger	RD850, RD850 Pro[Note 3]
System performance analyzer	AZ850[Note 1]
Middleware	AP703000-Bxxx, AP703100-Bxxx

Notes 1. Packaged in SP850
2. Included with CA850
3. Included with RX850, RX850 Pro

Remark For details, refer to the **V800 Series™ Development Environment Pamphlet (U10782E)**.

Development Tools (2/3)

■Hardware tools

Target Device		In-Circuit Emulator	
Device Name	Package	Main Unit	Emulation Board
V850E/MA1	144-pin plastic LQFP (20 × 20 mm)	IE-V850E-MC-A	IE-703107-MC-EM1
	161-pin plastic FBGA (13 × 13 mm)		IE-703107-MC-EM1 + CSSOCKET161A1413N01S1 (under development)[Note 1] LSPACK161A1413N01 (under development)[Note 1] CSICE161A1413N02 (under development)[Note 1]
V850E/MA2	100-pin plastic LQFP (14 × 14 mm)		IE-703107-MC-EM1 + VP-V850E/MA1-MA2 (under development)[Note 2]
V850E/IA1	144-pin plastic LQFP (20 × 20 mm)	IE-V850E-MC	IE-703116-MC-EM1
V850E/IA2	100-pin plastic LQFP (14 × 14 mm)		IE-703114-MC-EM1
V850E/MS1 (5V)	144-pin plastic LQFP (20 × 20 mm)	IE-703102-MC	IE-703102-MC-EM1
V850E/MS1 (3.3V)	144-pin plastic LQFP (20 × 20 mm)		IE-703102-MC-EM1-A
	157-pin plastic FBGA (14 × 14 mm)		IE-703102-MC-EM1-A + CSPACK157A1614N01[Note 1] CSICE157A1614N01[Note 1]
V850E/MS2 (5V)	100-pin plastic LQFP (14 × 14 mm)		IE-703102-MC-EM1 + VP-V850E/MS1-MS2[Note 2]
V850/SA1	100-pin plastic LQFP (14 × 14 mm)	IE-703002-MC	IE-703017-MC-EM1
	121-pin plastic FBGA (12 × 12 mm)		IE-703017-MC-EM1 + CSPACK121A1312N02[Note 1] CSICE121A1312N02[Note 1]
V850/SB1, V850/SB2	100-pin plastic LQFP (14 × 14 mm)		IE-703037-MC-EM1
	100-pin plastic QFP (14 × 20 mm)		IE-703037-MC-EM1 + NEXB-100SD/RB[Note 1]
V850/SV1	176-pin plastic LQFP (24 × 24 mm)		IE-703040-MC-EM1
	180-pin plastic FBGA (13 × 13 mm)		IE-703040-MC-EM1 + CSSOCKET180A1513N01N[Note 1] CSSOCKET180A1513N01S01[Note 1] EXC-180A/SV1[Note 1]
V850/SF1	100-pin plastic LQFP (14 × 14 mm)		IE-703079-MC-EM1
	100-pin plastic QFP (14 × 20 mm)		IE-703079-MC-EM1 + SWEX100SD/GF-N17D[Note 1] NQPACK100RB[Note 1] YQPACK100RB[Note 1] HQPACK100RB[Note 1] YQSOCKET100RBN[Note 1] YQGUIDE[Note 1]
V850/SC1, V850/SC2, V850/SC3	144-pin plastic LQFP (20 × 20 mm)		IE-703089-MC-EM1
V853	100-pin plastic LQFP (14 × 14 mm)		IE-703003-MC-EM1

Notes 1. Tokyo Eletech Corp.

2. Naito Densei Machida Mfg. Co., Ltd.

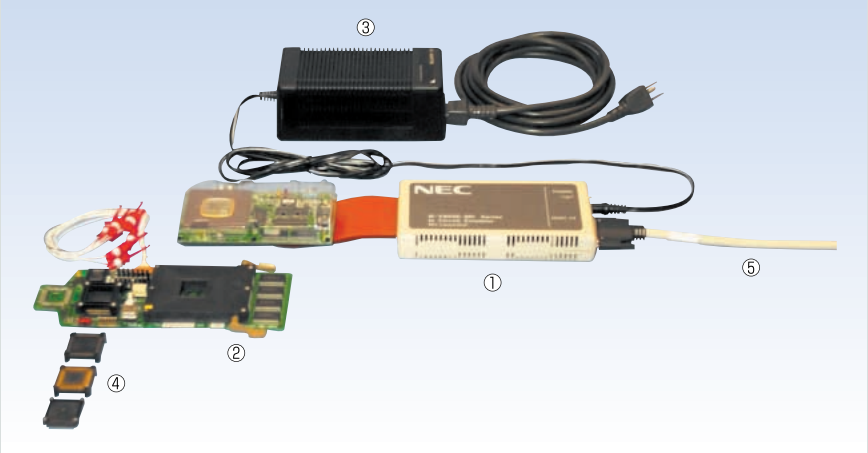
Remarks 1. The following parts are required as common products.

- PC interface board : IE-70000-PCI-IF-A or IE-70000-CD-IF-A
- Power supply : IE-70000-MC-PS-B

2. For details, refer to the **V800 Series™ Development Environment Pamphlet (U10782E)**.

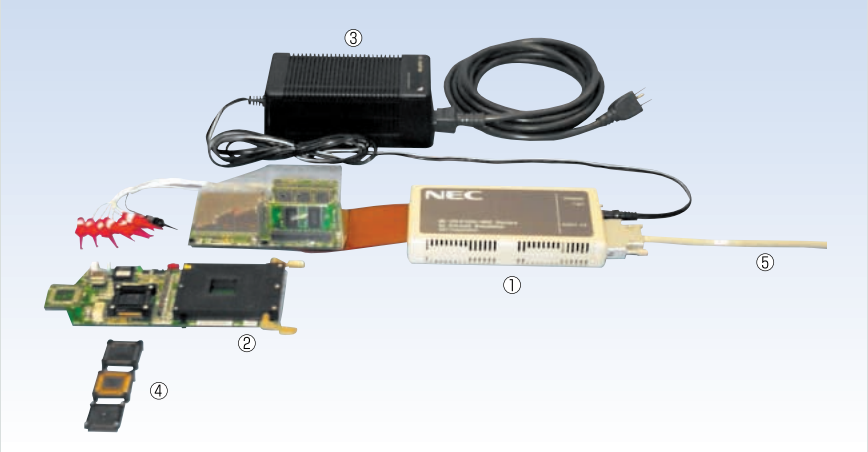
Development Tools (3/3)

● V850E/MA1, V850E/MA2, V850E/IA1, V850E/IA2 hardware tool configuration example



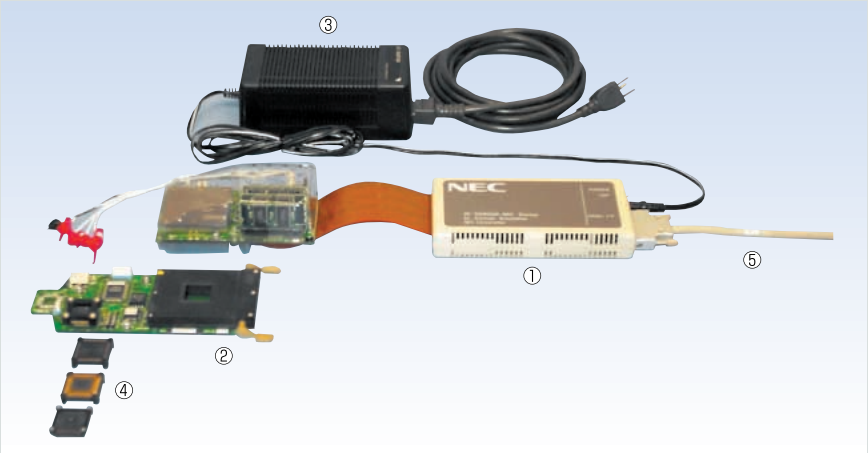
① In-circuit emulator (main unit)
② Emulation board
③ Power supply unit
④ Conversion adapter/conversion socket
⑤ To common interface block

● V850E/MS1, V850E/MS2 hardware tool configuration example



① In-circuit emulator (main unit)
② Emulation board
③ Power supply unit
④ Conversion adapter/conversion socket
⑤ To common interface block

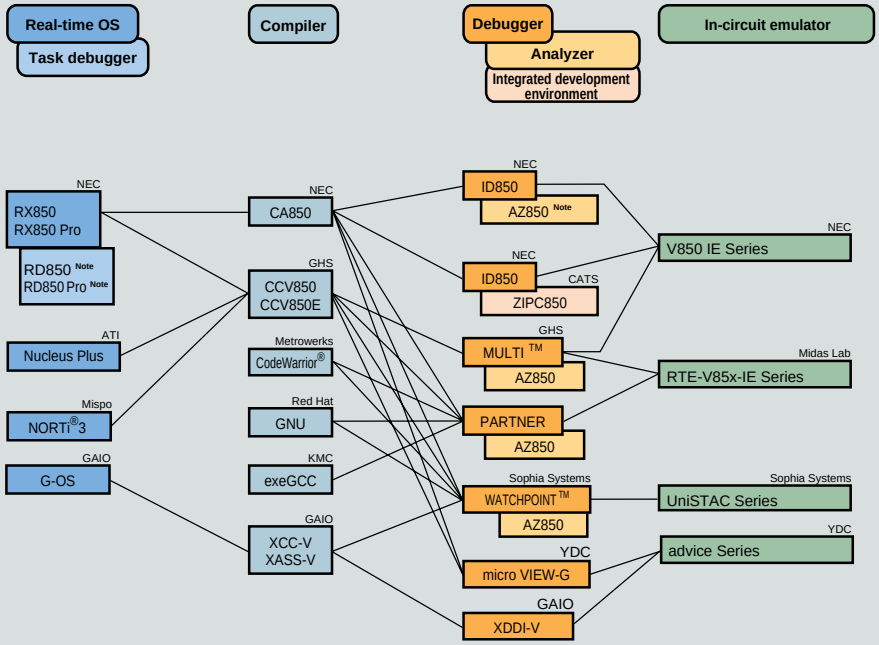
● V850/SA1, V850/SB1, V850/SB2, V850/SV1, V850/SF1, V850/SC1 ,V850/SC2, V850/SC3, V853 hardware tool configuration example



① In-circuit emulator (main unit)
② Emulation board
③ Power supply unit
④ Conversion adapter/conversion socket
⑤ To common interface block

Development Environment (1/2)

■ Development environment using in-circuit emulator

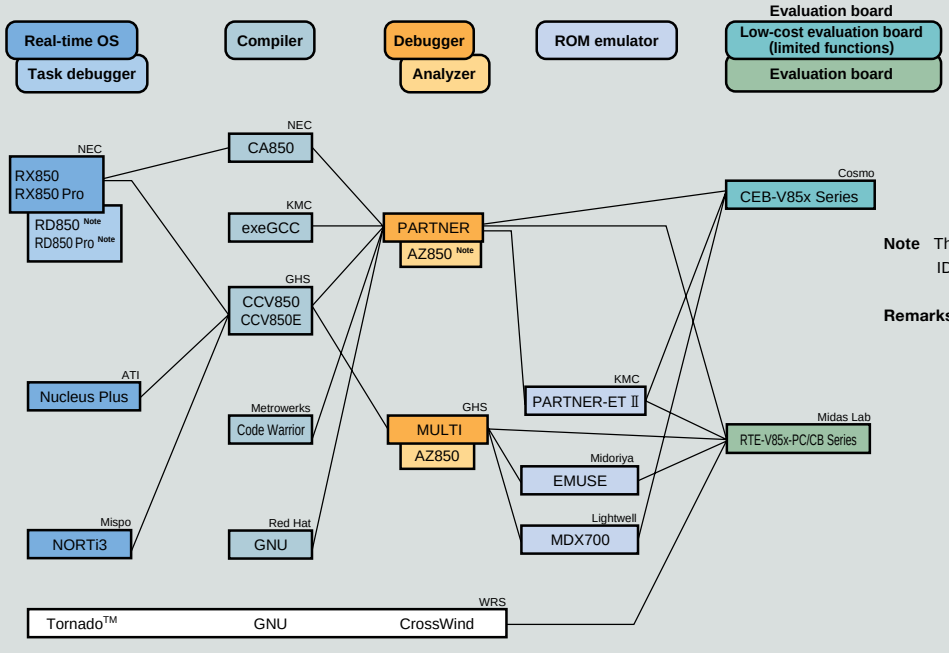


Note The RD850, RD850 Pro, and AZ850 can be used with ID850, MULTI, PARTNER, and WATCHPOINT.

Remarks 1. ATI : Accelerated Technology, Inc.
CATS : Communication And Technology Systems, Inc.
GAIO : Gaio Technology Co., Ltd.
GHS : Green Hills Software™, Inc.
KMC : Kyoto Microcomputer Corporation
Metrowerks : Metrowerks Corporation
Midas Lab : Midas Lab Co., Ltd.
Mispo : MiSPO, Inc.
Red Hat : Red Hat Corporation
Sophia Systems : Sophia Systems Co., Ltd.
YDC : Yokogawa Digital Computer Corporation

2. For details, refer to the **V800 Series Development Environment Pamphlet (U10782E).**

■ Development environment using ROM emulator and evaluation board



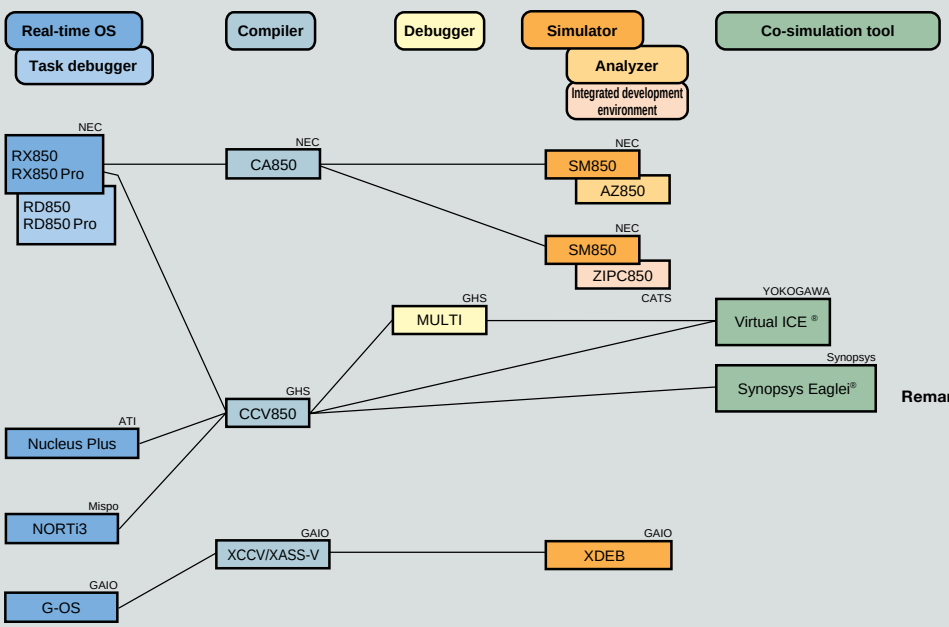
Note The RD850, RD850 Pro, and AZ850 can be used with ID850, MULTI, and PARTNER.

Remarks 1. ATI : Accelerated Technology, Inc.
Cosmo : Cosmo Co., Ltd.
GAIO : Gaio Technology Co., Ltd.
GHS : Green Hills Software™, Inc.
KMC : Kyoto Microcomputer Corporation
Lightwell : Lightwell Co., Ltd.
Metrowerks : Metrowerks Corporation
Midas Lab : Midas Lab Co., Ltd.
Midoriya : Midoriya Electric Co., Ltd.
Mispo : MiSPO, Inc.
Red Hat : Red Hat Corporation
WRS : Wind River Systems, Inc.

2. For details, refer to the **V800 Series Development Environment Pamphlet (U10782E).**

Development Environment (2/2)

■ Development environment using simulator



Remarks 1. ATI : Accelerated Technology, Inc.
CATS : Communication And Technology Systems, Inc.
GAIO : Gaio Technology Co., Ltd.
GHS : Green Hills Software, Inc.
Mispo : MiSPO, Inc.
YOKOGAWA : Yokogawa Electric Corporation
Synopsys : Nihon Synopsys, Inc.

2. For details, refer to the **V800 Series Development Environment Pamphlet (U10782E).**

Software Package (SP850)

■ Product configuration

The SP850 software package consists of the following software development tools.

- •C compiler (CA850)
- •Project Manager (PM)
- •Integrated debugger (ID850)
- •System simulator (SM850)
- •System performance analyzer (AZ850)
- •Device file (DF703xxx)

C Compiler (CA850)

■ Features

- •Complies with ANSI-C, a C language standard.
- •Supports libraries for embedded systems
- •Compact code size and faster execution speed can be realized through powerful optimization
- •Utilities useful for embedded systems (ROMization processor, etc.)
- •Description of embedded systems in C language (specification of memory allocation and I/O register access) is possible.

System Simulator (SM850)

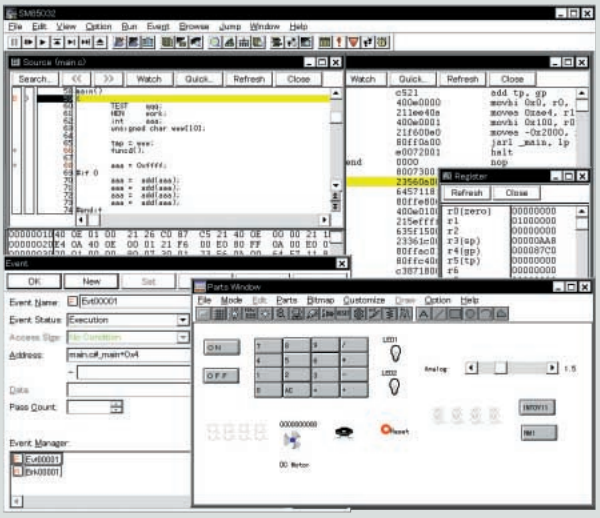
■ Features

- •Same operability as debugger
- •Target-less evaluation prior to target completion possible
- •In addition to the operation of the CPU itself, target system operation including on-chip peripheral unit and interrupt servicing can also be simulated.
- •Pseudo-target system construction and I/O operation are possible through external parts.
- •Data generated by 0/1 logic and timing charts can be input to the program being simulated.
- •Larger number of events than in-circuit emulator
- •Execution speed estimates can be done on the host machine to accurately simulate pipeline operation[Note].
- •Construction by user target system users is possible through user open interface.
- •A peripheral I/O register status can be specified and when this status occurs, the system can be made to output an interrupt at the desired timing or transfer data to memory (peripheral I/O register event & action function).

Note The pipeline mode is supported by the V853.

■ Target devices

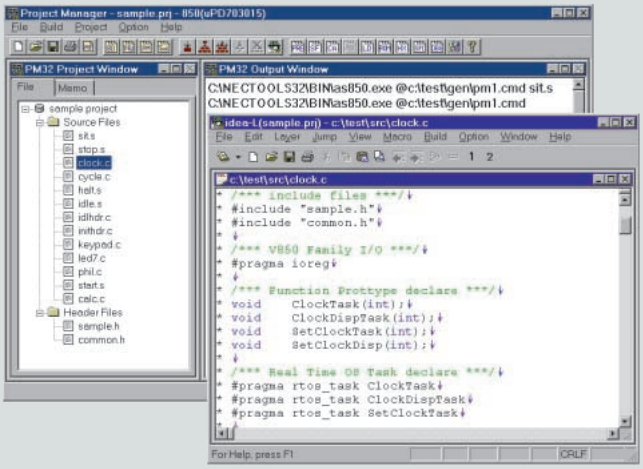
V853, V850/SA1, V850/SB1, V850/SB2, V850/SF1, V850E/MS1, V850E/MA1, V850E/IA1



Project Manager (PM)

■ Features

- •Project management (management of target chip, source, and environment during debugging is possible.)
- •Automation of series of operations consisting of edit, build, and debug
- •Integration of Help function
- •Included with C compiler package



Integrated Debugger (ID850)

■ Features

- Supports object files
- Debugging at source level
- Debugging using target resources
- Real-time execution on target
- Event setting according to complex software operation
- Online help function

In-Circuit Emulator

■ Features

- Realization of high transparency with emulator functions concentrated in a dedicated chip
- V850 core IE enabling easy product expansion
- V850E1 core IE enabling high-speed operation
- Connectable to various personal computers

Real-Time OSs (RX850, RX850 Pro)

■ Features

- Comply with global standard (µITRON 3.0 specifications).
- Support power management function.
- Enable embedding of required functions only (selection of system calls to be used).
- Support sophisticated task development through task debugger (RD).
- Support application operation analysis through system performance analyzer (AZ)
- Inherit attributes of real-time OS of 16-bit V Series and 78K Series

Task Debuggers (RD850, RD850 Pro)

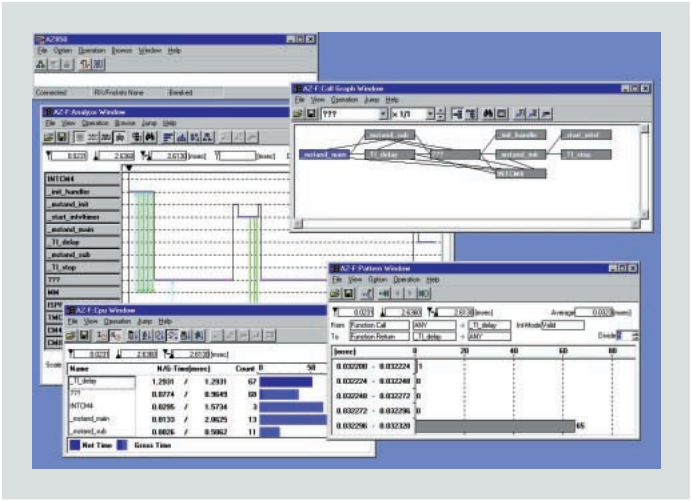
■ Features

- Display detailed information on OS resources such as tasks.
- Issue system calls.
- Display source of referenced tasks.
- Included with real-time OS (RX850, RX850 Pro)

System Performance Analyzer (AZ850)

■ Features

- Detection of bugs through system timing errors
- Detection of bugs due to simultaneous operation of complex tasks
- Detection/analysis of real-time system execution performance
- Operation linked to various debuggers



TCP/IP Software Library (RX-NET) for V850E Products

■ Product configuration

- TCP/IP protocol stack
- Applications
- LAN control driver

■ Features

- RFC-compliant
- Multiprotocol stack
- Support of numerous socket interfaces/libraries
- Support of applications as option products
- Simplified device driver
- Support of NEC real-time OS (RX850 Pro)

■ Target devices

V850E products

OSEK/VDX Specification-Compliant OS (RX-OSEK850)

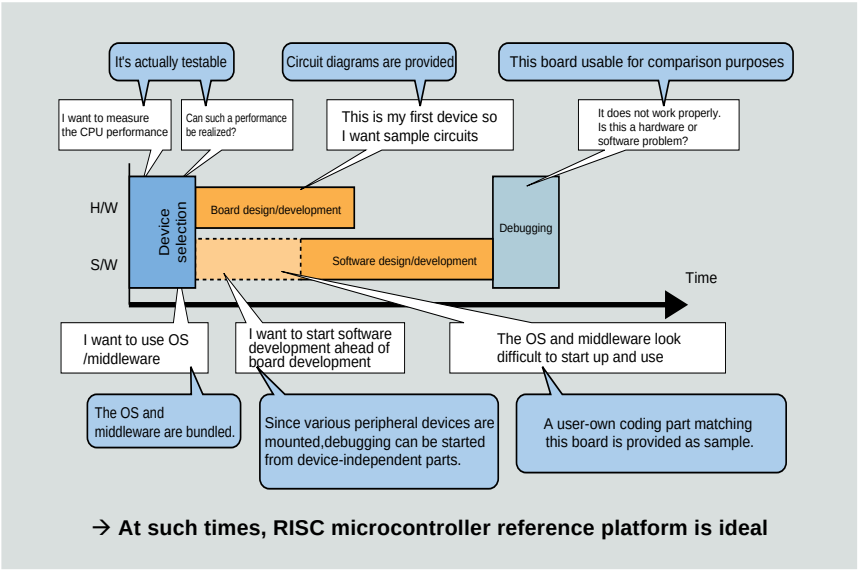
■ Features

- Kernel
  OSEK/VDX OS Ver. 2.0 specification-compliant
  Supports four conformance classes (BCC1, BCC2, ECC1, ECC2).
- Communications
  OSEK/VDX COM Ver. 2.1 Rev. 1 specification-compliant
  Supports three conformance classes (CCC1, CCC2, CCC3).
- Configurator
  Configurator simplifying construction of system information (OIL850)
  OIL Ver. 2.0-compliant format supported for configuration files
- Task debugger (RD-OSEK850)
  Task debugger effective for debugging applications that use the RX-OSEK850 included as standard.

RISC Microcontroller Reference Platform (SolutionGear™)

■ Features

- General-purpose evaluation boards available as development platforms for RISC microcontroller software
- Supported CPU: V850E/MA1
- Global and PC-compatible interfaces provided, including PCI, ISA, PCMCIA, E-IDE, Ethernet™, Serial, Parallel, PS/2, and USB
- Used combined with CPU-independent motherboard (usable in common with VR Series) and any of various CPU boards
- Real-time OS, middleware, and sample drivers are included.
- Development environment of Green Hills Software (evaluation version) provided
- MULTI/PARTNER remote monitor version can be used.
- Reference design information provided



→ **At such times, RISC microcontroller reference platform is ideal**

Cooperation with Third Parties

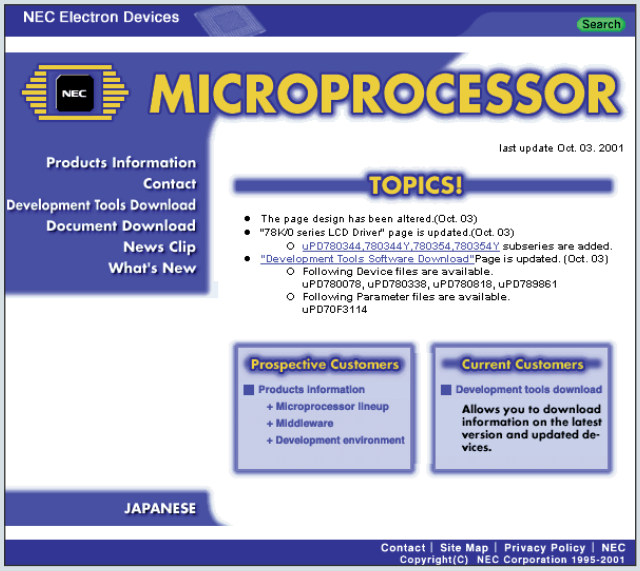
By strengthening its cooperation with third-party companies and creating tool groups that combine the best characteristics of NEC tools and third-party tools, NEC provides a development environment that answers diversified user needs.

Information

V850 Series Website Introduction

For information about the V850 Series and the V850 Series development environment, check out the NEC Microcomputer website.

http://www.ic.nec.co.jp/micro/index_e.html



Product Information

- Product information on the V850 Series, development environments for the V850 Series, and the middleware reference platform can be referenced.

Downloading Development Tools

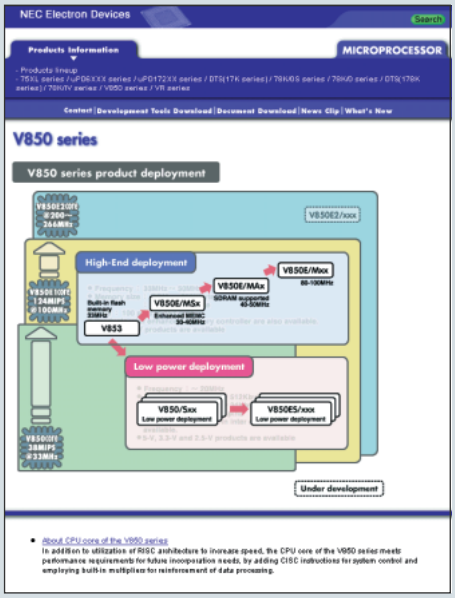
- Development tools for the V850 Series can be downloaded. Upgrade information is provided.

Downloading Documents

- Documents about the V850 Series and V850 Series development environment can be downloaded.

FAQ

- Answer to questions about the V850 Series development environment are introduced.



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TRON stands for The Realtime Operating system Nucleus.

ITRON is an abbreviation of Industrial TRON.

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Caution: The I^2C bus interface circuit is incorporated in the μPD703014AY, 703014BY, 703015AY, 703015BY, 70F3015BY, 703017AY, 70F3017AY, 703030AY, 703031AY, 703032AY, 70F3032AY, 703033AY, 70F3033AY, 703034AY, 703035AY, 70F3035AY, 703036AY, 703037AY, 70F3037AY, 703038Y, 70F3038Y, 703039Y, 703040Y, 70F3040Y, 703041Y, 703068Y, 703069Y, 703078Y, 703079Y, 70F3079Y, 703088Y, 703089Y, 70F3089Y, 703201Y, 70F3201Y, 703204Y, 70F3204Y. Those who use the I^2C bus interface can be granted the license below by giving prior notification before ordering the custom code.

Purchase of NEC I^2C components conveys a license under the Philips I^2C Patent Rights to use these components in an I^2C system, provided that the system conforms to the I^2C Standard Specification as defined by Philips.

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