

## FEATURES

- *Guaranteed* Reset Assertion at  $V_{CC} = 1V$
- Pin Compatible with LTC694/LTC695 for 3.3V Systems
- 200 $\mu$ A Typical Supply Current
- Fast (30ns Typ) On-Board Gating of RAM Chip Enable Signals
- SO-8 and SO-16 Packages
- 2.90V Precision Voltage Monitor
- Power OK/Reset Time Delay: 200ms or Adjustable
- Minimum External Component Count
- 1 $\mu$ A Maximum Standby Current
- Voltage Monitor for Power Fail or Low Battery Warning
- Thermal Limiting
- Performance Specified Over Temperature

## APPLICATIONS

- 3.3V Low Power Systems
- Critical  $\mu$ P Power Monitoring
- Intelligent Instruments
- Battery-Powered Computers and Controllers
- Automotive Systems

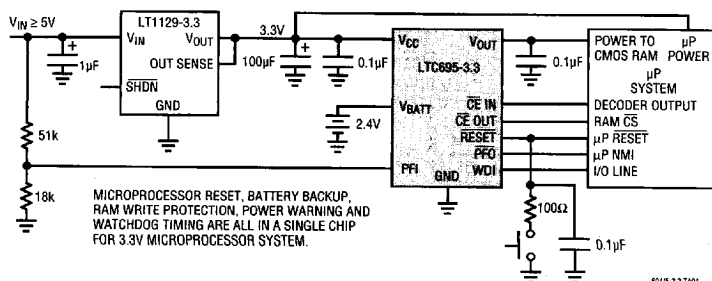
## DESCRIPTION

The LTC694-3.3/LTC695-3.3 provide complete 3.3V power supply monitoring and battery control functions. These include power-on reset, battery backup, RAM write protection, power failure warning and watchdog timing. The devices are pin compatible upgrades of the LTC694/LTC695 that are optimized for 3.3V systems. Operating power consumption has been reduced to 0.6mW (typical) and 3 $\mu$ W maximum in battery backup mode. Microprocessor reset and memory write protection are provided when the supply falls below 2.9V. The RESET output is guaranteed to remain logic low with  $V_{CC}$  as low as 1V.

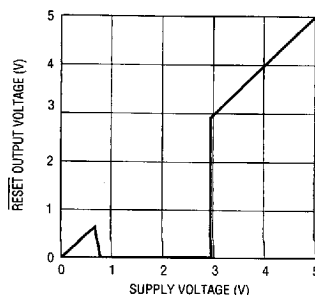
The LTC694-3.3/LTC695-3.3 power the active RAMs with a charge pumped NMOS power switch to achieve low dropout and low supply current. When primary power is lost, auxiliary power, connected to the battery input pin, powers the RAMs in standby through an efficient PMOS switch.

For an early warning of impending power failure, the LTC694-3.3/LTC695-3.3 provide an internal comparator with a user-defined threshold. An internal watchdog timer is also available, which forces the reset pins to active states when the watchdog input is not toggled prior to a preset time-out period.

## TYPICAL APPLICATION



**RESET Output Voltage vs  
Supply Voltage**



# LTC694-3.3/LTC695-3.3

## ABSOLUTE MAXIMUM RATINGS (Notes 1 and 2)

Terminal Voltage

$V_{CC}$  ..... -0.3V to 6V

$V_{BATT}$  ..... -0.3V to 6V

All Other Inputs ..... -0.3V to ( $V_{OUT} + 0.3V$ )

Input Current

$V_{CC}$  ..... 100mA

$V_{BATT}$  ..... 25mA

GND ..... 10mA

$V_{OUT}$  Output Current ..... Short-Circuit Protected

Power Dissipation ..... 500mW

Operating Temperature Range

LTC694C-3.3/LTC695C-3.3 ..... 0°C to 70°C

LTC694I-3.3/LTC695I-3.3 ..... -40°C to 85°C

Storage Temperature Range ..... -65°C to 150°C

Lead Temperature (Soldering, 10 sec) ..... 300°C

## PACKAGE/ORDER INFORMATION (Note 3)

<p><b>TOP VIEW</b></p> <p>LTC695-3.3</p> <p>N PACKAGE 16-LEAD PLASTIC DIP</p> <p><math>T_{JMAX} = 110^{\circ}\text{C}, \theta_{JA} = 130^{\circ}\text{C/W}</math></p>	<p><b>ORDER PART NUMBER</b></p> <p>LTC695CN-3.3 LTC695IN-3.3</p>	<p><b>TOP VIEW</b></p> <p>LTC695-3.3</p> <p>S PACKAGE 16-LEAD PLASTIC SOIC</p> <p><math>T_{JMAX} = 110^{\circ}\text{C}, \theta_{JA} = 130^{\circ}\text{C/W}</math></p>	<p><b>ORDER PART NUMBER</b></p> <p>LTC695CS-3.3 LTC695IS-3.3</p>
<p><b>TOP VIEW</b></p> <p>LTC694-3.3</p> <p>N8 PACKAGE 8-LEAD PLASTIC DIP</p> <p><math>T_{JMAX} = 110^{\circ}\text{C}, \theta_{JA} = 130^{\circ}\text{C/W}</math></p>	<p>LTC694CN-3.3 LTC694IN-3.3</p>	<p><b>TOP VIEW</b></p> <p>LTC694-3.3</p> <p>S8 PACKAGE 8-LEAD PLASTIC SOIC</p> <p><math>T_{JMAX} = 110^{\circ}\text{C}, \theta_{JA} = 180^{\circ}\text{C/W}</math></p>	<p>LTC694CS-3.3 LTC694IS-3.3</p> <p><b>S8 PART MARKING</b></p> <p>694 694I</p>

Consult factory for Military grade parts.

## PRODUCT SELECTION GUIDE

	PINS	RESET THRESHOLD (V)	WATCHDOG TIMER	BATTERY BACKUP	POWER FAIL WARNING	RAM WRITE PROTECT	PUSHBUTTON RESET	CONDITIONAL BATTERY BACKUP
LTC694-3.3	8	2.90	X	X	X			
LTC695-3.3	16	2.90	X	X	X	X		
LTC690	8	4.65	X	X	X			
LTC691	16	4.65	X	X	X	X		
LTC694	8	4.65	X	X	X			
LTC695	16	4.65	X	X	X	X		
LTC699	8	4.65	X					
LTC1232	8	4.37/4.62	X				X	
LTC1235	16	4.65	X	X	X	X	X	X

9-20



5518468 0011071 887

**ELECTRICAL CHARACTERISTICS** $V_{CC} = 3.3V$ ,  $V_{BATT} = 2V$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Battery Backup Switching						
Operating Voltage Range $V_{CC}$ $V_{BATT}$		● ●	3.0 1.5		5.50 2.75	V V
$V_{OUT}$ Output Voltage	$I_{OUT} = 1\text{mA}$	● ●	$V_{CC} - 0.1$ $V_{CC} - 0.2$	$V_{CC} - 0.01$ $V_{CC} - 0.01$		V V
	$I_{OUT} = 50\text{mA}$	●	$V_{CC} - 0.8$	$V_{CC} - 0.4$		V
$V_{OUT}$ in Battery Backup Mode	$I_{OUT} = 250\mu\text{A}$ , $V_{CC} < V_{BATT}$	●	$V_{BATT} - 0.1$	$V_{BATT} - 0.02$		V
Supply Current (Exclude $I_{OUT}$ )	$I_{OUT} \leq 50\text{mA}$ , $V_{CC} = 3.6\text{V}$	●		0.2 0.2	0.6 1.0	mA mA
Supply Current in Battery Backup Mode	$V_{CC} = 0\text{V}$ , $V_{BATT} = 2\text{V}$	●		0.04 0.04	1 5	$\mu\text{A}$ $\mu\text{A}$
Battery Standby Current (+ = Discharge, - = Charge)	$3.6\text{V} > V_{CC} > V_{BATT} + 0.2\text{V}$	●	-0.02 -0.10		0.02 0.10	$\mu\text{A}$ $\mu\text{A}$
Battery Switchover Threshold ( $V_{CC} - V_{BATT}$ )	Power Up Power Down			70 50		mV mV
Battery Switchover Hysteresis				20		mV
BATT ON Output Voltage (Note 4)	$I_{SINK} = 800\mu\text{A}$	●			0.3	V
BATT ON Output Short-Circuit Current (Note 4)	BATT ON = $V_{OUT}$ , Sink Current BATT ON = 0V, Source Current	●	0.5	25 1	25	mA $\mu\text{A}$
Reset and Watchdog Timer						
Reset Voltage Threshold		●	2.8	2.9	3.0	V
Reset Threshold Hysteresis				40		mV
Reset Active Time	OSC SEL HIGH, $V_{CC} = 3\text{V}$	● ●	160 140	200 200	240 280	ms ms
Watchdog Time-Out Period, Internal Oscillator	Long Period, $V_{CC} = 3\text{V}$	● ●	1.2 1.0	1.6 1.6	2.0 2.25	sec sec
	Short Period, $V_{CC} = 3\text{V}$	●	80 70	100 100	120 140	ms ms
Watchdog Time-Out Period, External Clock (Note 5)	Long Period, $V_{CC} = 3\text{V}$ Short Period, $V_{CC} = 3\text{V}$	● ●	4032 960		4097 1025	Clock Cycles
Reset Active Time PSRR				4		ms/V
Watchdog Time-Out Period PSRR, Internal OSC	Short Period Long Period			2 32		ms/V ms/V
Minimum WDI Input Pulse Width	$V_{IL} = 0.4\text{V}$ , $V_{IH} = 3\text{V}$	●	200			ns
RESET Output Voltage at $V_{CC} = 1\text{V}$	$I_{SINK} = 10\mu\text{A}$ , $V_{CC} = 1\text{V}$	●		4	200	mV
RESET and LOW LINE Output Voltage (Note 4)	$I_{SINK} = 400\mu\text{A}$ , $V_{CC} = 2.8\text{V}$	●			0.3	V
	$I_{SOURCE} = 1\mu\text{A}$ , $V_{CC} = 3\text{V}$	●	2.3			V
RESET and WDO Output Voltage (Note 4)	$I_{SINK} = 400\mu\text{A}$ , $V_{CC} = 3\text{V}$	●			0.3	V
	$I_{SOURCE} = 1\mu\text{A}$ , $V_{CC} = 2.8\text{V}$	●	2.3			V
RESET, RESET, WDO, LOW LINE Output Short-Circuit Current (Note 4)	Output Source Current	●	1	3	25	$\mu\text{A}$
	Output Sink Current			9		mA



**ELECTRICAL CHARACTERISTICS** $V_{CC} = 3.3V$ ,  $V_{BATT} = 2V$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
WDI Input Threshold	Logic Low Logic High	● ●	2.3	0.4	V V
WDI Input Current	WDI = $V_{OUT}$ WDI = 0V	● ●	4 -50	50	$\mu A$ $\mu A$
<b>Power Fail Detector</b>					
PFI Input Threshold		●	1.25	1.3	1.35 V
PFI Input Threshold PSRR			0.3		mV/V
PFI Input Current		●	$\pm 0.01$	$\pm 25$	nA
PFO Output Voltage (Note 4)	$I_{SINK} = 800\mu A$ $I_{SOURCE} = 1\mu A$	● ●	2.3	0.3	V V
PFO Short-Circuit Source Current (Note 4)	PFI = HIGH, PFO = 0V PFI = LOW, PFO = $V_{OUT}$	●	1	3 17	$\mu A$ mA
PFI Comparator Response Time (Falling)	$\Delta V_{IN} = -20mV$ , $V_{OD} = 15mV$			2	$\mu s$
PFI Comparator Response Time (Rising) (Note 4)	$\Delta V_{IN} = 20mV$ , $V_{OD} = 15mV$ with 10k $\Omega$ Pullup			40 8	$\mu s$ $\mu s$
<b>Chip Enable Gating</b>					
$\overline{CE}$ IN Threshold	$V_{IL}$ $V_{IH}$		1.9	0.45	V V
$\overline{CE}$ IN Pullup Current (Note 6)			3		$\mu A$
$\overline{CE}$ OUT Output Voltage	$I_{SINK} = 800\mu A$ $I_{SOURCE} = 400\mu A$ $I_{SOURCE} = 1\mu A$ , $V_{CC} = 0V$	● ● ●	$V_{OUT} - 0.50$ $V_{OUT} - 0.05$	0.3	V V V
$\overline{CE}$ IN Propagation Delay	$C_L = 20pF$	●	30	50	ns
$\overline{CE}$ OUT Output Short-Circuit Current	Output Source Current Output Sink Current		15 20		mA mA
<b>Oscillator</b>					
OSC IN Input Current (Note 6)			$\pm 2$		$\mu A$
OSC SEL Input Pullup Current (Note 6)			5		$\mu A$
OSC IN Frequency Range	OSC SEL = 0V OSC SEL = 0V, $C_{OSC} = 47pF$	●	0	125	kHz kHz

The ● denotes specifications which apply over the operating temperature range.

**Note 1:** Absolute maximum ratings are those values beyond which the life of device may be impaired.

**Note 2:** All voltage values are with respect to GND.

**Note 3:** For military temperature range parts, consult the factory.

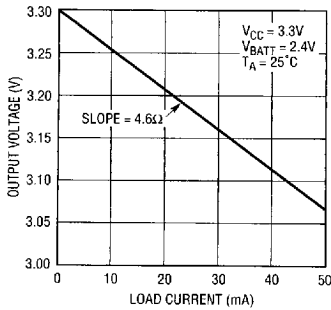
**Note 4:** The output pins of BATT ON, LOW LINE, PFO, WDO, RESET and RESET have weak internal pullups of typically 3 $\mu A$ . However, external pullup resistors may be used when higher speed is required.

**Note 5:** The external clock feeding into the circuit passes through the oscillator before clocking the watchdog timer. Variation in the time-out period is caused by phase errors which occur when the oscillator divides the external clock by 64. The resulting variation in the time-out period is 64 plus one clock of jitter.

**Note 6:** The input pins of  $\overline{CE}$  IN, OSC IN and OSC SEL have weak internal pullups which pull to the supply when the input pins are floating.

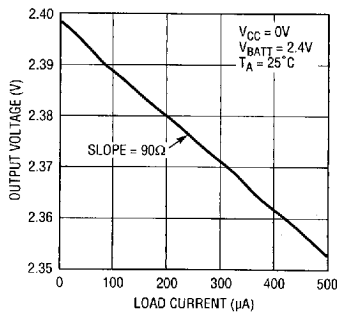
## TYPICAL PERFORMANCE CHARACTERISTICS

Output Voltage vs Load Current



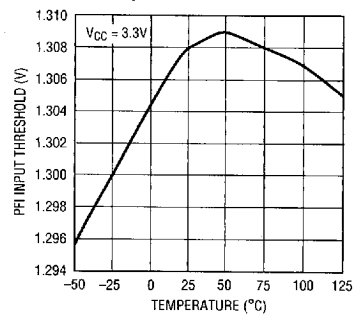
694-3.3 G01

Output Voltage vs Load Current



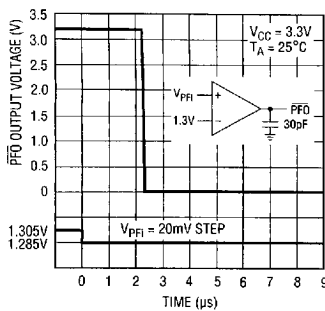
694-5-3.3 G02

Power Failure Input Threshold vs Temperature



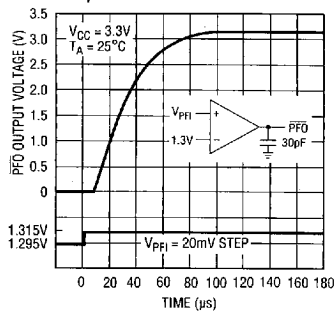
694-5-3.3 G03

Power Fail Comparator Response Time



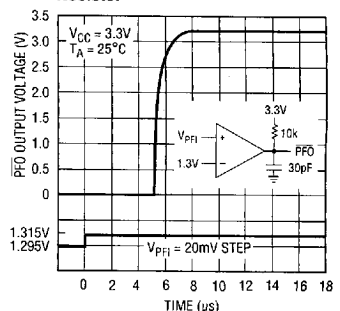
694-5-3.3 G04

Power Fail Comparator Response Time



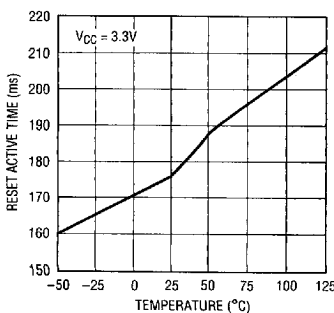
694-5-3.3 G05

Power Fail Comparator Response Time with Pullup Resistor



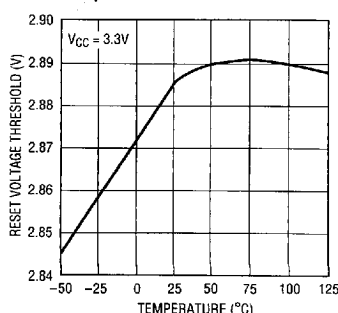
694-5-3.3 G06

Reset Active Time vs Temperature



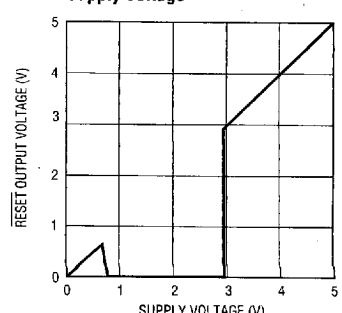
694-5-3.3 G07

Reset Voltage Threshold vs Temperature



694-5-3.3 G08

RESET Output Voltage vs Supply Voltage



694-5-3.3 TA02

## PIN FUNCTIONS

**V<sub>CC</sub>**: 3.3V Supply Input. The V<sub>CC</sub> pin should be bypassed with a 0.1μF capacitor.

**V<sub>OUT</sub>**: Voltage Output for Backed Up Memory. Bypass with a capacitor of 0.1μF or greater. During normal operation, V<sub>OUT</sub> obtains power from V<sub>CC</sub> through an NMOS power switch, M1, which can deliver up to 50mA and has a typical on resistance of 5Ω. When V<sub>CC</sub> is lower than V<sub>BATT</sub>, V<sub>OUT</sub> is internally switched to V<sub>BATT</sub>. If V<sub>OUT</sub> and V<sub>BATT</sub> are not used, connect V<sub>OUT</sub> to V<sub>CC</sub>.

**V<sub>BATT</sub>**: Backup Battery Input. When V<sub>CC</sub> falls below V<sub>BATT</sub>, auxiliary power connected to V<sub>BATT</sub>, is delivered to V<sub>OUT</sub> through PMOS switch, M2. If backup battery or auxiliary power is not used, V<sub>BATT</sub> should be connected to GND.

**GND**: Ground Pin.

**BATT ON**: Battery On Logic Output from Comparator C2. BATT ON goes low when V<sub>OUT</sub> is internally connected to V<sub>CC</sub>. The output typically sinks 25mA and can provide base drive for an external PNP transistor to increase the output current above the 50mA rating of V<sub>OUT</sub>. BATT ON goes high when V<sub>OUT</sub> is internally switched to V<sub>BATT</sub>.

**PFI**: Power Failure Input. PFI is the noninverting input to the power fail comparator, C3. The inverting input is internally connected to a 1.3V reference. The power failure output remains high when PFI is above 1.3V and goes low when PFI is below 1.3V. Connect PFI to GND or V<sub>OUT</sub> when C3 is not used.

**PFO**: Power Failure Output from C3. PFO remains high when PFI is above 1.3V and goes low when PFI is below 1.3V. When V<sub>CC</sub> is lower than V<sub>BATT</sub>, C3 is shut down and PFO is forced low.

**RESET**: Logic Output for μP Reset Control. Whenever V<sub>CC</sub> falls below either the reset voltage threshold (2.90V, typically) or V<sub>BATT</sub>, RESET goes active low. After V<sub>CC</sub> returns to 3.3V, the reset pulse generator forces RESET to remain active low for a minimum of 140ms. When the watchdog timer is enabled but not serviced prior to a preset time-out period, the reset pulse generator also forces RESET to active low for a minimum of 140ms for

every preset time-out period (see Figure 11). The reset active time is adjustable on the LTC695-3.3. An external pushbutton reset can be used in connection with the RESET output. See Pushbutton Reset in Applications Information section.

**RESET**: Active High Logic Output. It is the inverse of RESET.

**LOW LINE**: Logic Output from Comparator C1. LOW LINE indicates a low line condition at the V<sub>CC</sub> input. When V<sub>CC</sub> falls below the reset voltage threshold (2.90V typically), LOW LINE goes low. As soon as V<sub>CC</sub> rises above the reset voltage threshold, LOW LINE returns high (see Figure 1). LOW LINE goes low when V<sub>CC</sub> drops below V<sub>BATT</sub> (see Table 1).

**WDI**: Watchdog Input. WDI is a three-level input. Driving WDI either high or low for longer than the watchdog time-out period, forces both RESET and WDO low. Floating WDI disables the watchdog timer. The timer resets itself with each transition of the watchdog input (see Figure 11).

**WDO**: Watchdog Logic Output. When the watchdog input remains either high or low for longer than the watchdog time-out period, WDO goes low. WDO is set high whenever there is a transition on the WDI pin, or LOW LINE goes low. The watchdog timer can be disabled by floating WDI (see Figure 11).

**CE IN**: Logic Input to the Chip Enable Gating Circuit. CE IN can be derived from microprocessor's address line and/or decoder output. See Applications Information section and Figure 5 for additional information.

**CE OUT**: Logic Output on the Chip Enable Gating Circuit. When V<sub>CC</sub> is above the reset voltage threshold, CE OUT is a buffered replica of CE IN. When V<sub>CC</sub> is below the reset voltage threshold CE OUT is forced high (see Figure 5).

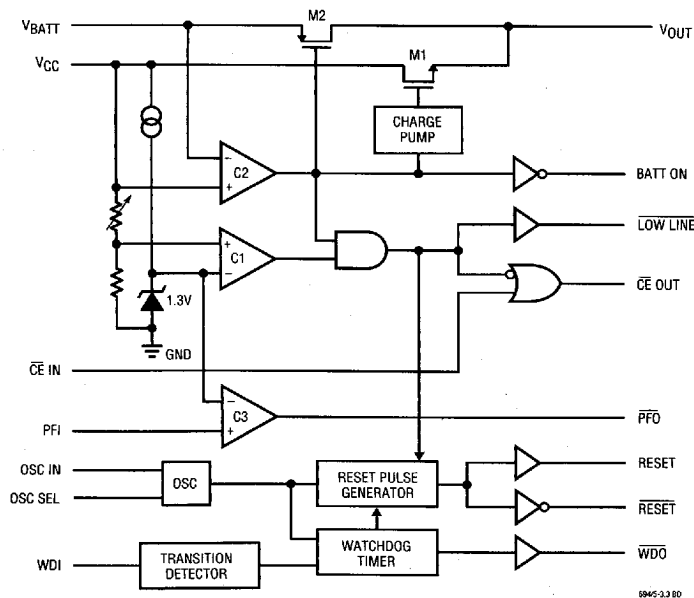
**OSC SEL**: Oscillator Selection Input. When OSC SEL is high or floating, the internal oscillator sets the reset active time and watchdog time-out period. Forcing OSC SEL low, allows OSC IN to be driven from an external clock signal or an external capacitor can be connected between OSC IN and GND.

## PIN FUNCTIONS

**OSC IN:** Oscillator Input. OSC IN can be driven by an external clock signal or an external capacitor can be connected between OSC IN and GND when OSC SEL is forced low. In this configuration the nominal reset active time and watchdog time-out period are determined by the number of clocks or set by the formula (see Applications

Information section). When OSC SEL is high or floating, the internal oscillator is enabled and the reset active time is fixed at 200ms typical for the LTC695-3.3. OSC IN selects between the 1.6 seconds and 100ms typical watchdog time-out periods. In both cases, the time-out period immediately after a reset is 1.6 seconds typical.

## BLOCK DIAGRAM



## APPLICATIONS INFORMATION

### Microprocessor Reset

The LTC694-3.3/LTC695-3.3 use a bandgap voltage reference and a precision voltage comparator C1 to monitor the 3.3V supply input on  $V_{CC}$  (see Block Diagram). When  $V_{CC}$  falls below the reset voltage threshold, the RESET output is forced to active low state. The reset voltage threshold accounts for a 10% variation on  $V_{CC}$ , so the RESET output becomes active low when  $V_{CC}$  falls below 3.0V (2.9V typical). On power-up, the RESET signal is held active low for a minimum of 140ms after reset voltage threshold is reached to allow the power supply and microprocessor to

### Battery Switchover

The battery switchover circuit compares  $V_{CC}$  to the  $V_{BATT}$  input, and connects  $V_{OUT}$  to whichever is higher. When  $V_{CC}$  rises to 70mV above  $V_{BATT}$ , the battery switchover comparator, C2, connects  $V_{OUT}$  to  $V_{CC}$  through a charge-pumped NMOS power switch, M1. When  $V_{CC}$  falls to 50mV above  $V_{BATT}$ , C2 connects  $V_{OUT}$  to  $V_{BATT}$  through a PMOS switch, M2. C2 has typically 20mV of hysteresis to prevent spurious switching when  $V_{CC}$  remains nearly equal to  $V_{BATT}$ . The response time of C2 is approximately 20 $\mu$ s.

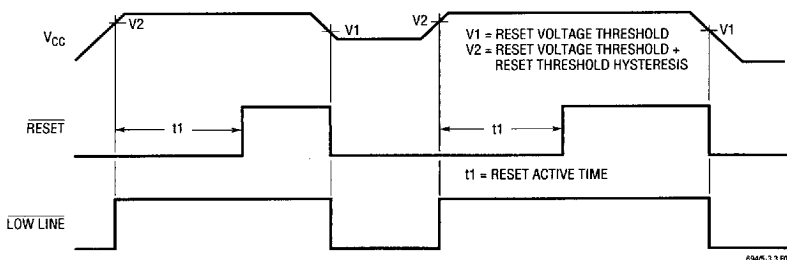


Figure 1. Reset Active Time

stabilize. The reset active time is adjustable on the LTC695-3.3. On power-down, the RESET signal remains active low even with  $V_{CC}$  as low as 1V. This capability helps hold the microprocessor in stable shutdown condition. Figure 1 shows the timing diagram of the RESET signal.

The precision voltage comparator, C1, typically has 40mV of hysteresis which ensures that glitches at  $V_{CC}$  pin do not activate the RESET output. Response time is typically 10 $\mu$ s. To help prevent mistripping due to transient loads, the  $V_{CC}$  pin should be bypassed with a 0.1 $\mu$ F capacitor with the leads trimmed as short as possible.

The LTC695-3.3 has two additional outputs: RESET and LOW LINE. RESET is an active high output and is the inverse of RESET. LOW LINE is the output of the precision voltage comparator C1. When  $V_{CC}$  falls below the reset voltage threshold, LOW LINE goes low. LOW LINE returns high as soon as  $V_{CC}$  rises above the reset voltage threshold.

During normal operation, the LTC694-3.3/LTC695-3.3 use a charge-pumped NMOS power switch to achieve low dropout and low supply current. This power switch can deliver up to 50mA to  $V_{OUT}$  from  $V_{CC}$  and has a typical on resistance of 5 $\Omega$ . The  $V_{OUT}$  pin should be bypassed with a capacitor of 0.1 $\mu$ F or greater to ensure stability. Use of a larger bypass capacitor is advantageous for supplying current to heavy transient loads.

When operating currents larger than 50mA are required from  $V_{OUT}$ , or a lower dropout ( $V_{CC} - V_{OUT}$  voltage differential) is desired, the LTC695-3.3 should be used. This product provides BATT ON output to drive the base of an external PNP transistor (Figure 2). If higher currents are needed with the LTC694-3.3, a high current Schottky diode can be connected from the  $V_{CC}$  pin to the  $V_{OUT}$  pin to supply the extra current.



## APPLICATIONS INFORMATION

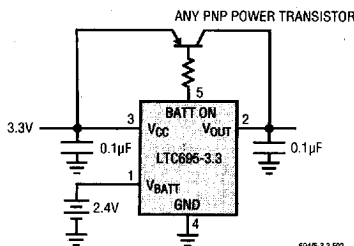


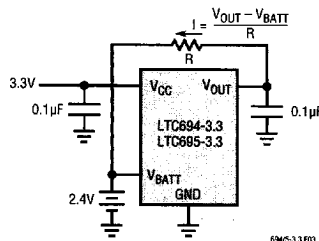
Figure 2. Using BATT ON to Drive External PNP Transistor

The LTC694-3.3/LTC695-3.3 are protected for safe area operation with short-circuit limit. Output current is limited to approximately 200mA. If the device is overloaded for a long period of time, thermal shutdown turns the power switch off until the device cools down. The threshold temperature for thermal shutdown is approximately 155°C with about 10°C of hysteresis which prevents the device from oscillating in and out of shutdown.

The PNP switch used in competitive devices was not chosen for the internal power switch because it injects unwanted current into the substrate. This current is collected by the  $V_{BATT}$  pin in competitive devices and adds to the charging current of the battery which can damage lithium batteries. The LTC694-3.3/LTC695-3.3 use a charge-pumped NMOS power switch to eliminate unwanted charging current while achieving low dropout and low supply current. Since no current goes to the substrate, the current collected by  $V_{BATT}$  pin is strictly junction leakage.

A 125Ω PMOS switch connects the  $V_{BATT}$  input to  $V_{OUT}$  in battery backup mode. The switch is designed for very low dropout voltage (input-to-output differential). This feature is advantageous for low current applications such as battery backup in CMOS RAM and other low power CMOS circuitry. The supply current in battery backup mode is 1µA maximum.

The operating voltage at the  $V_{BATT}$  pin ranges from 1.5V to 2.75V. The charging resistor for rechargeable batteries should be connected to  $V_{OUT}$  since this eliminates the discharge path that exists when the resistor is connected to  $V_{CC}$  (Figure 3).

Figure 3. Charging External Battery Through  $V_{OUT}$ 

## Replacing the Backup Battery

When changing the backup battery with system power on, spurious resets can occur while the battery is removed due to battery standby current. Although battery standby current is only a tiny leakage current, it can still charge up the stray capacitance on the  $V_{BATT}$  pin. The oscillation cycle is as follows: When  $V_{BATT}$  reaches within 50mV of  $V_{CC}$ , the LTC694-3.3/LTC695-3.3 switch to battery backup.  $V_{OUT}$  pulls  $V_{BATT}$  low and the device goes back to normal operation. The leakage current then charges up the  $V_{BATT}$  pin again and the cycle repeats.

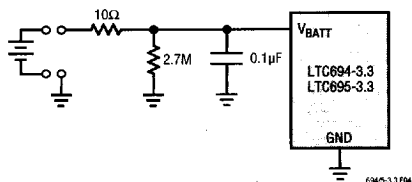
If spurious resets during battery replacement pose no problems, then no action is required. Otherwise, a resistor from  $V_{BATT}$  to GND will hold the pin low while changing the battery. For example, the battery standby current is 1µA maximum over temperature so the external resistor required to hold  $V_{BATT}$  below  $V_{CC}$  is:

$$R \leq \frac{V_{CC} - 50\text{mV}}{1\mu\text{A}}$$

With  $V_{CC} = 3\text{V}$ , a 2.7M resistor will work. With a 2V battery, this resistor will draw only 0.7µA from the battery, which is negligible in most cases.

If battery connections are made through long wires, a 10Ω to 100Ω series resistor and a 0.1µF capacitor are recommended to prevent any overshoot beyond  $V_{CC}$  due to the lead inductance (Figure 4).

## APPLICATIONS INFORMATION



**Figure 4.** 10Ω/0.1μF combination eliminates inductive overshoot and prevents spurious resets during battery replacement. The 2.7M pulls the  $V_{BATT}$  pin to ground while the battery is removed, eliminating spurious resets.

**Table 1.** Input and Output Status in Battery Backup Mode

SIGNAL	STATUS
$V_{CC}$	C2 monitors $V_{CC}$ for active switchover.
$V_{OUT}$	$V_{OUT}$ is connected to $V_{BATT}$ through an internal PMOS switch.
$V_{BATT}$	The supply current is 1μA maximum.
BATT ON	Logic high. The open-circuit output voltage is equal to $V_{OUT}$ .
PFI	Power Failure Input is ignored.
PFO	Logic low
RESET	Logic low
RESET	Logic high. The open-circuit output voltage is equal to $V_{OUT}$ .
LOW LINE	Logic low
WDI	Watchdog Input is ignored.
WDO	Logic high. The open-circuit output voltage is equal to $V_{OUT}$ .
CE IN	Chip Enable Input is ignored.
CE OUT	Logic high. The open-circuit output voltage is equal to $V_{OUT}$ .
OSC IN	OSC IN is ignored.
OSC SEL	OSC SEL is ignored.

Table 1 shows the state of each pin during battery backup. When the battery switchover section is not used, connect  $V_{BATT}$  to GND and  $V_{OUT}$  to  $V_{CC}$ .

## Memory Protection

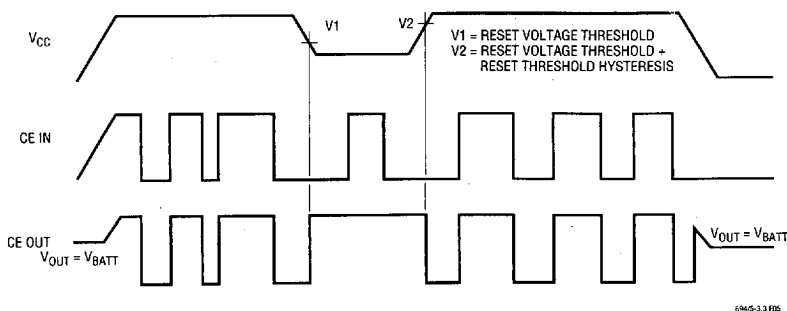
The LTC695-3.3 includes memory protection circuitry which ensures the integrity of the data in memory by preventing write operations when  $V_{CC}$  is at invalid level. Two additional pins, CE IN and CE OUT, control the Chip Enable or Write inputs of CMOS RAM. When  $V_{CC}$  is 3.3V, CE OUT follows CE IN with a typical propagation delay of 30ns. When  $V_{CC}$  falls below the reset voltage threshold or  $V_{BATT}$ , CE OUT is forced high, independent of CE IN. CE OUT is an alternative signal to drive the CE, CS, or Write input of battery backed up CMOS RAM. CE OUT can also be used to drive the Store or Write input of an EEPROM, EAROM or NOVRAM to achieve similar protection. Figure 5 shows the timing diagram of CE IN and CE OUT.

CE IN can be derived from the microprocessor's address decoder output. Figure 6 shows a typical nonvolatile CMOS RAM application.

Memory protection can also be achieved with the LTC694-3.3 by using RESET as shown in Figure 7.

## Power Fail Warning

The LTC694-3.3/LTC695-3.3 generate a Power Failure Output (PFO) for early warning of failure in the microprocessor's power supply. This is accomplished by



**Figure 5.** Timing Diagram for CE IN and CE OUT

## APPLICATIONS INFORMATION

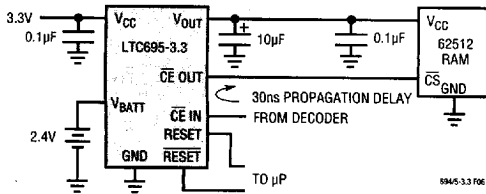


Figure 6. A Typical Nonvolatile CMOS RAM Application

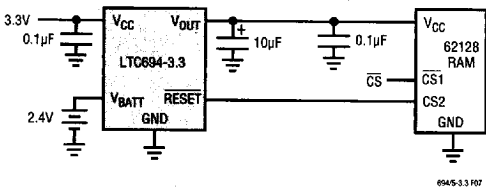


Figure 7. Write Protect for RAM with LTC694-3.3

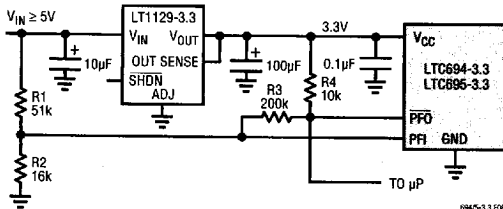


Figure 8. Monitoring Unregulated DC Supply with the LTC694-3.3/LTC695-3.3's Power Fail Comparator

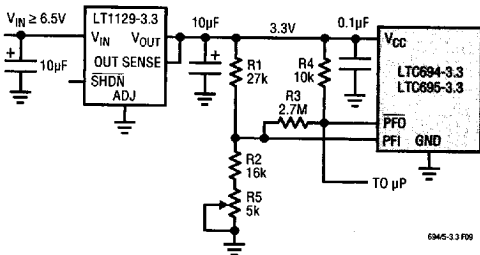


Figure 9. Monitoring Regulated DC Supply with the LTC694-3.3/LTC695-3.3's Power Fail Comparator

comparing the power failure input (PFI) with an internal 1.3V reference.

$\overline{\text{PFO}}$  goes low when the voltage at the PFI pin is less than 1.3V. Typically PFI is driven by an external voltage divider (R1 and R2 in Figures 8 and 9) which senses either an unregulated DC input or a regulated 3.3V output. The voltage divider ratio can be chosen such that the voltage at the PFI pin falls below 1.3V several milliseconds before the 3.3V supply falls below the maximum reset voltage threshold 3.0V.  $\overline{\text{PFO}}$  is normally used to interrupt the microprocessor to execute shutdown procedure between  $\overline{\text{PFO}}$  and RESET or RESET.

The power fail comparator, C3, does not have hysteresis. Hysteresis can be added however, by connecting a resistor between the  $\overline{\text{PFO}}$  output and the noninverting PFI input pin as shown in Figures 8 and 9. The upper and lower trip points in the comparator are established as follows:

When  $\overline{\text{PFO}}$  output is low, R3 sinks current from the summing junction at the PFI pin.

$$V_H = 1.3V \left( 1 + \frac{R_1}{R_2} + \frac{R_1}{R_3} \right)$$

When  $\overline{\text{PFO}}$  output is high, the series combination of R3 and R4 source current into the PFI summing junction.

$$V_L = 1.3V \left( 1 + \frac{R_1}{R_2} - \frac{(3.3V - 1.3V) R_1}{1.3V(R_3 + R_4)} \right)$$

$$\text{Assuming } R_4 \ll R_3, V_{\text{HYSTERESIS}} = 3.3V \frac{R_1}{R_3}$$

**Example 1:** The circuit in Figure 8 demonstrates the use of the power fail comparator to monitor the unregulated power supply input. Assuming the rate of decay of the supply input  $V_{IN}$  is 100mV/ms and the total time to execute a shutdown procedure is 8ms. Also the noise of  $V_{IN}$  is 200mV. With these assumptions in mind, we can reasonably set  $V_L = 5V$  which is 1.6V greater than the sum of maximum reset voltage threshold and the dropout voltage of the LT1129-3.3 (3V + 0.4V) and  $V_{\text{HYSTERESIS}} = 850mV$ .

## APPLICATIONS INFORMATION

$$V_{HYSTERESIS} = 3.3V \frac{R_1}{R_3} = 850mV$$

$$R_3 \approx 3.88 R_1$$

Choose  $R_3 = 200k$  and  $R_1 = 51k$ . Also select  $R_4 = 10k$  which is much smaller than  $R_3$ .

$$5V = 1.3V \left( 1 + \frac{51k}{R_2} - \frac{(3.3V - 1.3V)51k}{1.3V(210k)} \right)$$

$R_2 = 15.8k$ , Choose nearest 5% resistor 16k and recalculate  $V_L$ .

$$V_L = 1.3V \left( 1 + \frac{51k}{16k} - \frac{(3.3V - 1.3V)51k}{1.3V(210k)} \right) = 4.96V$$

$$V_H = 1.3V \left( 1 + \frac{51k}{16k} + \frac{51k}{200k} \right) = 5.77V$$

$$\frac{(4.96V - 3.4V)}{100mV/ms} = 15.6ms$$

$$V_{HYSTERESIS} = 5.77V - 4.96V = 810mV$$

The 15.6ms allows enough time to execute shutdown procedure for microprocessor and 810mV of hysteresis would prevent  $\overline{PFO}$  from going low due to the noise of  $V_{IN}$ .

**Example 2:** The circuit in Figure 9 can be used to measure the regulated 3.3V supply to provide early warning of power failure. Because of variations in the PFI threshold, this circuit requires adjustment to ensure the PFI comparator trips before the reset threshold is reached. Adjust  $R_5$  such that the  $\overline{PFO}$  output goes low when the  $V_{CC}$  supply reaches the desired level (e.g., 3.1V).

## Monitoring the Status of the Battery

C3 can also monitor the status of the memory backup battery (Figure 10). If desired, the  $\overline{CE OUT}$  can be used to apply a test load to the battery. Since  $\overline{CE OUT}$  is forced high in battery backup mode, the test load will not be applied to the battery while it is in use, even if the microprocessor is not powered.

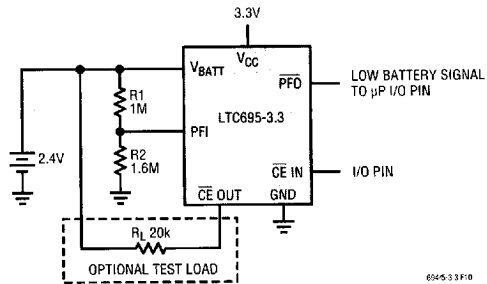


Figure 10. Backup Battery Monitor with Optional Test Load

## Watchdog Timer

The LTC694-3.3/LTC695-3.3 provide a watchdog timer function to monitor the activity of the microprocessor. If the microprocessor does not toggle the watchdog input (WDI) within a selected time-out period,  $\overline{RESET}$  is forced to active low for a minimum of 140ms. The reset active time is adjustable on the LTC695-3.3. Since many systems can not service the watchdog timer immediately after a reset, the LTC695-3.3 has a longer time-out period (1.0 second minimum) right after a reset is issued. The normal time-out period (70ms minimum) becomes effective following the first transition of WDI after  $\overline{RESET}$  is inactive. The watchdog time-out period is fixed at 1.0 second minimum on the LTC694-3.3. Figure 11 shows the timing diagram of watchdog time-out period and reset active time. The watchdog time-out period is restarted as soon as  $\overline{RESET}$  is inactive. When either a high-to-low or low-to-high transition occurs at the WDI pin prior to time-out, the watchdog time is reset and begins to time out again. To ensure the watchdog time does not time out, either a high-to-low or low-to-high transition on the WDI pin must occur at or less than the minimum time-out period. If the input to the WDI pin remains either high or low, reset pulses will be issued every 1.6 seconds typically. The watchdog time can be deactivated by floating the WDI pin. The timer is also disabled when  $V_{CC}$  falls below the reset voltage threshold or  $V_{BATT}$ .

## APPLICATIONS INFORMATION

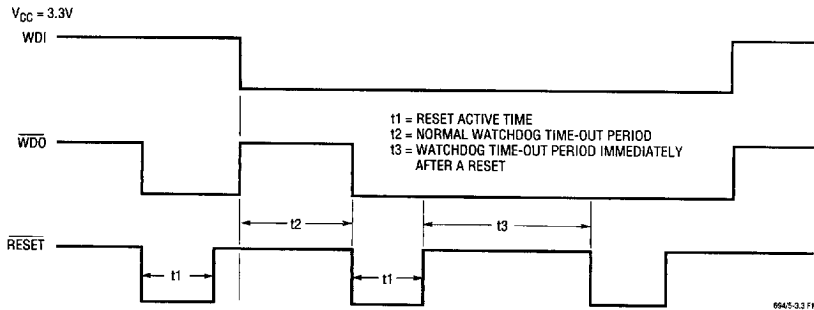


Figure 11. Watchdog Time-Out Period and Reset Active Time

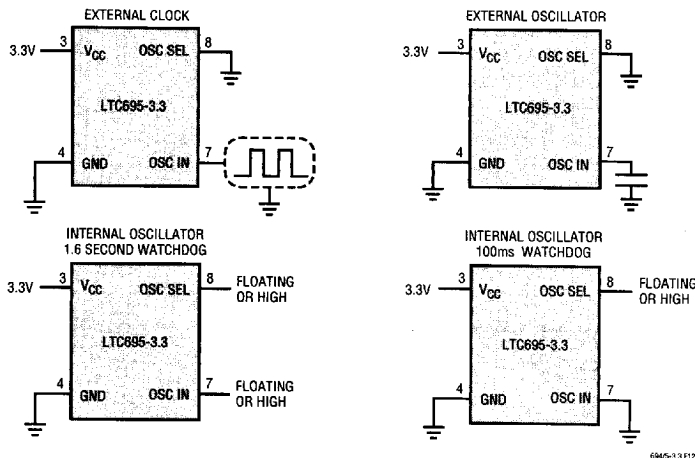


Figure 12. Oscillator Configurations

The LTC695-3.3 provides an additional output (Watchdog Output,  $\overline{\text{WDO}}$ ) which goes low if the watchdog timer is allowed to time out and remains low until set high by the next transition on the WDI pin.  $\overline{\text{WDO}}$  is also set high when  $V_{CC}$  falls below the reset voltage threshold or  $V_{BATT}$ .

The LTC695-3.3 has two additional pins, OSC SEL and OSC IN, which allow reset active time and watchdog time-out period to be adjusted per Table 2. Several configurations are shown in Figure 12.

OSC IN can be driven by an external clock signal or an external capacitor can be connected between OSC IN and GND when OSC SEL is forced low. In these configurations, the nominal reset active time and watchdog time-out period are determined by the number of clocks or set by the formula in Table 2. When OSC SEL is high or floating, the internal oscillator is enabled and the reset active time is fixed at 140ms minimum for the LTC695-3.3. OSC IN selects between the 1 second and 70ms minimum normal watchdog time-out periods. In both cases, the time-out period immediately after a reset is at least 1 second.

## APPLICATIONS INFORMATION

Table 2. LTC695-3.3 Reset Active Time and Watchdog Time-Out Selections

OSC SEL	OSC IN	WATCHDOG TIME-OUT PERIOD		RESET ACTIVE TIME
		NORMAL (Short Period)	IMMEDIATELY AFTER RESET (Long Period)	LTC695-3.3
Low	External Clock Input	1024 CLKs	4096 CLKs	2048 CLKs
Low	External Capacitor*	$\frac{400\text{ms}}{70\text{pF}} \times C$	$\frac{1.6\text{ sec}}{70\text{pF}} \times C$	$\frac{800\text{ms}}{70\text{pF}} \times C$
Floating or High	Low	100ms	1.6 sec	200ms
Floating or High	Floating or High	1.6 sec	1.6 sec	200ms

\*The nominal internal frequency is 10.24kHz. The nominal oscillator frequency with external capacitor is  $F_{\text{OSC}} (\text{Hz}) = \frac{184,000}{C(\text{pF})}$

### Pushbutton Reset

The LTC694-3.3/LTC695-3.3 do not provide a logic input for direct connection to a pushbutton. However, a pushbutton in series with a 100Ω resistor connected to the RESET output pin (Figure 13) provides an alternative for manual reset. Connecting a 0.1μF capacitor to the RESET pin debounces the pushbutton input.

The 100Ω resistor in series with the pushbutton is required to prevent the ringing, due to the capacitance and lead inductance, from pulling the RESET pins of the MPU and LTC69X below ground.

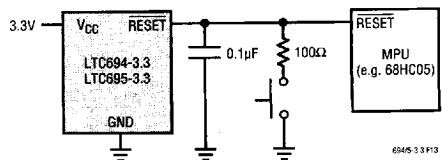
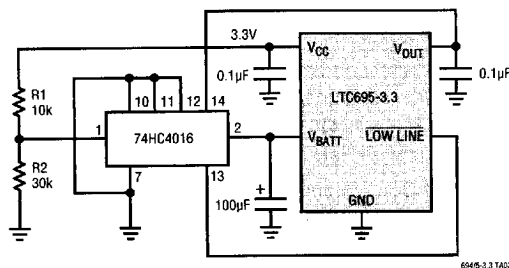


Figure 13. The External Pushbutton Reset

## TYPICAL APPLICATIONS

### Capacitor Backup with 74HC4016 Switch



## TYPICAL APPLICATIONS

Write Protect for Additional RAMs

