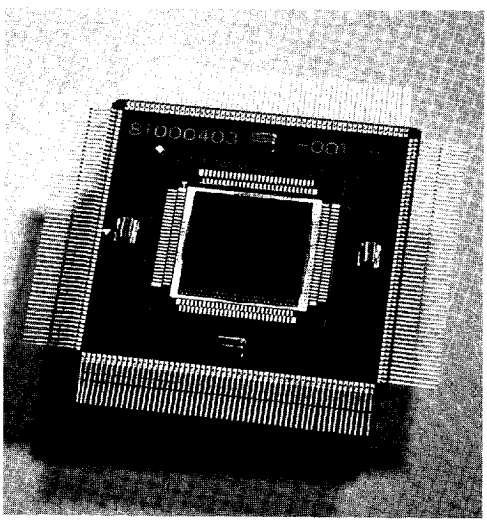
Features

- 1.0 µ Drawn Gate Length High-performance CMOS Gate Arrays
- All ATL Gate Arrays are Specified from 3.0 Volts to 5.5 Volts, for Standard and Low Voltage Applications
- Design Translation of Existing ASIC Designs Provide for Easy Alternate Sourcing with Equivalent or Improved Performance
- EPLD/FPGA Conversions to ATL Gate Array, Several EPLD and FPGA can be Combined into a Single Gate Array.
- ATL C Version, Fine Pad Pitch Gate Arrays are Ideal for High I/O, Low Gate Count Designs (Commercial, Industrial Only)
- ATL Gate Arrays can be Supplied Compliant to MIL-STD-883
- Improved Product Testability Using Serial Scan, Boundary Scan, JTAG and Built-in-self-test

Description

The high-performance ATL Series CMOS gate arrays employ 1.0 µ-drawn, double-level metal, Si-gate, CMOS technology processed in Atmel's U.S.-based, advanced manufacturing facility. The arrays utilize an enhanced channelless architecture which results in greater than 50 percent usable gates.

Atmel's flexible design system uses industry design standards and is compatible with popular CAD/CAE software and hardware packages. The customer can start designing with the ATL series today using existing CAD/CAE tools.



ATL Series Gate Arrays

ATL4
ATL10
ATL20
ATL40
ATL60
ATL75
ATL100
ATL130
ATL160

ATL7C
ATL10C
ATL15C
ATL20C
ATL35C
ATL55C
ATL75C

4

ATL Array Organization

Device Number	Maximum Gates	Routable Gates	Max Pin Count	Max I/O(1) Pins	Gate(2) Speed
ATL4	4,100	2,600	68	60	375 ps
ATL10	10,000	6,500	124	116	375 ps
ATL20	22,000	12,000	144	136	375 ps
ATL40	40,000	22,000	180	168	375 ps
ATL60	57,000	30,000	224	208	375 ps
ATL75	72,000	38,000	256	236	375 ps
ATL100	95,000	50,000	292	262	375 ps
ATL130	131,000	67,000	338	308	375 ps
ATL160	157,000	80,000	360	320	375 ps

ATL C Array Organization - Fine Pad Pitch

Device Number	Maximum Gates	Routable Gates	Max Pin Count	Max I/O(1) Pins	Gate(2) Speed
ATL7C	7,000	4,000	100	92	375 ps
ATL10C	10,000	6,000	120	112	375 ps
ATL15C	15,000	8,000	144	136	375 ps
ATL20C	22,000	12,000	160	152	375 ps
ATL35C	35,000	18,000	208	192	375 ps
ATL55C	55,000	29,000	256	236	375 ps
ATL75C	75,000	39,000	304	280	375 ps

Notes: 1. Absolute maximum I/O pins is maximum pin count minus 8. Additional power and ground pins are assumed to be required to support simultaneous switching outputs as pin count increases.
2. Nominal 2 input nand gate with a fan out of 2

ATL Design

Design Systems Supported

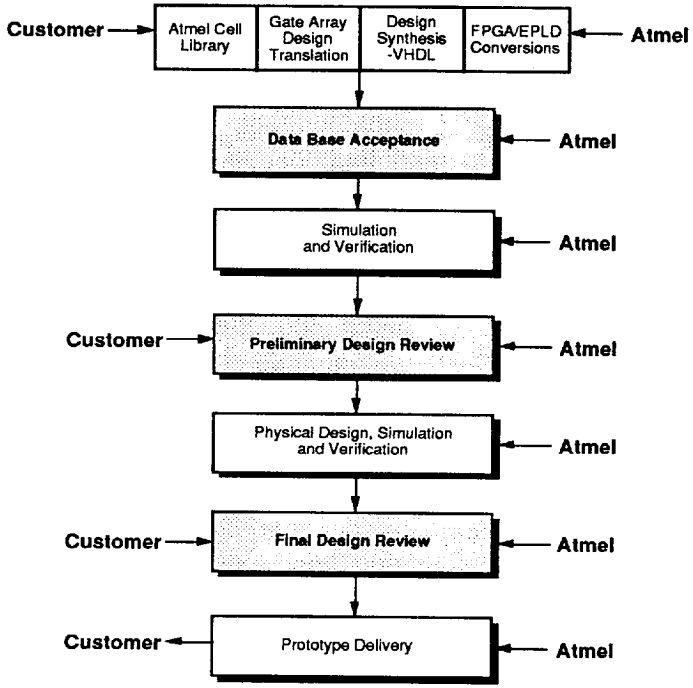
Atmel supports the major CAE/CAD software systems with complete macro cell libraries (symbols, timing and function), as well as utilities for checking the netlist and accurate pre-route delay simulations. Atmel uses Cadence's Verilog-XL as our golden simulator. The following design systems are supported:

Cadence	Viewlogic	Mentor	Dazix
Valid	Synopsys	Racal-Redac	

Design Flow

While Atmel provides four options for implementing a gate array design, they all have the same flow. Data base acceptance is the first milestone. This is when Atmel receives and accepts the complete design data base. Preliminary design review is where the performance of the design is set based on the Cadence simulation. Final design review is the last review of the design before making masks. The back annotation data is incorporated into the simulations. After final design review masks are released and prototypes in ceramic packages are delivered.

ATL Gate Array Design Flow



Design Options

Schematic Capture

Schematic capture and simulation are performed by the customer using an Atmel supplied macro cell library. The customer can also receive complete back annotation delay data for post-route simulation.

VHDL/Verilog-HDL

Atmel can accept Register Transfer level (RTL) designs for VHDL (MIL-STD-454, IEEE STD 1076) or Verilog-HDL format. Atmel fully supports Synopsys for VHDL simulation as well as synthesis. Design via VHDL or Verilog-HDL is the preferred method of performing a gate array design.

ASIC Design Translation

Atmel has successfully translated dozens of existing designs from most major ASIC vendors (LSI Logic, Oki, NEC, Fujitsu and others) into our ATL series gate arrays. These designs have been optimized for speed, gate count, modified to add logic or memory, or replicated for a pin-for-pin compatible, drop-in replacement.

FPGA and EPLD Conversions

Atmel has successfully translated existing FPGA/EPLD designs from most major vendors (Xilinx, Actel, Altera, AMD & Atmel) into our ATL series gate arrays. The design can be optimized for speed or power consumption, modified to add logic or memory or replicated for a pin-for-pin compatible, drop-in replacement. Atmel frequently combines several devices onto a single gate array.

ATL Series Cell Library

Atmel's ATL series gate arrays use cells from an accurately modeled and highly flexible library. The cell library contains over 120 hard-wired data path elements and has been characterized via extensive SPICE modeling at the transistor level and verified through measurements made on fabricated test arrays. Characterization has been performed over the military temperature and voltage ranges, to ensure that the simulation accurately predicts the performance of the finished product. Atmel is continually expanding the ATL series cell library with both soft and hard macros. Check with your sales representative for the most recent additions.

Cell Guide

Buffers and Inverters

1x Buffer	1x Inverter
2x Buffer	Dual 1x Inverter
2x Buffer with Enable	Quad 1x Inverter
2x Buffer with Enable Low	Quad Tri-state Inverter
3x Buffer	2x Inverter
4x Buffer	Dual 2x Inverter
8x Buffer	2x Tri-state Inverter
12x Buffer	3x Inverter
16x Buffer	4x Inverter
Delay Buffer 2.0 ns	8x Inverter
Delay Buffer 3.5 ns	10x Inverter
Delay Buffer 8.0 ns	

AND, NAND, OR, NOR Gates

2 input AND	2 input NOR
2 input AND with High Drive	Dual 2 input NOR
3 input AND	2 input NOR with High Drive
3 input AND with High Drive	3 input NOR
4 input AND	3 input NOR with High Drive
4 input AND with High Drive	4 input NOR
5 input AND	4 input NOR with High Drive
2 input NAND	5 input NOR
Dual 2-input NAND	8 input NOR
2 input NAND with High Drive	16 input NOR with High Drive
3 input NAND	2 input OR
3 input NAND with High Drive	2 input OR with High Drive
4 input NAND	3 input OR
4 input NAND with High Drive	3 input OR with High Drive
5 input NAND	4 input OR
5 input NAND with High Drive	4 input OR with High Drive
6 input NAND	
6 input NAND with High Drive	
8 input NAND	
8 input NAND with High Drive	

Cell Guide

Multiplexers	
2:1 MUX	4:1 MUX
2:1 MUX with High Drive	4:1 MUX w/o Buffered Inputs
Inverting 2:1 MUX w/o Buffered Inputs	4:1 MUX w/o Buffered Inputs, High Drive
Inverting 2:1 MUX w/o Buffered Inputs, High Drive	5:1 MUX with High Drive
2:1 MUX with Enable Low	8:1 MUX
Quad 2:1 MUX with Enable	8:1 MUX with Enable Low
Quad 2:1 MUX	8:1 MUX High Drive
Inverting 3:1 MUX w/o Buffered Inputs	
Inverting 3:1 MUX w/o Buffered Inputs, High Drive	

AND/OR, OR/AND Gates	
3 input AND OR INVERT	3 input OR AND INVERT
3 input AND OR INVERT with High Drive	3 input OR AND INVERT with High Drive
4 input AND OR INVERT	4 input OR AND INVERT
4 input AND OR INVERT with High Drive	4 input OR AND INVERT with High Drive
6 input AND OR INVERT	8 input OR AND INVERT
6 input AND OR INVERT with High Drive	4 input OR AND INVERT with 2 inputs to AND

Exclusive OR/NOR Gates	
1 bit Adder	2 input Exclusive OR with High Drive
1 bit Adder with Buffered Outputs	2 input Exclusive NOR
7 input Carry Lookahead	2 input Exclusive NOR with High Drive
2 input Exclusive OR	

Decoders	
2:4 Decoder	3:8 Decoder with Low Enable
2:4 Decoder with Low Enable	

Flip-flops/Latches	
D Flip-flop	LATCH
D Flip-flop with Clear/Preset	LATCH with Complementary Outputs
D Flip-flop with Clear	LATCH with Inverted Gate Signal
D Flip-flop with High Drive	QUAD LATBG with Common Gate Signal
D Flip-flop with Reset	LATCH with High Drive
D Flip-flop with Set	QUAD Inverting LATCH
D Flip-flop with Set/Reset	LATCH with Reset
JK Flip-flop	LATCH with Set
JK Flip-flop with Clear/Preset	LATCH with Set and Reset
JK Flip-flop with Clear	

Cell Guide

Scan Cells	
Set-scan Register	Set-scan Register with Set
Set-scan Register with Clear and Preset	Set-scan Register with Set and Reset
Set-scan Register with Reset	

I/O Options

Input, Output, Bidirectional, Tristate Output, Internal Clock Driver and Oscillator

Output Drive Value Programmable from 2 mA to 24 mA in 2 mA increments with Slew Rate Control

CMOS or TTL Operation

Schmitt Trigger (Bidirectional, Input)

Testable NAND Gate on Input (Bidirectional, Input)

Inverting and Non-inverting Input Buffers (Bidirectional, Input)

Pullup Resistor - 10K Ω to 310K Ω

Pulldown Resistor - 3.5K Ω to 108.5K Ω

74XX Series Soft Macros

24 cells available

HDL Macros - Available in Verilog-HDL or VHDL Simulation Models

Function Group	Available Cells
adder	37
alu	29
baud rate generator	3
comparator	18
counter	27
fifo	56
incrementor/decrementor	60
mux	7
parity/error correction	15
scan	31
shifter	9
multipliers	10

CMOS/TTL Input Interface Characteristics

Interface	Logic High	Logic Low	Switchpoint
CMOS	3.5 V Minimum	1.5 V Maximum	$V_{dd}/2$ Typical
TTL	2.0 V Minimum	0.8 V Maximum	1.4 V Typical

Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0 V to +7.0 V[1]
Maximum Operating Voltage	6.0 V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Notes:
1. Minimum voltage is -0.6 V dc which may undershoot to -2.0 V for pulses of less than 20 ns. Maximum output pin voltage is V_{dd} + 0.75 V dc which may overshoot to +7.0 V for pulses of less than 20 ns.

5.0 Volt DC Characteristics

Applicable over recommended operating range from T_a = -55°C to +125°C, V_{dd} = 4.5 V to 5.5 V (unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
I_{IH}	Input Leakage High	$V_{IN} = V_{dd}$, V_{dd} = 5.5 V		.01	10	µA
I_{IL}	Input Leakage Low (no pull-up)	$V_{IN} = V_{SS}$, V_{dd} = 5.5 V	-10	.01		µA
	40K pull-up	$V_{IN} = V_{SS}$, V_{dd} = 5.5 V	-325	-160	-40	µA
I_{OZ}	Output Leakage (no pull-up)	$V_{IN} = V_{dd}$ or V_{SS}, V_{dd} = 5.5 V	-10	.01	10	µA
I_{OS}	Output Short Circuit Current (3 x Buffer)[2]	V_{dd} = 5.5 V, $V_{OUT} = V_{dd}$	10	50	100	mA
		V_{dd} = 5.5 V, $V_{OUT} = V_{SS}$	-100	-50	-10	mA
V_{IL}	TTL Input Low Voltage				0.8	V
V_{IL}	CMOS Input Low Voltage				0.3 x V_{dd}	V
V_{IH}	TTL Input High Voltage		2.0			V
V_{IH}	CMOS Input High Voltage		0.7 x V_{dd}			V
V_T	TTL Switching Threshold	V_{dd} = 5.0 V, 25°C		1.4		V
	CMOS Switching Threshold	V_{dd} = 5.0 V, 25°C		2.4		V
V_{OL}	Output Low Voltage Output buffer has 12 stages of drive capability with 2 mA I_{OL} per stage.	I_{OL} = as rated V_{dd} = 4.5 V		0.2	0.4	V
V_{OH}	Output High Voltage Output buffer has 12 stages of drive capability with -2 mA I_{OH} per stage.	I_{OH} = as rated V_{dd} = 4.5 V	0.7 x V_{dd}	4.2		V

Note: 2. This is the specification for the 3 x Output Buffer. Output short circuit current for other outputs will scale accordingly. Not more than one output shorted at a time, for a maximum of one second, is allowed.

3.3 Volt DC Characteristics

Applicable over recommended operating range from T_a = -55°C to +125°C, V_{dd} = 3.0 V to 3.6 V (unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
I_{IH}	Input Leakage High	$V_{IN} = V_{dd}$, V_{dd} = 3.6 V		.01	10	µA
I_{IL}	Input Leakage Low (no pull-up)	$V_{IN} = V_{SS}$, V_{dd} = 3.6 V	-10	.01		µA
	40K pull-up	$V_{IN} = V_{SS}$, V_{dd} = 3.6 V	-200	-60	-10	µA
I_{OZ}	Output Leakage (no pull-up)	$V_{IN} = V_{dd}$ or V_{SS}, V_{dd} = 3.6 V	-10	.01	10	µA
I_{OS}	Output Short Circuit Current (3 x Buffer)(2)	V_{dd} = 3.6 V, $V_{OUT} = V_{dd}$	5	25	60	mA
		V_{dd} = 3.6 V, $V_{OUT} = V_{SS}$	-60	-25	-5	mA
V_{IL}	CMOS Input Low Voltage				0.3 x V_{dd}	V
V_{IH}	CMOS Input High Voltage		0.7 x V_{dd}			V
V_T	CMOS Switching Threshold	V_{dd} = 3.3 V, 25°C		1.5		V
V_{OL}	Output Low Voltage Output buffer has 12 stages of drive capability with 1 mA I_{OL} per stage.	I_{OL} = as rated V_{dd} = 3.0 V			0.4	V
V_{OH}	Output High Voltage Output buffer has 12 stages of drive capability with -1 mA I_{OH} per stage.	I_{OH} = as rated V_{dd} = 3.0 V	0.7 x V_{dd}			V

Note: 2. This is the specification for the 3 x Output Buffer. Output short circuit current for other outputs will scale accordingly. Not more than one output shorted at a time, for a maximum of one second, is allowed.

I/O Buffer DC Characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
C_{IN}	Capacitance Input Buffer (Die)	5.0 V, 3.3 V		2.4		pF
C_{OUT}	Capacitance Output Buffer (Die)	5.0 V, 3.3 V		5.6		pF
$C_{I/O}$	Capacitance Bi-Directional	5.0 V, 3.3 V		6.6		pF
Schmitt Trigger						
V+	TTL Positive Threshold	25°C, 5.0 V		1.8	2.0	V
	CMOS Positive Threshold	25°C, 5.0 V		3.2	3.5	V
V-	TTL Negative Threshold	25°C, 5.0 V	0.6	0.8		V
	CMOS Negative Threshold	25°C, 5.0 V	1.0	1.2		V
ΔV	TTL Hysteresis	25°C, 5.0 V	0.4	1.0		
	CMOS Hysteresis	25°C, 5.0 V	1.0	2.0		
V+	CMOS Positive Threshold	25°C, 3.3 V		2.2	2.3	V
V-	CMOS Negative Threshold	25°C, 3.3 V	.65	0.9		V
ΔV	CMOS Hystersis	25°C, 3.3 V	.65	1.3		

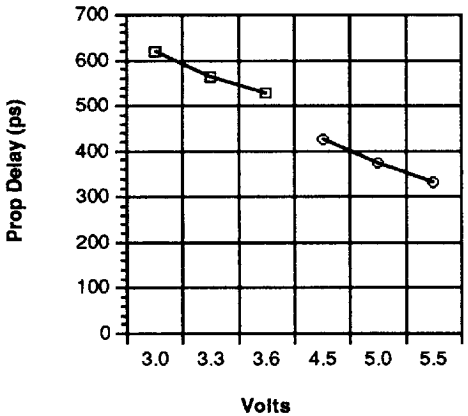
I/O Buffers

- Programmable output drive
  (2 to 24 mA I_{OL}, -2 to -24 mA I_{OH} for 5.0 V
  1 to 12 mA I_{OL}, -1 to -12 mA I_{OH} for 3.3 V)
- 3000 volts ESD protection
- Built-in configurable test logic

The ATL series input/output ring contains the I/O buffer circuitry capable of sourcing and sinking currents up to 24 mA, and responds to CMOS or TTL logic levels. I/O locations on this ring can accommodate bidirectional cells.

AC Characteristics

Delay vs V_{dd}

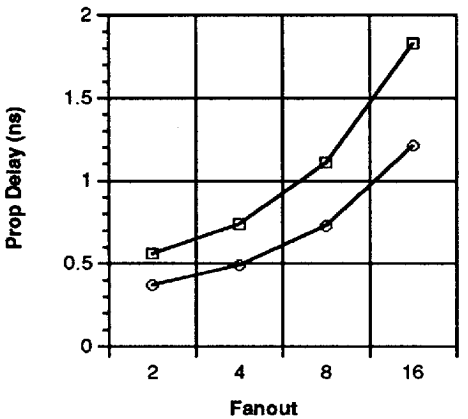


3.3 Volts V_{dd}

5.0 Volts V_{dd}

NAND2 - 2 input NAND
Temp = 25°C
FO = 2

Delay vs Fanout

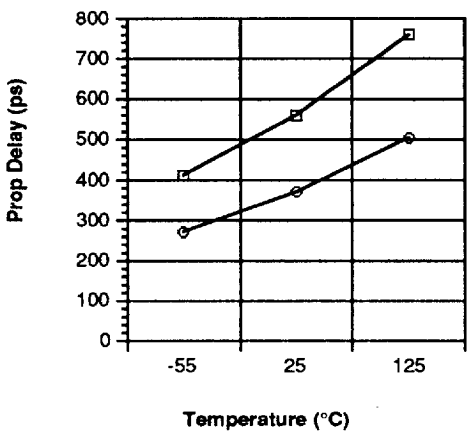


3.3 Volts V_{dd}

5.0 Volts V_{dd}

NAND2 - 2 input NAND
Temp = 25°C

Delay vs Temperature

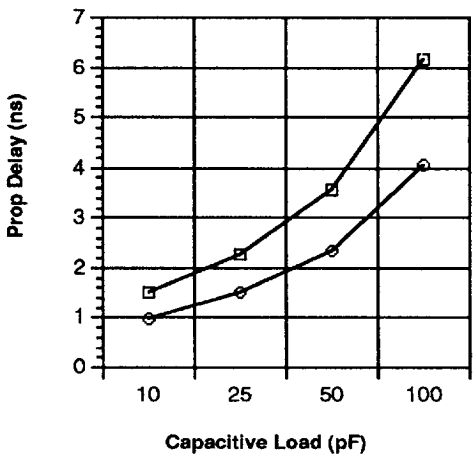


3.3 Volts V_{dd}

5.0 Volts V_{dd}

NAND2 - 2 input NAND
FO = 2

Output Buffer vs Load



3.3 Volts V_{dd}

5.0 Volts V_{dd}

PDO4 - Output Buffer 8 mA
Temp = 25°C

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Design for Testability

Atmel supports a full range of Design-for-Test improvement techniques which reduce design and prototype debug time, production test time, and board & system test time. These techniques can also improve system level test and diagnostic capability.

The ATL arrays support the Joint Test Action Group (JTAG) boundary scan architecture. The required soft and hard macros to implement IEEE 1149.1 compliant architecture are available in our macro cell library. Use of JTAG allows for scan testing with only 4-5 additional pins required.

Atmel can also provide automatic high fault coverage test pattern generation (ATPG) via Synopsys Test Compiler. By following a set of design rules, Test Compiler can automatically insert the scan cells and generate test vectors providing greater than 95% fault coverage. This is the easiest and least expensive method for designing testability into a gate array design.

Advanced Packaging

Atmel supports a wide variety of standard packages for the ATL series, but also offers its ATL series gate arrays in packages that are custom designed to maintain the performance obtained in the silicon.

All of Atmel's standard packages have been characterized for thermal and electrical performance. When a standard package can't meet a customer's needs, Atmel's package design center can develop a package to precisely fit the application. The company has delivered custom-designed packages in a wide variety of configurations, including multichip modules and Tape Automated Bonding (TAB) packages. Atmel's domestic packaging facility manufactures commercial, industrial, Class B and modified Class S level product.

Packaging Options

Package Type	Pin Count
TQFP	44, 48, 64, 80, 100, 144, 160, 208, 240, 248, 304
PQFP	44, 64, 68, 80, 100, 120, 128, 132, 136, 144, 160, 184, 208, 232, 256, 304
PLCC	28, 44, 68, 84
PPGA	68, 84, 100, 120, 132, 144, 180, 224
CPGA	64, 68, 84, 100, 124, 144, 155, 180, 223, 224, 256, 299, 391
CQFP	64, 68, 84, 132, 160, 224, 340
CLCC	44, 52, 84, 132, 148, 196
TAB	68, 100, 120, 128, 144, 160, 180, 208, 224, 256, 292, 304, 338, 360

Military Product Flow Chart

MIL-STD-883 Class B