T-50-17

GBL GigaBit Logic

16G041-H

Low Power, PLL Clock & Data Recovery Circuit 100 to 625 Mbit/s NRZ Data Rate

FEATURES

- Low power (1.25W typ.) clock recovery and data retiming and regeneration subsystem - no external components required
- Small, 1.25" x 1.25" surface mount package
- 0°C to 70°C operating temperature range
- Patented, self-acquiring PLL GaAs IC design
- Available in standard frequencies: 100, 155.52, 250, 565, and 622.08 Mbit/s. Custom frequencies available upon request.
- PLL design tracks input data frequency drift, generates a clock output even in the absence of incoming data and provides immunity to component aging and temperature effects
- Retains lock for long constant data run lengths
- Automatically reclocks data precisely in the center of each bit time providing maximum timing margin and low bit error rate
- Easy interface to 10G041A Time Division Demux

FUNCTIONAL DESCRIPTION

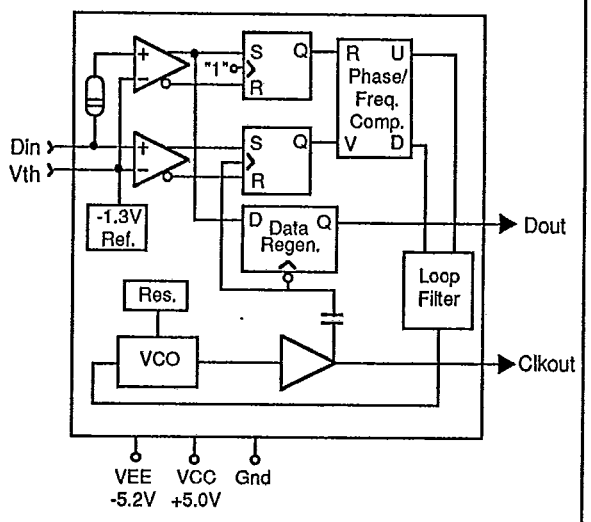
The 16G041-H is a complete phase locked loop clock recovery and data retiming / regeneration subsystem for applications requiring high data rates, low power and small size. The 16G041-H integrates GigaBit's 16G041 PLL clock and data recovery GaAs IC together with a high performance loop filter and other components to realize a complete, 3-terminal (data in, clock and data out) PLL clock recovery subsystem. No external components are required. The operating center frequency is factory set to the following standard frequencies: 100, 155.52 (SONET OC-3), 250, 565, and 622.08 Mbit/s (SONET OC-12). (Special orders for custom frequencies between 100 to 625 Mbit/s are also available. Consult with factory.) Devices are then hermetically sealed and tested prior to delivery. Frequency adjustment is made to fully assembled and tested circuits, as needed.

Unlike SAW filter clock recovery circuits which filter the clock signal from incoming data, the 16G041-H is capable of synchronizing an internal VCO directly to an incoming digital data steam, while simultaneously retiming and regenerating the data stream. In addition, the on-chip VCO will generate

APPLICATION

- High speed fiber optic and microwave receivers and repeaters and fiber comms. test equipment

16G041-H BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Description	Notes
16G041-HDxxx.x 16G041-HAxxx.x	DC-coupled input AC-coupled input	Available standard center frequencies are 100, 155.52, 250, 565, 622.08 Mbit/s. Custom frequencies between 100 to 625 Mbit/s are available with a minimum order and a NRE. Consult with your neareast sales office for more information.
Note: xxx.x denotes device center frequency.		

T-50-17

GigaBit Logic **16G041-H**

FUNCTIONAL DESCRIPTION (CONT.)

a clock output even in the absence of incoming data. This might be critical if the recovered clock drives a state machine or any other logic circuitry that might go into a metastable state in the absence of a clock. The 16G041-H is capable of unaided frequency acquisition, eliminating the need for special circuits to "pull" the loop into lock when the incoming data rate differs from the initial VCO (clock) rate.

Compared with SAW-based recovery/retiming circuits, the 16G041-H offers numerous design advantages, including: tracking out of component aging and temperature effects, elimination of phase margin and timing problems due to temperature and data pattern variation, tolerance to wide variation in input data frequency, retention of lock under conditions of long strings of constant data, easy and inexpensive tunability to a new center frequency, and easier customization for the specific acquisition time and stability requirements of different applications.

ABSOLUTE MAXIMUM RATINGS

(Beyond which useful life may be impaired) (Note 1)

SYMBOL	PARAMETER	ABSOLUTE MAXIMUM RATINGS	NOTES
TSTOR	Storage Temperature	-65 °C to +150 °C	
TJ	Junction Temperature	-55 °C to +150 °C	
TC	Case Temperature Under Bias	-55 °C to +125 °C	2
VCC	Supply Voltage	+1.0 V to +7.0 V	
VEE	Supply Voltage	-7.0 V to -2.9 V	
VIN	Voltage Applied to Any Input; Continuous VCC = 5.0V, VEE = -5.2 V	-4.0 V to +0.5 V	
I IN	Current Into Any Input; Continuous	-0.5 mA to 1.0 mA	
VOUT	Voltage Applied to Any Output	-4.0V to +7.0 V	3
IOUT	Current From Any Output; Continuous	-100 mA	
VTT	Load Termination Supply	-6.0 V to +6.0 V	

Notes:
1. Positive current is defined as current into the device.
2. TC is measured at case bottom.
3. Subject to IOUT and power dissipation limitations.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	NOM	MAX	UNITS	NOTES
TC	Case Operating Temperature	0	25	70	°C	1
VCC	Supply Voltage	4.75	5.0	5.25	V	
VEE	Supply Voltage	-5.5	-5.2	-5.1	V	
VTT	Load Termination Voltage	-5.2	-2.0	-2.0	V	2
RLOAD	Output Termination Load Resistance	25	50	100	Ω	2

Notes:
1. Tcase measured at case bottom.
2. The RLOAD and VTT combination used is subject to maximum output current and power restrictions.

T-50-17

GigaBit Logic

16G041-H

DC CHARACTERISTICS (Notes 1,2)

Tc = 0°C to 70 °C, VCC =4.75V to 5.25V, VEE = -5.5V to -5.1V, unless otherwise indicated.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS	NOTES
VOH	Output Voltage High	- 0.8	-0.5	-0.3	V		
VOL	Output Voltage Low	VTT	-1.9	- 1.7	V		
IOH	Output Current High		-70	-60	mA	VOH = -0.8V	3
VIH	Input Voltage High	- 1.0		Gnd	V		
VIL	Input Voltage Low	VTT		- 1.6	V		
Vth	Input threshold level	-1.6	-1.3	-1.0	V		
IIND	Input Current (16G041-HD)	8		20	mA	VIN = -1.0V to -1.6V	4
IINA	Input Current (16G041-HA)		0		mA		5
ICC	Power Supply Current		30	40	mA		
IEE	Power Supply Current		210	290	mA		
PD	Power Dissipation		1.25	1.7	W		6

Notes:
1. These characteristics are applicable from DC to 300 MHz.
2. Test conditions (unless otherwise indicated): Vth = -1.3V, VTT = -2.0V, RLOAD = 50Ω to -2.0V.
3. IOH is the available output current at VOH = -0.8V.
4. Input current for DC coupled input. Current is drawn through an internal 50Ω termination to VTT.
5. No current since input is AC coupled with user provided DC blocking capacitor. Input is internally terminated to -1.3 V via a 50Ω termination resistor.
6. At nominal supply voltages and 50% duty cycle. Exclusive of output power (typically15 mW per output).

AC CHARACTERISTICS (Notes 1,2)

Tc = 0°C to 70 °C, VCC =4.75V to 5.25V, VEE = -5.5V to -5.1V, unless otherwise indicated.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS	NOTES
fco	VCO center freq.	100		625	MHz		3
fdo	Center NRZ input data rate	100		625	Mb/s		3
fc	Loop capture range		±5		MHz	fo=565 MHz; 2exp15 -1 PRBS	4,5
fcm	Loop capture range@ 0° & 70°C	±0.1			% of fco	2exp15 -1 PRBS	4,5
Δfv	VCO drift over temperature	-125	-100		KHz/C		
tacq	Loop acquisition time		250		µs	fo=565 MHz; 2exp15 -1 PRBS	
Δtj	Clock to Data output RMS jitter in lock		50	75	ps	fo=565 MHz; 2exp15 -1 PRBS	4
n	Max. run length of consecutive 1s\or 0s before loss of lock	23			bits	fo=600 MHz; 2exp23 -1 PRBS; 50% transition density	
D	Input data transition density to maintain lock	0.20				One "1" followed by nine "0s"	
tod	Clock output falling edge to data transition output delay	400	600	800	ps	2exp15 -1 PRBS	
DC	Clock output duty cycle	40		60	%	2exp15 -1 PRBS	
tr, tf	Output rise and fall times		125	200	ps		

Notes:
1. Input signal level is 600 mVp-p centered at Vth = -1.3V.
2. Rload = 50Ω to Vtt = -2.0V.
3. Factory set frequency.
4. No bit error measured during testing time: 1 second; equivalent measurement resolution @ 565 Mb/s is $1.77\ 10^{-9}$ BER.
5. Defined with an initial condition of no incoming data.

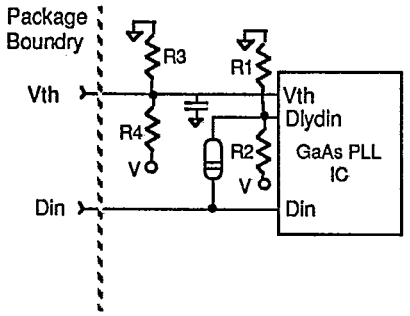
T-50-17

GigaBit Logic 16G041-H

INPUT CIRCUIT DESCRIPTION

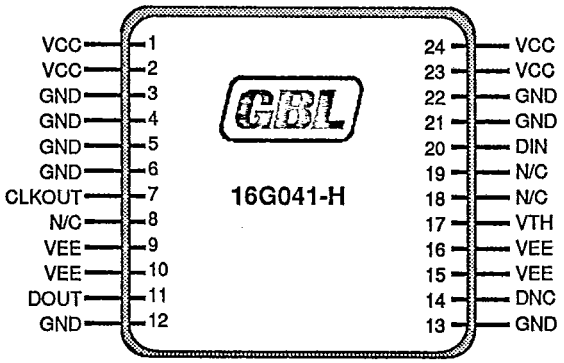
The 16G041-H is available with either AC (part no. 16G041-HA) or DC (part no. 16G041-HD) coupled data inputs. In the 16G041-HA, R1 and R2 form a 50Ω thevenin equivalent to -1.3V input. In the 16G041-HD, these resistors form a 50Ω to -2.0V thevenin equivalent.

Vth is used to set the decision level of the input comparators, and is therefore biased internally to -1.3V via the R3 and R4 thevenin equivalent input. In some applications, it may be useful to adjust the decision threshold of the input comparators. This is possible since R3 and R4 are chosen to present a ≥1KΩ input resistance, allowing the user to over-ride the internally set -1.3V bias via an externally applied voltage to the Vth pin.



PIN FUNCTIONS

TOP VIEW (LID SIDE)



PIN DESCRIPTIONS

DIN	Serial Data Input	GND	Ground
CLKOUT	Recovered Clock Output	VTH	Threshold bias control to the input comparators
DOUT	Recovered Data Output	N/C	No Connection
VCC	+5V supply	DNC	DO NOT CONNECT
VEE	-5.2V supply		

T-90-20

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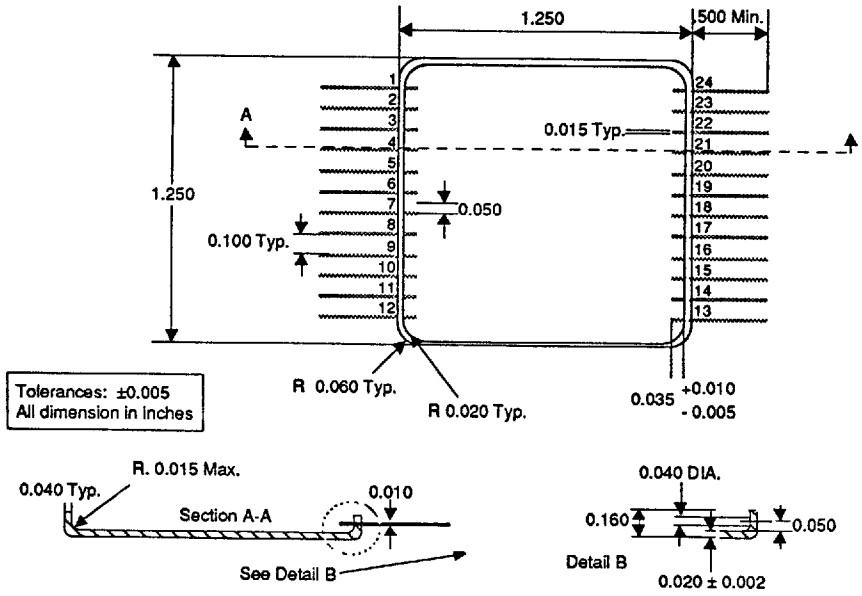
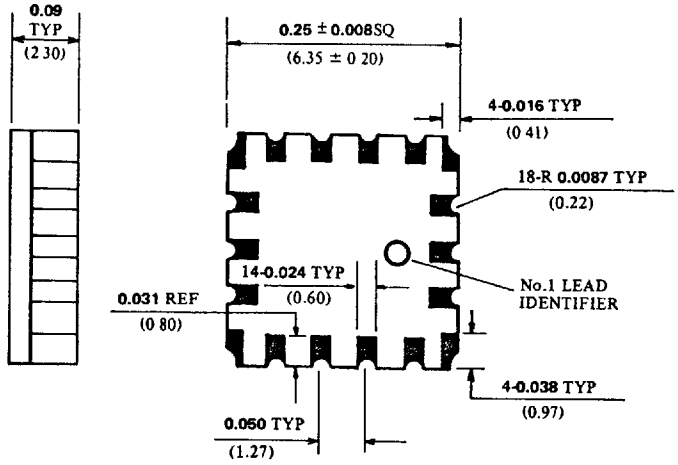
24 PIN METAL FLATPACK
18 PIN PACKAGE

24 PIN METAL FLATPACK
Type H



18 PIN LEADLESS CHIP CARRIER
TYPE L1



All dimensions shown in inches and (millimeters)

11

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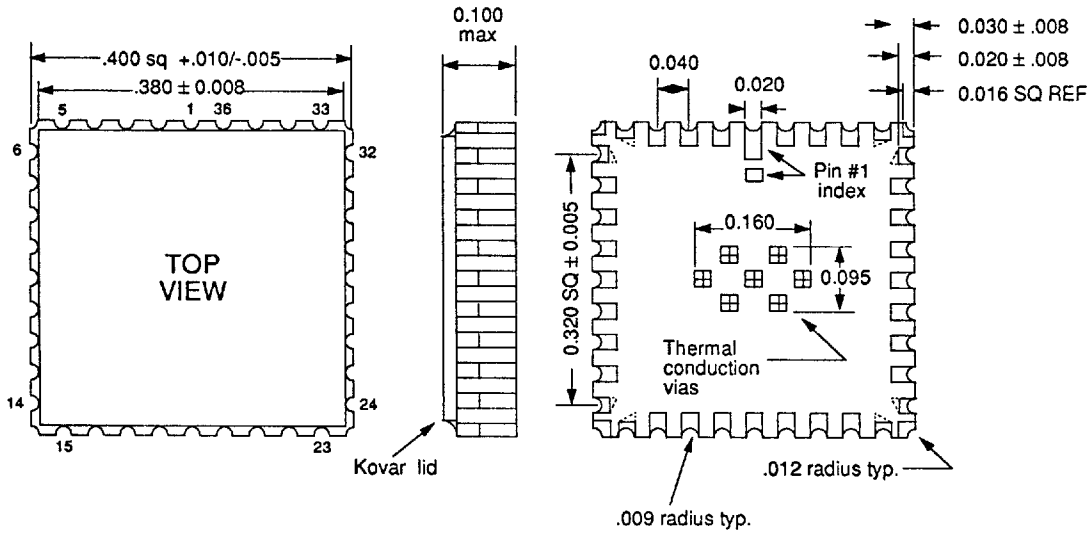
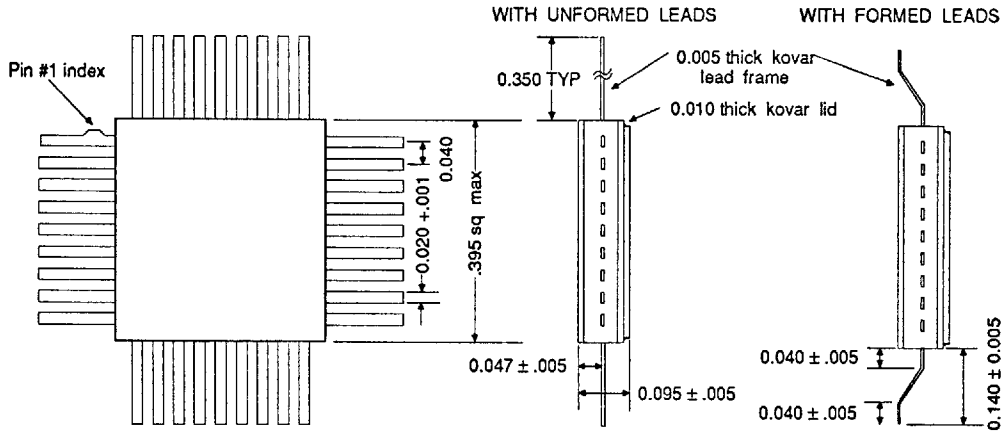
36 PIN PACKAGES

36 PIN LEADLESS CHIP CARRIER
TYPE L36



NOTES:
1) The package bottom thermal vias, top lid surface and 4 metallized corner castellations (when present) are all at Vss potential.
2) All dimensions in inches.
3) Plin #1 identifier may be an elongated pad or small, square gray marker.

36 I/O LEAD FLATPACK
TYPE F



T-90-20

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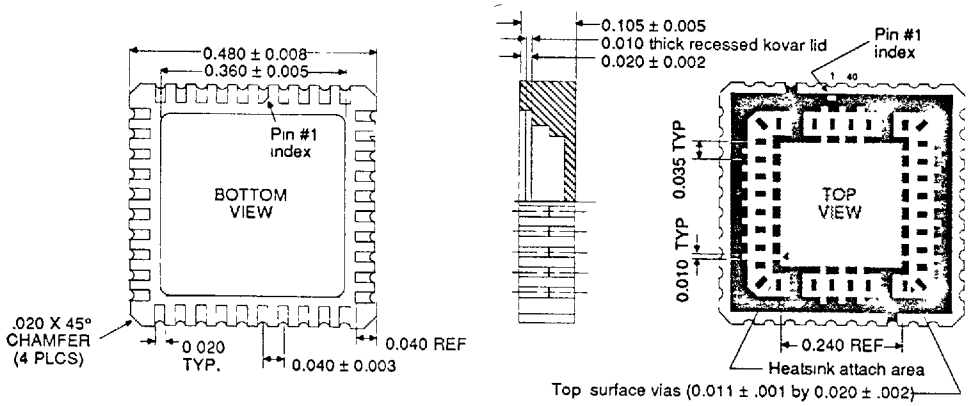
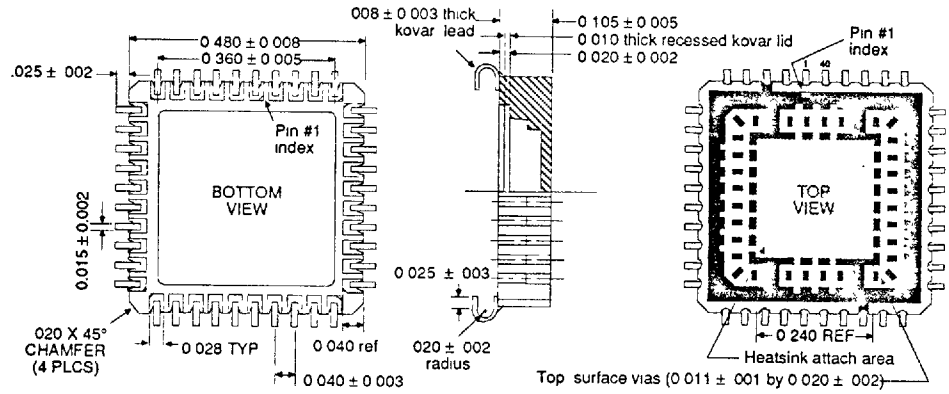
40 PIN PACKAGES

40 PIN LEADLESS CHIP CARRIER
TYPE L

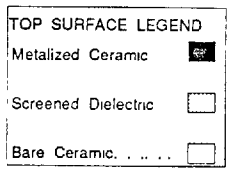


40 PIN LEADED CHIP CARRIER
TYPE C

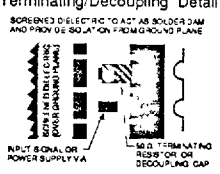


NOTES

(1) Footprint is JEDEC standard outline
(2) Top surface v as (for terminating resistors and decoupling capacitors) are not available on pins 3 4 17 18 23 24 37 and 38
(3) Top surface metal (not including vias) and p ns 3 and 23 are fixed at VTT potential
(4) Recommended top surface chip res stors are 0 040 long by 0 020 w de by 0 010 thick typ 100 mw min nominal power rating (M ni-Systems MSR 21 or equivalent)
(5) Recommended top surface ch p capac tors are 0 040 ong by 0 030 wide by 0 020 thick typ 25V VDCW 1000 pf min (Johanson R09 case or equivalent)
(6) Recommended heatsinks a e GBL P/Ns 90GHS 40 A and 90GHS 40 B
(7) Thermally conductive, e ectrically non-conductive epoxy is recommended for heatsink attachment (Ablestick 789 4 or 561K, or Thermalloy Thermalbond™ or equivalent.)
(8) L40 and C40 packages are dimensionally identical except for contact finger width



Top Surface Terminating/Decoupling Detail



T-90-20

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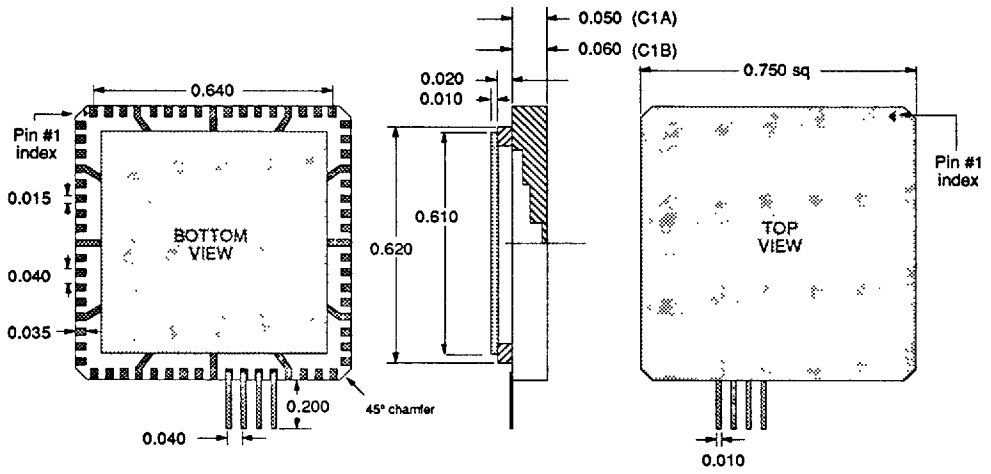
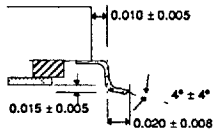
68 & 132 PIN PACKAGES

68 PIN LEADED CHIP CARRIER
TYPE C1



1. All dimensions in inches.
2. C1A PACKAGE: Package lid, top, and pins 4, 9, 14, 21, 26, 31, 38, 43, 48, 55, 60, 65 are at common potential (system ground).
3. C1B PACKAGE: Package lid and pins 4, 9, 14, 21, 26, 31, 38, 43, 48, 55, 60, 65 are at common potential (system ground).
4. Tolerance on all dimensions is ± 1 % but not larger than ± 0.005. Tolerance on 0.640 end pad to end pad dimension is ± 0.003.

GULLWING LEADS



132 PIN LEADED CHIP CARRIER
TYPE C3