SIEMENS

SIEMENS AKTIENGESELLSCHAF

T-46-23-18

1M x 9-Bit Dynamic RAM Module

HYM 91000S/L-60/-70/-80
HYM 9100SL/LL-60/-70

Advanced Information

- 1 048 576 words by 9-bit organization
- Fast access and cycle time
  60 ns access time
  110 ns cycle time (-60 version)
  70 ns access time
  130 ns cycle time (-70 version)
  80 ns access time
  150 ns cycle time (-80 version)
- Fast page mode capability with
  40 ns cycle time (-60/-70 version)
  45 ns cycle time (-80 version)
- Single + 5 V (± 10 %) supply
- Low power dissipation
  max. 4455 mW active (-60 version)
  max. 4000 mW active (-70 version)
  max. 3500 mW active (-80 version)
  CMOS – 50 mW standby
  TTL – 100 mW standby
  15 mW under battery back up condition (HYM 91000SL/LL)
- Common $\overline{CAS}$ control for eight common data-in and data-out lines
- Separate $\overline{CAS}$ control for ninth bit
- $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, hidden-refresh
- Decoupling capacitors mounted on substrate
- All inputs, outputs and clocks fully TTL compatible
- Single In-Line Memory Module socket (HYM 91000S/SL) and lead (HYM 91000L/LL) version
- Pin configuration according to JEDEC standards
- Utilizes nine 1M-DRAMs in SOJ package
- 512 refresh cycles/8 ms (HYM 91000S/L)
- 512 refresh cycles/64 ms (HYM 91000SL/LL)

The HYM 91000S/L-60/-70/-80 is a 1 Mbyte RAM module organized as 1 048 576 words by 9-bit in a 30-pin single-in-line package comprising in HYB 511000J 1M x 1 DRAMs in SOJ-packages mounted together with nine 0.2 µF multilayer ceramic decoupling capacitors on a PC board.

The HYM 91000SL/LL-60/-70/-80 is the low power version comprising nine HYB 511000JL 1M x 1 low power DRAMs specially selected for battery backup applications.

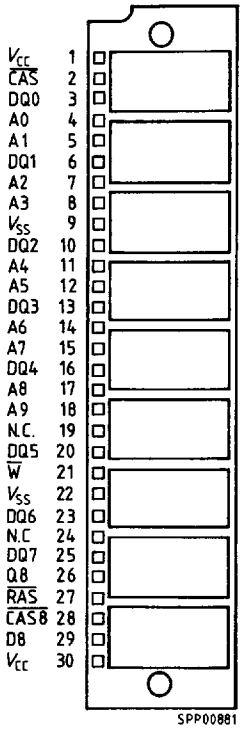
Each HYB 51000J/JL is described in the data sheet and is fully electrically tested and processed according to Siemens standard quality procedure prior to module assembly. After assembly onto the board, a further set of electrical tests is performed.

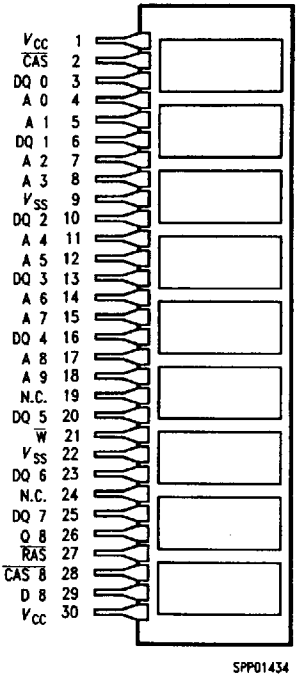
A common $\overline{CAS}$ controls for eight common data-in and data-out lines. Bit nine (D8, Q8) which is generally used for parity is controlled by $\overline{CAS8}$. The common I/O feature on the HYM 91500S/SL/L/LL-60/-70/-80 dictates the use of early write cycles to prevent contention on D and Q.

Ordering Information

Type	Ordering Code	Package	Descriptions
HYM 91000S-60	Q67100-Q470	L-SIM-30-800-1	DRAM Module (access time 60 ns) [1]
HYM 91000S-70	Q67100-Q445	L-SIM-30-800-1	DRAM Module (access time 70 ns) [1]
HYM 91000S-80	Q67100-Q396	L-SIM-30-800-1	DRAM Module (access time 80 ns) [1]
HYM 91000L-60	Q67100-Q564	L-SIM-30-800-1	DRAM Module (access time 60 ns) [1]
HYM 91000L-70	Q67100-Q497	L-SIM-30-800-2	DRAM Module (access time 70 ns) [2]
HYM 91000L-80	Q67100-Q448	L-SIM-30-800-2	DRAM Module (access time 80 ns) [2]
HYM 91000SL-60	Q67100-Q569	L-SIM-30-800-1	DRAM Module (access time 60 ns) Low Power [1]
HYM 91000SL-70	Q67100-Q571	L-SIM-30-800-1	DRAM Module (access time 70 ns) Low Power [1]
HYM 91000LL-60	Q67100-Q570	L-SIM-30-800-2	DRAM Module (access time 60 ns) Low Power [2]
HYM 91000LL-70	Q67100-Q572	L-SIM-30-800-2	DRAM Module (access time 70 ns) Low Power [2]

[1] Socket type
[2] Pin type





HYM 91000S/SL
(Socket Type)

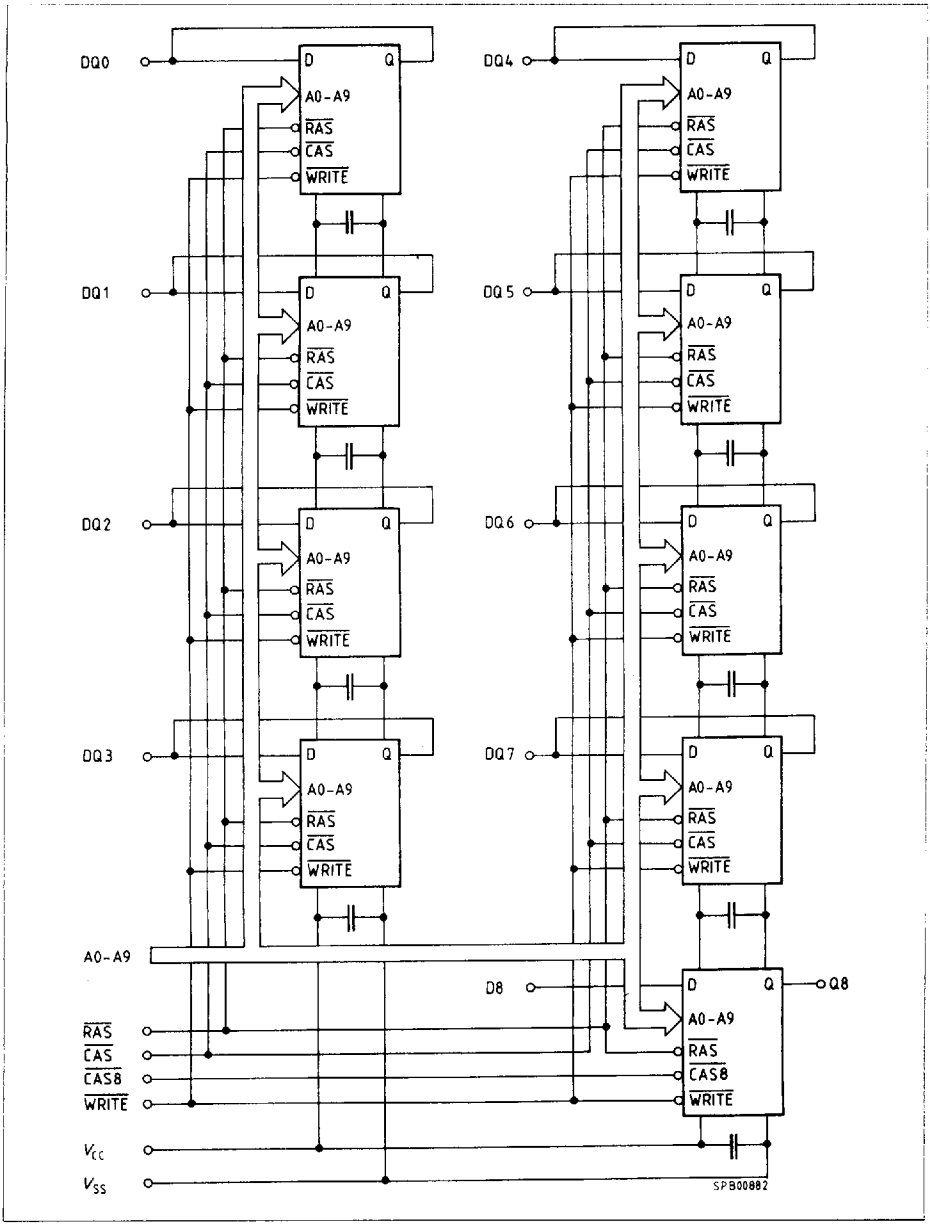
HYM 91000L/LL
(Pin type)

Pin Names

A0-A9	Address Inputs
DQ0-DQ7	Data Input/Output
D8	Data Input
Q8	Data Output
$\overline{CAS}$	Column Address Strobe
$\overline{RAS}$	Row Address Strobe

$\overline{WRITE}$	Read/Write Input
$\overline{CAS8}$	Column Address Strobe
V_{CC}	Power Supply (+ 5 V)
V_{SS}	Ground (0 V)
N.C.	No Connection

Pin Configuration



Block Diagram

Absolute Maximum Ratings

Operating temperature range ..... 0 to + 70 °C
Storage temperature range ..... – 55 to + 125 °C
Soldering temperature ..... 260 °C
Soldering time ..... 10 s
Input/output voltage ..... – 1 to + 7 V
Power supply voltage ..... – 1 to + 7 V
Power dissipation ..... 5.4 W
Data out current (short circuit) ..... 50 mA

Note: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

DC Characteristics

T_A = 0 to 70 °C; V_{CC} = 5 V ± 10 %

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input high voltage	V_{IH}	2.4	6.5	V	–
Input low voltage	V_{IL}	– 1.0	0.8	V	–
Output high voltage (I_{OUT} = – 5 mA)	V_{OH}	2.4	–	V	–
Output low voltage (I_{OUT} = 4.2 mA)	V_{OL}	–	0.4	V	–
Input leakage current (0 V ≤ V_{IN} ≤ 6.5 V, all other pins = 0 V)	$I_{I(L)}$	– 20	20	µA	–
Output leakage current (DO is disabled, 0 V ≤ V_{OUT} ≤ 5.5 V)	$I_{O(L)}$	– 20	20	µA	–
Average V_{CC} supply current:	I_{CC1}				
HYM 91000**-60		–	810	mA	1) 2) 3)
HYM 91000**-70		–	720	mA	1) 2) 3)
HYM 91000**-80		–	630	mA	1) 2) 3)
($\overline{RAS}$, $\overline{CAS}$, address cycling, t_{RC} = t_{RC} min.)					
Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	–	18	mA	1)
Average V_{CC} supply current, during	I_{CC3}				
$\overline{RAS}$ only refresh cycles: HYM 91000**-60		–	810	mA	1) 2) 3)
HYM 91000**-70		–	720	mA	1) 2) 3)
HYM 91000**-80		–	630	mA	1) 2) 3)
($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = t_{RC} min.)					

Notes see page 152.

DC Characteristics (cont'd)
T_A = 0 to 70 °C; V_{CC} = 5 V ± 10 %

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Average V_{CC} supply current, during fast page mode: HYM 91000**-60	I_{CC4}	–	630	mA	1) 2) 3)
HYM 91000**-70		–	540	mA	1) 2) 3)
HYM 91000**-80		–	450	mA	1) 2) 3)
($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, address cycling, t_{PC} = t_{PC} min.)					
Standby V_{CC} supply current: ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2 V)	I_{CC5}	–	9	mA	–
Average V_{CC} supply current, during $\overline{CAS}$-before-$\overline{RAS}$ mode:	I_{CC6}	–			
HYM 91000**-60		–	810	mA	1)
HYM 91000**-70		–	720	mA	1)
HYM 91000**-80			630	mA	1)
($\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC} = t_{RC} min.)					

for HYM 91000SL/LL only:

Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	–	1.8	mA	1)
Battery backup current average power supply current battery backup mode: ($\overline{CAS}$ = $\overline{CAS}$ before $\overline{RAS}$ cycling or 2.0 V, $\overline{WRITE}$ = V_{CC} – 0.2 V or 0.2 V, A0 to A9 = V_{CC} – 0.2 V or 0.2 V DI = V_{CC} – 0.2 V or 0.2 V or open, t_{RC} = 125 µs, t_{RAS} = t_{RAS} min. ~ 1 µs	I_{CC7}	–	2.7	mA	2) 13)

Notes see page 152.

AC Characteristics [4) 5)]

T_A = 0 to 70 °C; V_{CC} = 5 V ± 10 %; t_T = 5 ns

Parameter	Symbol	Limit Values						Unit
		HYM 91000**-60		HYM 91000**-70		HYM 91000**-80		
		min.	max.	min.	max.	min.	max.	
Random read or write cycle time	t_{RC}	110	–	130	–	150	–	ns
Fast page mode cycle time	t_{PC}	40	–	40	–	45	–	ns
Access time from $\overline{RAS}$ [6) 11)]	t_{RAC}	–	60	–	70	–	80	ns
Access time from $\overline{CAS}$ [6) 11)]	t_{CAC}	–	20	–	20	–	20	ns
Access time from column address [6) 12)]	t_{AA}	–	30	–	35	–	40	ns
Access time from $\overline{CAS}$ precharge [6)]	t_{CPA}	–	30	–	35	–	40	ns
$\overline{CAS}$ to output in low-Z [6)]	t_{CLZ}	0	–	0	–	0	–	ns
Output buffer turn-off delay [7)]	t_{OFF}	0	20	0	20	0	20	ns
Transition time (rise and fall) [7)]	t_T	3	50	3	50	3	50	ns
$\overline{RAS}$ precharge time	t_{RP}	40	–	50	–	60	–	ns
$\overline{RAS}$ pulse width	t_{RAS}	60	10.000	70	10.000	80	10.000	ns
$\overline{RAS}$ pulse width (fast page mode)	t_{RASP}	60	100.000	70	100.000	80	100.000	ns
$\overline{RAS}$ hold time	t_{RSH}	20	–	20	–	20	–	ns
$\overline{CAS}$ hold time	t_{CSH}	60	–	70	–	80	–	ns
$\overline{CAS}$ pulse width	t_{CAS}	20	10.000	20	10.000	20	10.000	ns
$\overline{RAS}$ to $\overline{CAS}$ delay time [11)]	t_{RCD}	20	40	20	50	20	60	
$\overline{RAS}$ to column address delay time [12)]	t_{RAD}	15	30	15	35	15	40	ns
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5	–	5	–	5	–	ns

Notes see page 152.

AC Characteristics (cont'd) [4) 5)]

T_A = 0 to 70 °C; V_{CC} = 5 V ± 10 %; t_T = 5 ns

Parameter	Symbol	Limit Values						Unit
		HYM 91000**-60		HYM 91000**-70		HYM 91000**-80		
		min.	max.	min.	max.	min.	max.	
$\overline{CAS}$ precharge time (fast page mode)	t_{CP}	10	–	10	–	10	–	ns
Row address setup time	t_{ASR}	0	–	0	–	0	–	ns
Row address hold time	t_{RAH}	10	–	10	–	10	–	ns
Column address setup time	t_{ASC}	0	–	0	–	0	–	ns
Column address hold time	t_{CAH}	15	–	15	–	15	–	ns
Column address hold time referenced to $\overline{RAS}$	t_{AR}	50	–	55	–	60	–	ns
Column address to $\overline{RAS}$ lead time	t_{RAL}	30	–	35	–	40	–	ns
Read command setup time	t_{RCS}	0	–	0	–	0	–	ns
Read command hold time [8)]	t_{RCH}	0	–	0	–	0	–	ns
Read command hold time referenced to $\overline{RAS}$ [8)]	t_{RRH}	0	–	0	–	0	–	ns
Write command hold time	t_{WCH}	15	–	15	–	15	–	ns
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	50	–	55	–	60	–	ns
Write command pulse width	t_{WP}	15	–	15	–	15	–	ns
Write command to $\overline{RAS}$ lead time	t_{RWL}	20	–	20	–	20	–	ns
Write command to $\overline{CAS}$ lead time	t_{CWL}	20	–	20	–	20	–	ns
Data setup time [9)]	t_{DS}	0	–	0	–	0	–	ns
Data hold time [9)]	t_{DH}	15	–	15	–	15	–	ns
Data hold time referenced to $\overline{RAS}$	t_{DHR}	50	–	55	–	60	–	ns

Notes see page 152.

AC Characteristics (cont'd) [4) 5)]

T_A = 0 to 70 °C; V_{CC} = 5 V ± 10 %; t_T = 5 ns

Parameter	Symbol	Limit Values						Unit
		HYM 91000**-60		HYM 91000**-70		HYM 91000**-80		
		min.	max.	min.	max.	min.	max.	
Refresh period HYM 91000 S/L	t_{REF}	–	8	–	8	–	8	ms
Refresh period HYM 91000 SL/LL	t_{REF}	–	64	–	64	–	64	ms
Write command setup time [10)]	t_{WCS}	0	–	0	–	0	–	ns
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	t_{CSR}	10	–	10	–	10	–	ns
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	t_{CHR}	30	–	30	–	30	–	ns
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	0	–	0	–	0	–	ns
$\overline{CAS}$ precharge time ($\overline{CAS}$-before-$\overline{RAS}$ counter test cycle)	t_{CPT}	40	–	40	–	40	–	ns
$\overline{CAS}$ precharge time	t_{CPN}	10	–	10	–	10	–	ns

Notes see page 152.

Capacitance

T_A = 0 to 70 °C; V_{CC} = 5 V ± 10 %; f = 1 MHz

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input capacitance (A0 to A9, $\overline{RAS}$, $\overline{WE}$, $\overline{CAS}$)	C_{I1}	–	60	pF
Input capacitance (D8, $\overline{CAS8}$)	C_{I2}	–	10	pF
I/O capacitance (D0 to D8)	C_{IO}	–	15	pF
Output capacitance (Q8)	C_O	–	10	pF

Notes for pages 147 to 151:

1) All voltages are referenced to V_{SS}.

2) I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.

3) I_{CC1} and I_{CC4} depend on output loading. Specified values are measured with the output open.

4) An initial pause of 200 µs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles is required.

5) V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Transition times are also measured between V_{IH} and V_{IL}.

6) Measured with a load equivalent to 2 TTL loads and 100 pF.

7) t_{OFF} (max.) defines the time at which the output achieves the open-circuit conditions and is not referenced to output voltage levels.

8) Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

9) These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{WRITE}$ leading edge in read-write cycles.

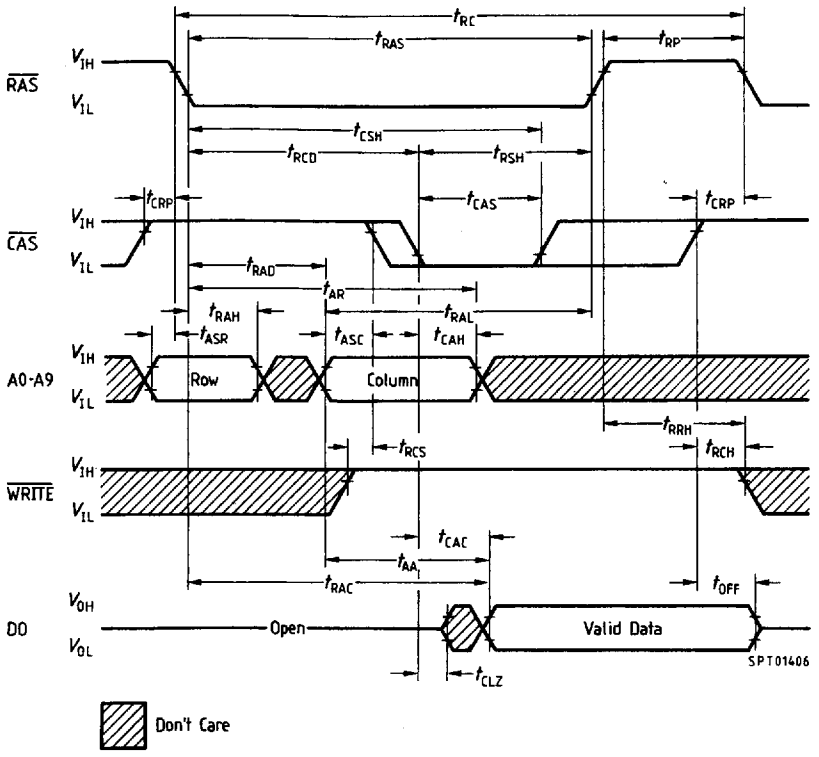
10) t_{WCS} is not a restrictive operating parameter. This is included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance).

11) Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.

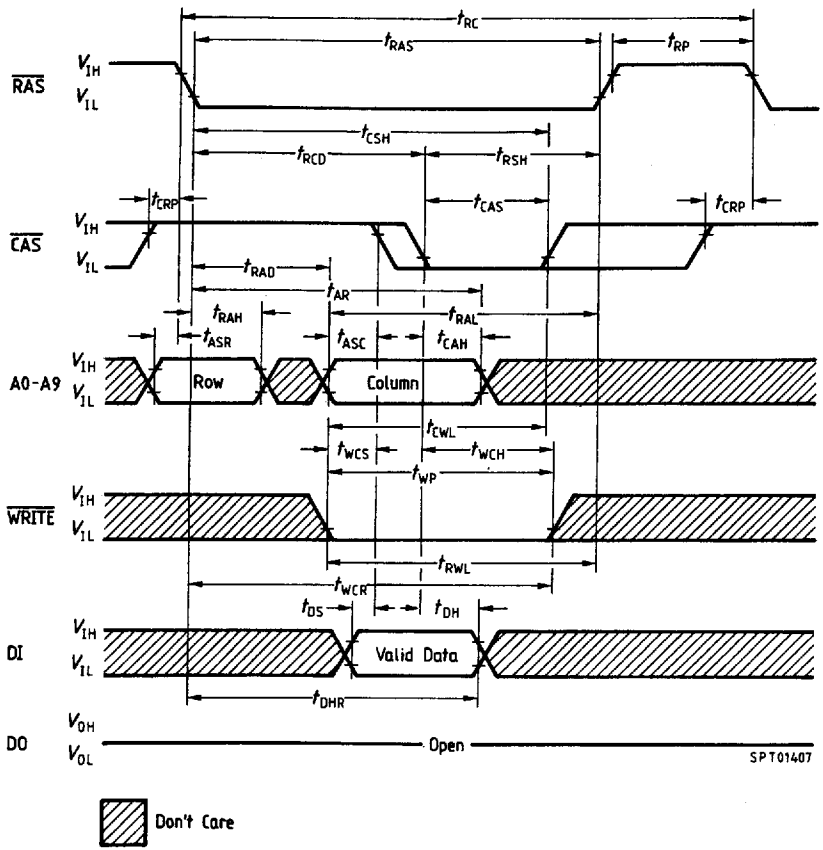
12) Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

13) t_{RAS} (max.) = 1 µs is only applied to refresh of battery-backup.
t_{RAS} (max.) = 10 µs is applied to functional operating.

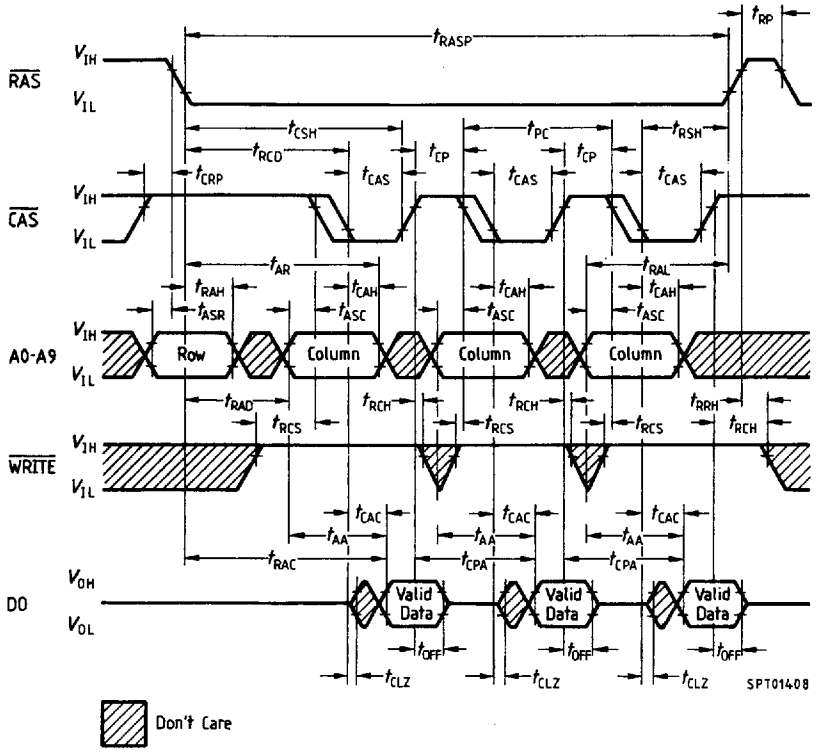
Waveforms



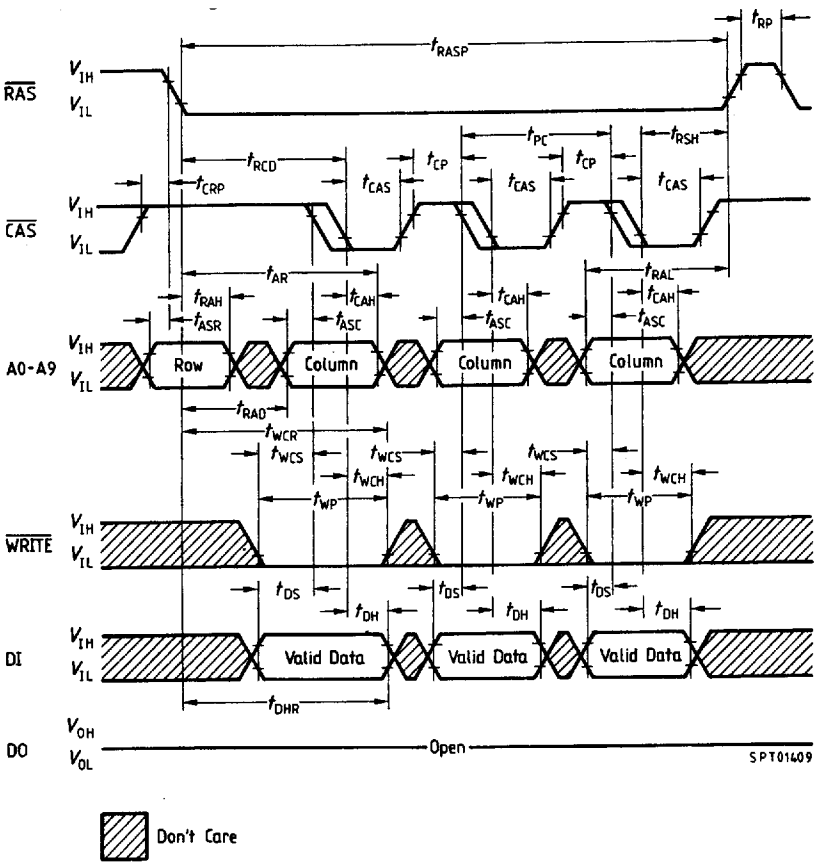
Read Cycle



Write Cycle (Early Write)



Fast Page Mode Read Cycle



Fast Page Mode Write Cycle (Early Write)

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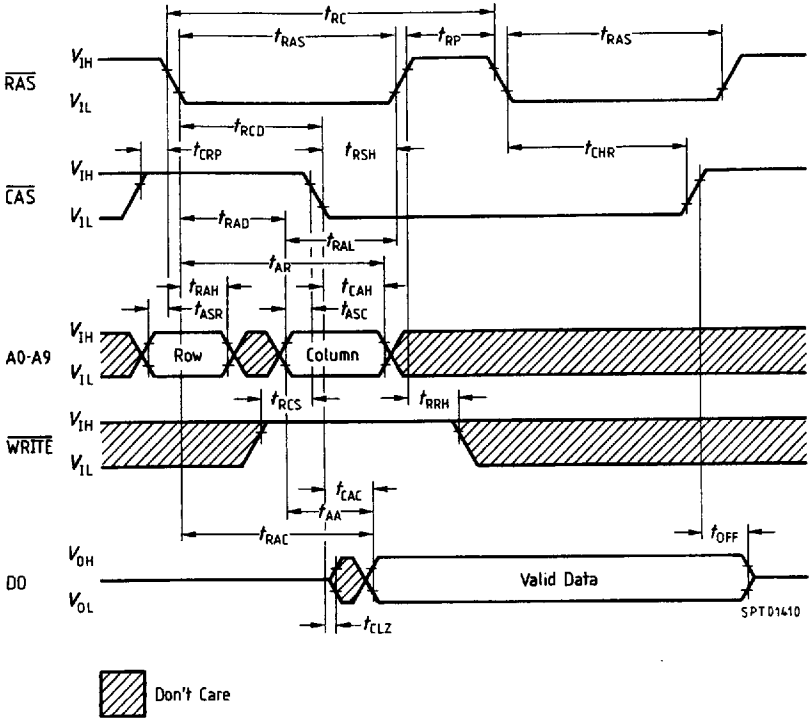
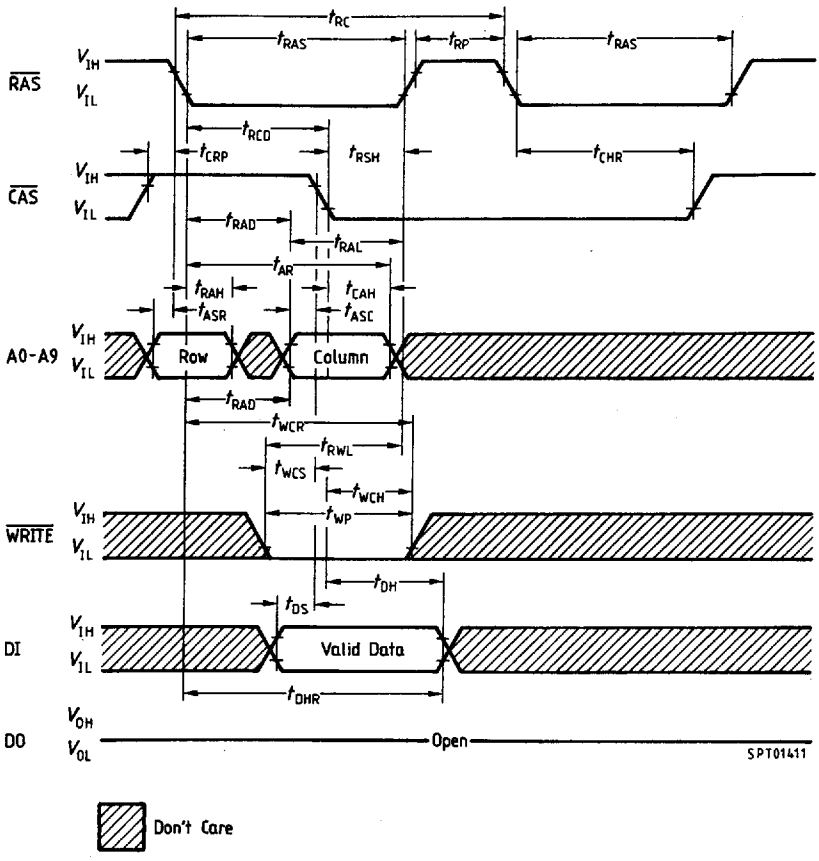


Hidden Refresh Cycle (Read)



Hidden Refresh Cycle (Write)

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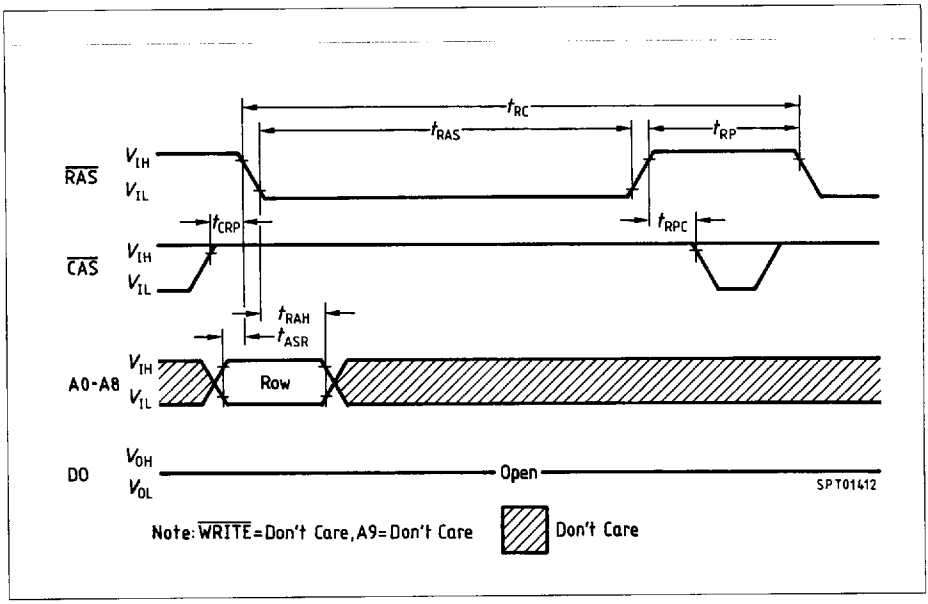
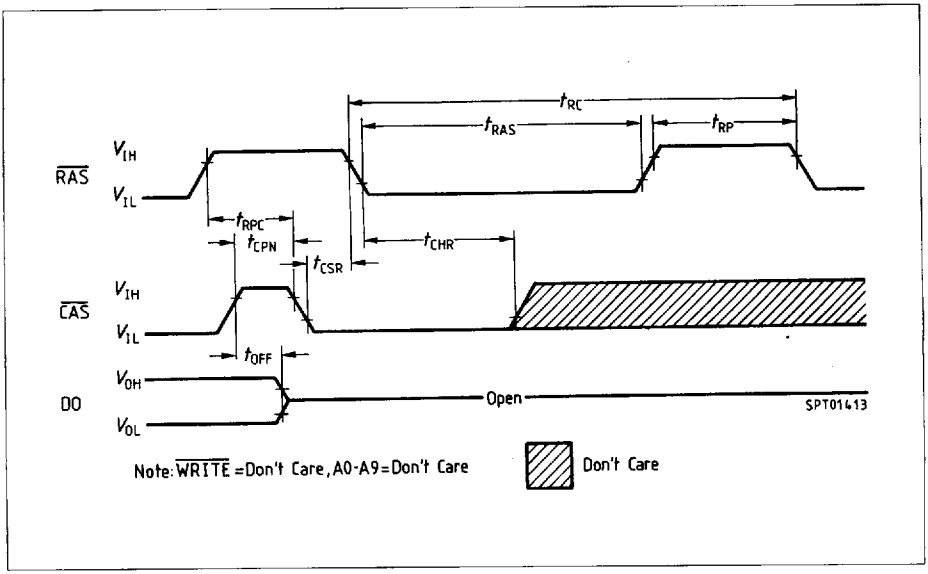


RAS-Only Refresh Cycle



CAS-Before-RAS Refresh Cycle