T-46-23-14

PRELIMINARY **CYM1838**

CYPRESS SEMICONDUCTOR

128K x 32 Static RAM Module

Features

- High-density 4-megabit SRAM module
- High-speed CMOS SRAMs
  - —Access time of 25 ns
- 66-pin, 1.1-inch-square PGA package
- Low active power
  - —4.0W (max.)
- Hermetic SMD technology
- TTL-compatible inputs and outputs
- Commercial and military temperature ranges

Functional Description

The CYM1838 is a very high performance 4-megabit static RAM module organized as 128K words by 32 bits. The module is constructed using four 128 x 8 static RAMs mounted onto a multilayer ceramic substrate. Four chip selects ($\overline{CS}_1$, $\overline{CS}_2$, $\overline{CS}_3$, $\overline{CS}_4$) are used to independently enable the four bytes. Reading or writing can be executed on individual bytes or any combination of multiple bytes through proper use of selects.

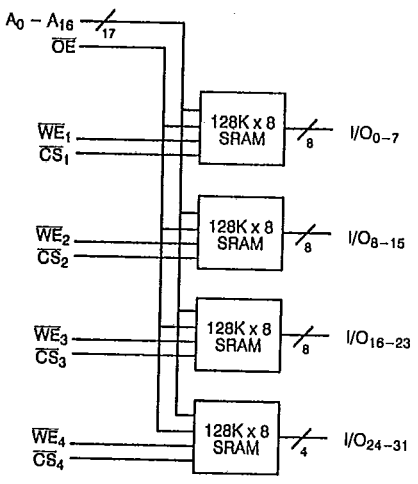
Writing to each byte is accomplished when the appropriate chip selects ($\overline{CS}_N$) and write enable ($\overline{WE}_N$) inputs are both LOW.

Data on the input/output pins (I/O_X) is written into the memory location specified on the address pins (A_0 through A_{14}).

Reading the device is accomplished by taking chip selects LOW while write enable remains HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the data input/output pins.

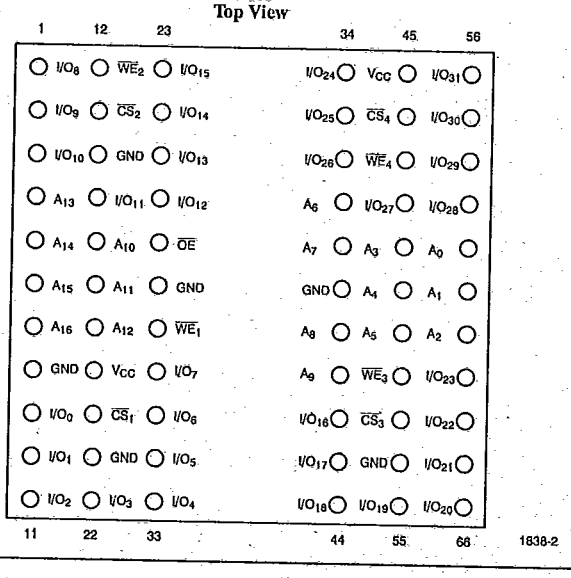
The data input/output pins remain in a high-impedance state when write enable is LOW or the appropriate chip selects are HIGH.

Logic Block Diagram



Pin Configuration

PGA
Top View



Selection Guide

		1838–25	1838–30	1838–35
Maximum Access Time (ns)		25	30	35
Maximum Operating Current (mA)	Commercial	720	720	720
	Military	720	720	720
Maximum Standby Current (mA)	Commercial	240	240	240
	Military	240	240	240

CYPRESS SEMICONDUCTOR

PRELIMINARY **CYM1838**

T-46-23-14

Maximum Ratings

(Above which the useful life may be impaired.)

Storage Temperature ..... – 65°C to +150°C
Supply Voltage to Ground Potential ..... – 0.5V to +7.0V
DC Voltage Applied to Outputs in High Z State ..... – 0.5V to +7.0V
DC Input Voltage ..... – 0.5V to +7.0V

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military	– 55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range

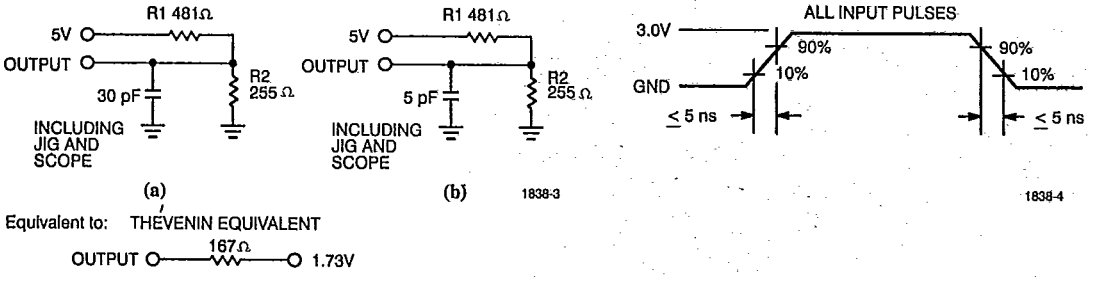
Parameters	Description	Test Conditions		Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4.0 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4	V
V_{IH}	Input HIGH Voltage			2.2	6.0	V
V_{IL}	Input LOW Voltage			– 0.3	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}, V_{CC} = Max.		– 10	+10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		– 10	+10	µA
I_{CCx32}	V_{CC} Operating Supply Current by 32 Mode	V_{CC} = Max., I_{OUT} = 0 mA, $\overline{CS}_N$ ≤ V_{IL}			720	mA
			L Version		720	
I_{CCx16}	V_{CC} Operating Supply Current by 16 Mode	V_{CC} = Max., I_{OUT} = 0 mA, $\overline{CS}_N$ ≤ V_{IL}			480	mA
			L Version		480	
I_{CCx8}	V_{CC} Operating Supply Current by 8 Mode	V_{CC} = Max., I_{OUT} = 0 mA, $\overline{CS}_N$ ≤ V_{IL}			360	mA
			L Version		360	
I_{SB1}	Automatic $\overline{CS}$ Power-Down Current[1]	Max. V_{CC}; $\overline{CS}$ ≥ V_{IH}, Min. Duty Cycle = 100%			240	mA
			L Version		200	
I_{SB2}	Automatic $\overline{CS}$ Power-Down Current[1]	Max. V_{CC}; $\overline{CS}$ ≥ V_{CC} – 0.2V, V_{IN} ≥ V_{CC} – 0.2V or V_{IN} ≤ 0.2V			40	mA
			L Version		20	

Capacitance[2]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	50	pF
C_{OUT}	Output Capacitance		50	pF

Notes:
1. A pull-up resistor to V_{CC} on the $\overline{CS}_N$ input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.
2. Tested on a sample basis.

AC Test Loads and Waveforms



Equivalent to: THEVENIN EQUIVALENT

Switching Characteristics Over the Operating Range[3]

Parameters	Description	1838–25		1838–30		1838–35		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	25		30		35		ns
t_{AA}	Address to Data Valid		25		30		35	ns
t_{OHA}	Data Hold from Address Change	3		3		3		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		25		30		35	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		12		13		15	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z		10		15		20	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z[4]	0		0		0		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z[4, 5]		15		18		20	ns
WRITE CYCLE[6]								
t_{WC}	Write Cycle Time	25		30		35		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	20		25		30		ns
t_{AW}	Address Set-Up to Write End	20		25		30		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	17		21		25		ns
t_{SD}	Data Set-Up to Write End	12		13		15		ns
t_{HD}	Data Hold from Write End	2		2		2		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[4]	0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[4, 6]	0	10	0	12	0	15	ns

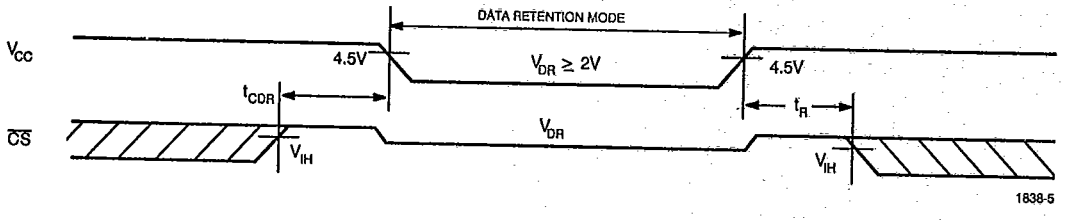
Data Retention Characteristics Over the Operating Range (L Version Only)

Parameters	Description	Test Conditions	1838		Units
			Min.	Max.	
V_{DR}	V_{CC} for Retention Data	$\overline{CS} > V_{CC} - 0.2V$	2.0	5.5	V
I_{CCDR3}	Data Retention Current	$\overline{CS} > V_{CC} - 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$, or $V_{IN} \leq 0.2V$, $V_{DR} = 3.0V$		3000	µA
t_{CDR}[7]	Chip Deselect to Data Retention Time		0		ns
t_R[7]	Operation Recovery Time		t_{RC}		ns

Notes:

3. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
4. At any given temperature and voltage condition, t_{HZCS} is less than t_{LZCS} for any given device. These parameters are guaranteed and not 100% tested.
5. t_{HZCS} and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
6. The internal write time of the memory is defined by the overlap of $\overline{CS}_N$ LOW and $\overline{WE}_N$ LOW. Both signals must be LOW to initiate a write, and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
7. Guaranteed, not tested.

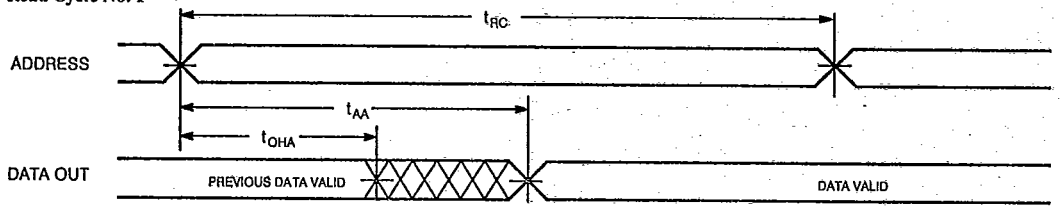
Data Retention Waveform



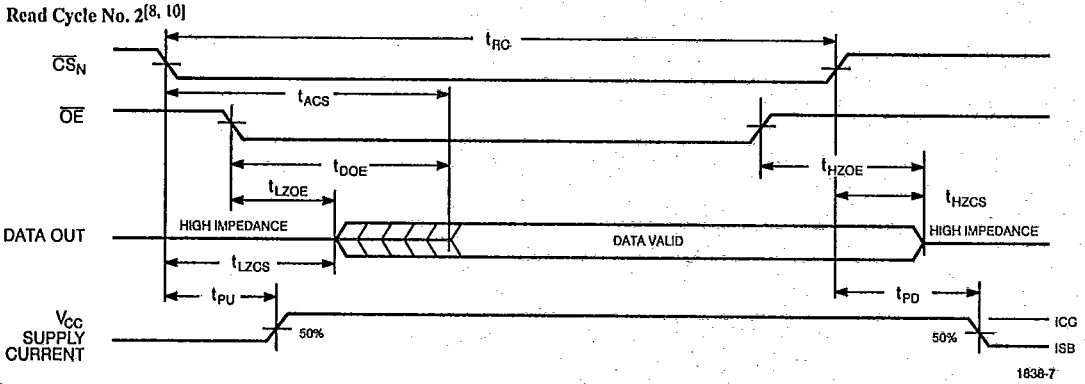
MODULES

Switching Waveforms

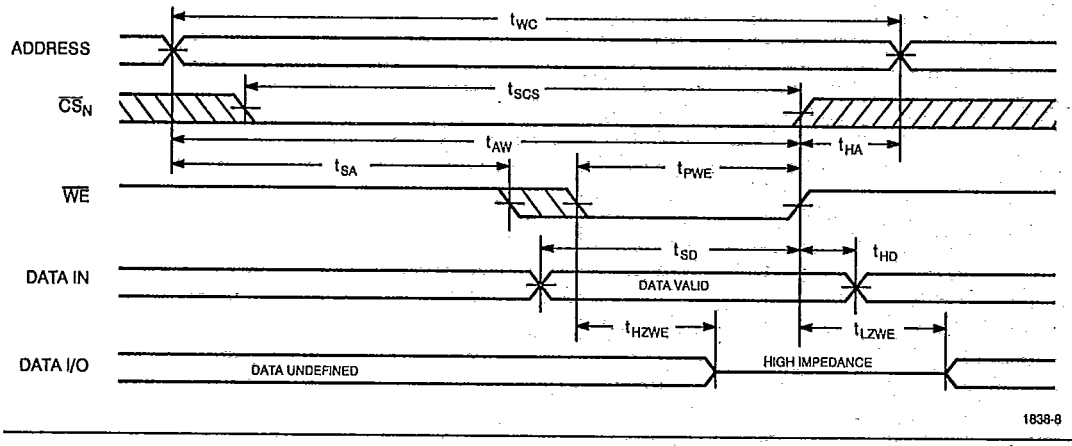
Read Cycle No. 1[8, 9]



Read Cycle No. 2[8, 10]



Write Cycle No. 1 ($\overline{WE}$ Controlled)[6, 11]

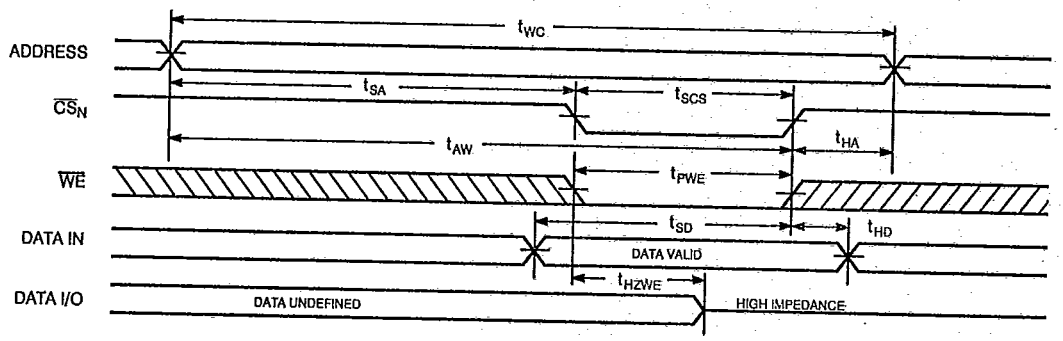


Notes:
8. $\overline{WE}_N$ is HIGH for read cycle.
9. Device is continuously selected, $\overline{CS} = V_{IL}$ and $\overline{OE} = V_{IL}$.
10. Address valid prior to or coincident with $\overline{CS}$ transition LOW.
11. Data I/O will be high impedance if $\overline{OE} = V_{IH}$.

T-46-23-14

Switching Waveforms (continued)

Write Cycle No. 2 ($\overline{CS}$ Controlled)[6, 11, 12]



Note:
12. If $\overline{CS}_N$ goes HIGH simultaneously with $\overline{WE}_N$ HIGH, the output remains in a high-impedance state.

Truth Table

$\overline{CS}_N$	$\overline{OE}$	$\overline{WE}_N$	Inputs/Outputs	Mode
H	X	X	High Z	Deselect/Power–Down
L	L	H	Data Out	Read
L	X	L	Data In	Write
L	H	H	High Z	Deselect

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
25	CYM1838HG–25C	HG01	Commercial
	CYM1838LHG–25C	HG01	
	CYM1838HG–25MB	HG01	Military
	CYM1838LHG–25MB	HG01	
30	CYM1838HG–30C	HG01	Commercial
	CYM1838LHG–30C	HG01	
	CYM1838HG–30MB	HG01	Military
	CYM1838LHG–30MB	HG01	
35	CYM1838HG–35C	HG01	Commercial
	CYM1838LHG–35C	HG01	
	CYM1838HG–35MB	HG01	Military
	CYM1838LHG–35MB	HG01	

Document #: 38–M–00046–A