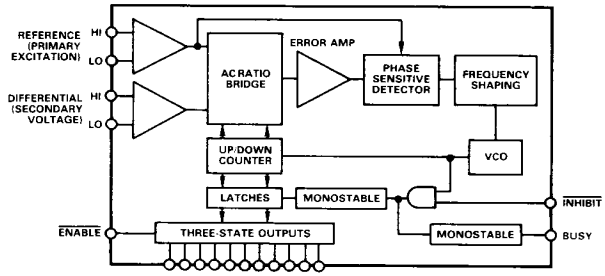
LVDT-to-Digital Converter

2S50

FEATURES
Internal Signal Conditioning
Direct Conversion to Digits
Reference Frequency 400Hz or 1kHz to 10kHz
High MTBF
No External Trims
Absolute Encoding

APPLICATIONS
Industrial Measurement and Gauging
Numerical Control
Avionic Control Systems
Valves and Actuators
Limit Sensing

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The 2S50 series converters translate the outputs from LVDT and RVDT transducers into digits directly. No signal conditioning, trims, preamplifiers, demodulators or filters are required. The 2S50 series can also be used as general purpose ratiometric A-to-D converters; very compatible with load cells, strain gauge bridges, some pressure transducers and interferometers.

The 2S50 linearly converts ac signals into an 11-bit parallel digital word. The digital output is an offset binary word which is the ratio of the signal and reference inputs. When used with LVDT and RVDT transducers, the digital output represents the linear or rotary displacements of the transducer. The converter is a continuous tracking type using a type 2 servo loop.

PRINCIPLE OF OPERATION

The 2S50 is a tracking converter. This means that the output automatically follows the input without the necessity of a convert command.

A conversion is initiated by a change of input signal equivalent to 1LSB of the output.

Each LSB increment of the output is indicated by a "Busy" pulse.

With an LVDT connected to give a null at center position, the output will track the input from digital "1 + all zeroes" to digital "all ones" for plus full scale, and digital "1 + all zeroes" to digital "all zeroes" for negative full scale.

The 2S50 operates only on the ratio of the two inputs for the conversion process. As such the whole system, consisting of excitation oscillator, LVDT and converter, is insensitive to change in excitation voltage, amplitude, frequency and waveshape.

Since a phase sensitive demodulator is included with the conversion loop of the 2S50, the system has a high rejection to signals that are not phase and frequency coherent with the excitation voltage. This feature, combined with ratiometric conversion gives a very high standard of integrity to digitized LVDT and RVDT systems.

PIN FUNCTION DESCRIPTION

$-V_S$	Main negative power supply $-15V$ dc.
$+V_S$	Main positive power supply $+15V$ dc.
$+5V$	Logic supply.
GND	Power supply ground. Digital ground. Reference voltage low.
Bit 1-11	Parallel output data bits.
Ref Hi	Analog reference input (Hi).
Diff Hi	Analog difference input (Hi).
Ref Lo	Analog reference input (Lo).
Diff Lo	Analog difference input (Lo).
$\overline{\text{INHIBIT}}$	Inhibit logic input. Taking this pin "Lo" inhibits data transfer from counter to output latches. The conversion loop continues to track.
BUSY	Converter BUSY. A "Hi" output indicates that the output latches are being updated. Data should not be transferred from the converter while BUSY is "Hi".
$\overline{\text{ENABLE}}$	The output data bits are set to a low impedance state by application of a logic "Lo".
CASE	This should normally be grounded. Case can be taken to any voltage with a low impedance up to $\pm 20V$.
N/C	Pins designated N/C not connected internally.

ORDERING INFORMATION

2S50/ X Y 0 B

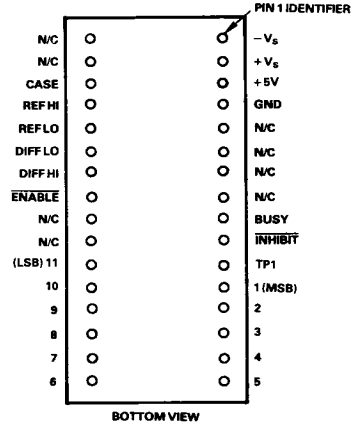
- B — High Reliability Processing
- Y = 1 — 400Hz reference frequency
- Y = 6 — 1kHz to 10kHz reference frequency
- X = 4 — −55°C to +125°C operating temperature range (Metal Package)
- X = 5 — 0 to +70°C operating temperature range (Ceramic Package)

2S50—SPECIFICATIONS (typical @ +25°C, unless otherwise noted)

Models	2S50/510	2S50/560	2S50/410	2S50/460
RESOLUTION	11 Bits	*	*	*
ACCURACY[1]	0.1% (Full Scale)	0.1%	0.2%	0.2%
LINEARITY	± 1/2LSB	*	*	*
REFERENCE FREQUENCY	400Hz	1kHz–10kHz	400Hz	1kHz–10kHz
SIGNAL INPUTS[2]	2.5V rms	*	*	*
INPUT IMPEDANCE	5MΩ (min)	*	*	*
SLEW RATE (Min)	200LSB/ms	400LSB/ms	200LSB/ms	400LSB/ms
SETTLING TIME (99% FS Step)	50ms	25ms	50ms	25ms
ACCELERATION CONSTANT (k_a)	70,000	650,000	70,000	650,000
BUSY PULSE	1μs (max) 1 LS TTL Load	* *	* *	* *
INHIBIT INPUT	Logic "Lo" to Inhibit 1 LS TTL Load	* *	* *	* *
POWER DISSIPATION	550mW	*	*	*
POWER SUPPLIES[3]	−15V @ 18mA (typ) 25mA (max) +15V @ 18mA (typ) 25mA (max) +5V @ 3mA (max)	* * *	* * *	* * *
TEMPERATURE RANGE Operating Storage	 0 to +70°C −60°C to +150°C	 * *	 −55°C to +125°C *	 ** *
DIMENSIONS	1.72" × 1.1" × 0.205" (43.5 × 28.0 × 5.2mm)	* *	1.74" × 1.14" × 0.28" (44.2 × 28.9 × 7.1mm)	** **
WEIGHT	1 oz. (28g)	*	*	*
PACKAGE OPTIONS[4]	DH-32E	DH-32E	M-32	M-32

NOTES
[1]Accuracy applies over ± 20% signal voltage, ± 20% excitation frequency and full temperature range, and for not greater than 3° phase error between reference and difference inputs.
[2]This is a nominal value.
[3]± 12 volts to ± 17 volts.
[4]DH-32E = Bottom Brazed Ceramic DIP; M = Metal Platform DIP. For outline information see Package Information section.
*Specifications same as 2S50/510.
**Specifications same as 2S50/410.
Specifications subject to change without notice.

PIN CONFIGURATION



ABSOLUTE MAXIMUM INPUTS (with respect to GND)

$+V_S$	0V to +17V dc
$-V_S$	0V to −17V dc
+5V	0V to +5.5V dc
Ref, Hi to Lo	±20V dc
Diff, Hi to Lo	±20V dc
Case to GND	±20V dc
Any Logical Input	−0.4V to +5.5V dc