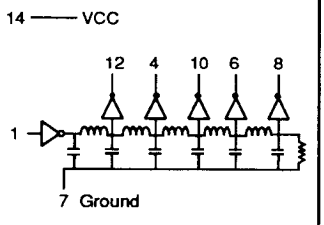
SMD 14 Pin J-Lead 5 Tap High Speed CMOS (HCT) Compatible Active Delay Lines

Tap Delays ±5% or ±2 nS				Total Delay ±5% or ±2 nS	Part Number
12*	17	22	27	32	EPA505-32
12*	18	24	30	36	EPA505-36
12*	19	26	33	40	EPA505-40
12*	20	28	36	44	EPA505-44
12*	21	30	39	48	EPA505-48
12*	22	32	42	52	EPA505-52
12*	24	36	48	60	EPA505-60
15	30	45	60	75	EPA505-75
20	40	60	80	100	EPA505-100

** Inherent Delay • Delay times referenced from input to leading edges at 25°C, 5.0V.*

DC Electrical Characteristics Parameter		Test Conditions	Min	Max	Unit
V_{IH}	High Level Input Voltage	V_{CC}=4.5 to 5.5	2.0		Volt
V_{IL}	Low Level Input Voltage	V_{CC}=4.5 to 5.5		0.8	Volt
V_{OH}	High Level Output Voltage	V_{CC}=4.5V,I_O=-4.0mA@V_{IH} or V_{IL}	4.0		Volt
V_{OL}	Low Level Output Voltage	V_{CC}=4.5V,I_O= 4.0mA@V_{IH} or V_{IL}		0.3	Volt
I_L	Input Leakage Current	V_{CC}=5.5V @V_{IH} or V_{IL}		±1.0	uA
I_{CC}	Supply Current	V_{CC}=5.5V,V_{IN}=0		15	mA
T_{RO}	Output Rise Time	.75 - 2.4 Volts		4	nS
N_H	High Fanout	V_{CC}=5.5V,V_{OH}=4.0V	10	LSTTL Load	

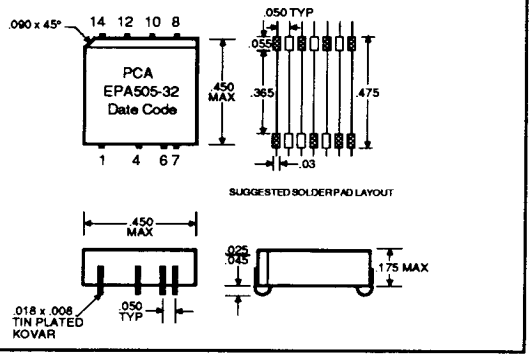
Schematic



Recommended Operating Conditions		Min	Max	Unit
V_{CC}	DC Supply Voltage	4.5	5.5	Volt
V_I	DC Input Voltage Range	0	V_{CC}	Volt
V_O	DC Output Voltage Range	0	V_{CC}	Volt
I_O	DC Output Source/Sink Current		25	mA
P_W*	Pulse Width % of Total Delay	40		%
D*	Duty Cycle		40	%
T_A	Operating Free Air Temperature	0	70	°C

**These two values are inter-dependent.*

Package Dimensions



Input Pulse Test Conditions @ 25°C (Taps Unloaded)

E_{IN}	Pulse Input Voltage	3.2 Volts
P_W	Pulse Width % of Total Delay	150%
T_{RI}	Input Rise Time (0.75 - 2.4 Volts)	2.0 nS
P_{RR}	Pulse Repetition Rate	1.0 MHz
V_{CC}	Supply Voltage	5.0 Volts

EPA505 9/90

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