SMALL COMPUTER SYSTEM INTERFACE (SCSI)

FEATURES

SCSI INTERFACE

- Interface to 1.5M bps (asynchronous)
- Supports initiator and target roles
- Parity generation with optional checking
- Arbitration support
- Direct control of all bus signals
- High current outputs drive SCSI bus

MPU INTERFACE

- Memory or I/O mapped interface
- DMA of programmed I/O
- Normal or block mode DMA
- Optional MPU interrupts

DESCRIPTION

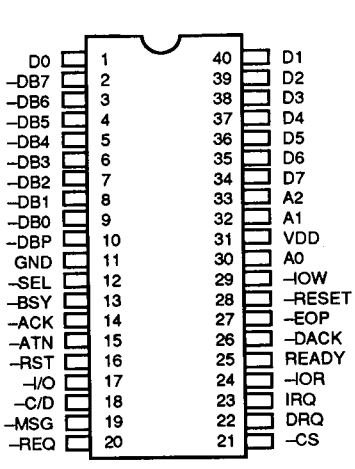
The VLSI Technology VL53C80 SCSI device is a 40-pin CMOS device designed to accommodate the Small Computer Systems Interface (SCSI) as defined by the ANSI X3T9.2 committee. The VL53C80 operates as both the initiator and the target and can therefore be used in host adapter, host port, and formatter designs. This device supports arbitration, including reselection. Special high-current open-collector output drivers, capable of sinking 48 mA at 0.5 V, connect directly to the SCSI bus.

The VL53C80 interfaces with the system microprocessor as a peripheral.

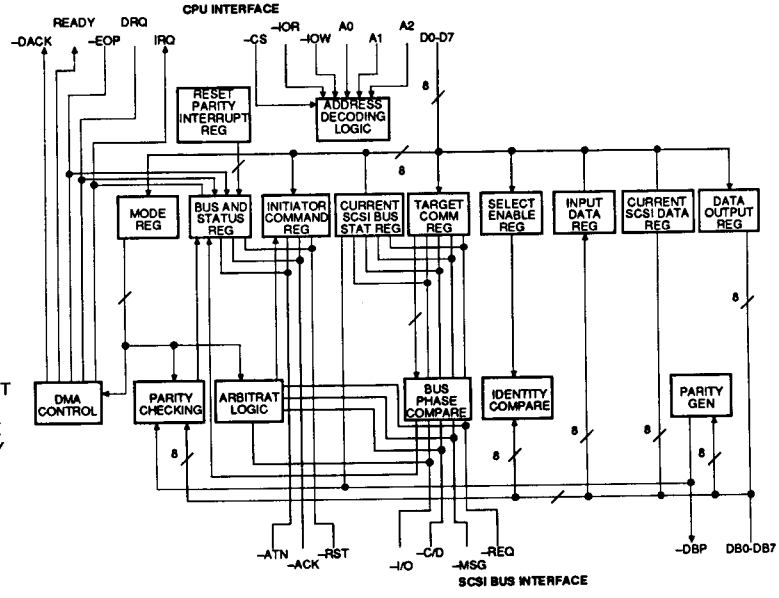
The device is controlled by reading and writing several internal registers which are addressed as standard or memory mapped I/O. DMA transfers require little CPU support because the VL53C80 controls the necessary handshake signals. The VL53C80 interrupts the MPU when it detects a bus condition requiring service. Normal and block mode DMA is also available to match several popular DMA controllers.

The VL53C80 is available in a 40-pin plastic or ceramic DIP as well as a 44-pin plastic leaded chip carrier.

PIN DIAGRAM



BLOCK DIAGRAM



ORDER INFORMATION

Part Number	Package
VL53C80-PC	Plastic DIP
VL53C80-CC	Ceramic DIP
VL53C80-QC	Plastic Leaded Chip Carrier (PLCC)

Note: Operating temperature range is 0°C to +70°C.

SIGNAL DESCRIPTIONS

Signal Name	Pin Number	Signal Type	Signal Description
D0-D7	1, 40-34	I/O*	Three-state microprocessor data bus lines. Active high when an output.
A0-A2	30, 32, 33	I*	These signals are used with –CS, –IOR, or –IOW to address the internal registers.
–RESET	28	I*	Reset - Clears all registers. It does not force the SCSI signal –RST to the active state. –RESET is active low.
–EOP	27	I*	End Of Process - Used to terminate a DMA transfer. If asserted during a DMA cycle, the current byte will be transferred but no additional bytes will be requested.
–IOR	24	I*	I/O Read - Used to read an internal register selected by –CS and A0-A2. It also selects the Input Data Register when used with –DACK. –IOR is active low.
–IOW	29	I*	I/O Write - Used to write an internal register selected by CS and A0-A2. When used with –DACK it selects the Output Data Register . –IOW is active low.
–CS	21	I*	Chip Select - An active low signal that enables a read or write of the internal register selected by address lines A0-A2.
–DACK	26	I*	DMA Acknowledge - This active low signal resets DRQ and selects the data register for input or output of data transfers.
IRQ	23	O*	Interrupt Request - Informs the microprocessor of an error condition or an event completion.
DRQ	22	O*	DMA Request - Indicates that the data register is ready to be read or written. DRQ occurs only if DMA mode is true in the Command Register. It is cleared by –DACK.
READY	25	O*	Ready - Can be used to control the speed of block mode DMA transfers. It goes active to indicate the chip is ready to send/receive data and remains false after a transfer until the last byte is sent or until the DMA Mode bit is reset.
VDD	31		+5 V.
GND	11		Ground.

*All pins interface directely with the microprocessor.

SIGNAL DESCRIPTIONS

Signal Name	Pin Number	Signal Type	Signal Description
–ACK	14	I/O*	Acknowledge - Driven by an initiator, –ACK shows an acknowledgment for a REQ/ACK data transfer handshake. In the target role, –ACK is received as a response to the –REQ signal.
–ATN	15	I/O*	Attention - Driven by an initiator, –ATN indicates an attention condition. This signal is received in the target role.
–BSY	13	I/O*	Busy - Indicates that the SCSI bus is being used and can be driven by both the initiator and the target device.
–C/D	18	I/O*	Control or Data - Driven by the target, –C/D indicates Control or Data information is on the data bus. It is received by the initiator.
–DB0- –DB7, –DBP	9-2, 10	I/O*	Data Bus - These eight data bits (–DB0- –DB7), plus a parity bit (–DBP) form the data bus. –DB7 is the most significant bit and has the highest priority during the Arbitration phase. Data parity is odd. Parity is always generated and optionally checked. Parity is not valid during arbitration.
–I/O	17	I/O*	Input/Output - Driven by a target which controls the direction of data movement on the SCSI bus. True (low) indicates input to the initiator. It is also used to distinguish between Selection and Reselection phases.
–MSG	19	I/O*	Message - Received by the initiator, and driven by the target during the Message phase.
–REQ	20	I/O*	Request - Driven by a target, –REQ indicates a request for a REQ/ACK data transfer handshake. It is received by the initiator.
–RST	16	I/O*	Reset - Indicates an SCSI bus reset condition.
–SEL	12	I/O*	Select - Used by an initiator to select a target or by a target to reselect an initiator.

*Bidirectional, active low, open collector signals with 48 mA sink capability. All pins interface directly with the SCSI bus.

FUNCTIONAL DESCRIPTION

The VL53C80 Small Computer Systems Interface (SCSI) device is seen as a set eight registers to the controlling MPU. By reading and writing the correct registers, the MPU may start any SCSI Bus function or may sample and assert any signal on the SCSI Bus. This permits the user to use all or portions of the SCSI protocol in software. These registers are read (written) by activating –CS with an address on A0-A2, and then issuing an –IOR (–IOW) pulse. The following section will describe the operation of the internal registers.

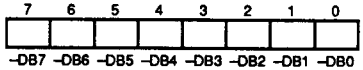
SCSI signal names are used to define the contents of the internal registers. Even though the bus is active low, a one (1) is used to indicate signal assertion and a zero (0) is used to indicate the inactive state. See Table 1.

DATA REGISTERS

The data registers are used for the transfer of SCSI commands, data, status, and message bytes between the microprocessor Data Bus and the SCSI Bus. The VL53C80 does not handle any information that passes through the data registers. The data registers consist of the transparent Current SCSI Data Register, the Output Data Register, and the Input Data Register.

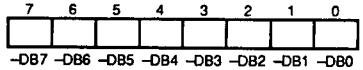
Current SCSI Data Register

Address 0 (Read Only) - The Current SCSI Data Register is a read only register which permits the microprocessor to read the active SCSI Data Bus. This is done by activating –CS with an address on A2-A0 of 000, and issuing an –IOR pulse. If parity checking is enabled, the SCSI Bus parity is checked at the beginning of the read cycle. This register is active during a programmed I/O data read, or during Arbitration to inspect for higher priority arbitrating devices. Parity is not assured valid during Arbitration.



Output Data Register

Address 0 (Write Only) - The Output Data Register is a write only register that is used to send data to the SCSI Bus. This done by either using a normal MPU write, or under DMA control, by using –IOW and –DACK. This register is further used to assert the correct ID bits on the SCSI Bus during the Arbitration and Selection phases.



Input Data Register

Address 6 (Read Only) - The Input Data Register is a read only register that is used to read latched data from the SCSI Bus. Data is latched either during a DMA Target receive operation as –ACK goes active, or during a DMA Initiator receive when –REQ goes active. The DMA Mode bit (port 2, bit 1) is to be set before data can be latched in the Input Data Register. This register may be read under DMA control using –IOR and –DACK. Parity may be checked when the Input Data Register is loaded, if desired.

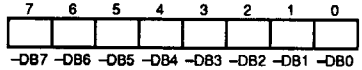
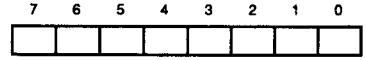


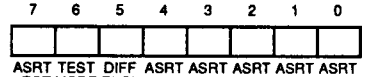
TABLE 1. REGISTER SUMMARY

Address			R/W	Register Name
A2	A1	A0		
0	0	0	R	Current SCSI Data
0	0	0	W	Output Data
0	0	1	R/W	Initiator Command
0	1	0	R/W	Mode
0	1	1	R/W	Target Command
1	0	0	R	Current SCSI Bus Status
1	0	0	W	Select Enable
1	0	1	R	Bus and Status
1	0	1	W	Start DMA Send
1	1	0	R	Input Data
1	1	0	W	Start DMA Target Receive
1	1	1	R	Reset Parity/Interrupts
1	1	1	W	Start DMA Initiator Receive

Initiator Command Register

Address 1 (Read/Write) - The Initiator Command Register is a read/write register that is used to assert some SCSI Bus signals, to monitor those signals, and to monitor the progress of bus arbitration. Many of these bits are significant only when being used as an Initiator. However, most can be used during Target role operation. Values for the Read and Write registers are shown below, respectively.





The following is a description of the operation of all bits in the Initiator Command Register.

Bit 7 - Assert –RST - Whenever a one (1) is written to bit 7 of the Initiator Command Register, the –RST signal is

asserted on the SCSI Bus. The –RST signal stays asserted until this bit is reset or an external –RESET occurs. After this bit is set (1), IRQ goes active. Then, all internal logic and control registers are reset (except for the interrupt latch and the Assert –RST bit). Writing a zero (0) to bit 7 of the Initiator Command Register releases the –RST signal. Reading this register shows the status of this bit.

Bit 6 - AIP (Arbitration in Progress) (Read Bit) - This bit is used to determine if arbitration is in progress. For this bit to be active, the Arbitrate bit (port 2, bit 0) must have been previously set . It indicates that a "bus free" condition has been detected, that the chip has asserted –BSY, and the contents of the Output Data Register (port 0) onto the SCSI Bus. AIP will remain active until the Arbitrate bit is reset.

Bit 6 - Test Mode (Write Bit) - This bit may be written during a test environment to disable all output drivers, thereby removing the VL53C80 from the circuit. Resetting this bit returns the device to normal operation.

Bit 5 - LA (Lost Arbitration) (Read Bit) - This bit, when active, indicates that the VL53C80 has found a bus free condition, arbitrated for use of the bus by asserting –BSY and its ID on the Data Bus, and lost Arbitration due to –SEL being asserted by another bus device. For this bit to be active, the Arbitrate bit (port 2, bit 0) must be active.

Bit 5 - DIFF ENBL (Differential Enable) (Write Bit) - This bit must be written with a zero (0) for proper operation.

Bit 4 - Assert –ACK - This bit is used by the bus initiator to assert –ACK on the SCSI Bus. To assert –ACK, the Target Mode bit (port 2, bit 6) must be false. Writing a zero (0) to this bit resets –ACK on the SCSI Bus. Reading this register simply reflects the status of this bit.

Bit 3 - Assert –BSY - Writing a one (1) into this bit position asserts –BSY onto the SCSI Bus. Conversely, a zero (0) resets the –BSY signal. Asserting –BSY indicates a successful selection or reselection and resetting this bit creates a bus disconnect condition. Reading this register simply reflects the status of this bit.

Bit 2 - Assert –SEL - Writing a one (1) into this bit position asserts –SEL onto the SCSI Bus. –SEL is normally asserted after Arbitration has been correctly completed. –SEL may be released by resetting this bit to a zero (0). A read of this register shows the status of this bit.

Bit 1 - Assert –ATN - –ATN may be asserted on the SCSI Bus by setting this bit to a one (1) if the Target Mode bit (port 2, bit 6) is false. –ATN is normally asserted, by the initiator, to request a Message Out bus phase. Note that since Assert –SEL and Assert –ATN are in the same register, a select with –ATN may be implemented with one MPU write. –ATN may not be asserted by resetting this bit to zero (0). A read of this register simply reflects the status of this bit.

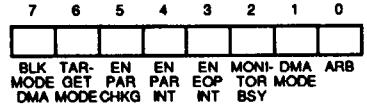
Bit 0 - Assert Data Bus - The Assert Data Bus bit, when set, allows the contents of the Output Data Register to be enabled as chip outputs on the signals –DB0 through –DB7. Parity is generated and asserted on –DBP also.

Connected as an Initiator, the outputs are only enabled if the Target Mode bit (port 2, bit 6) is false, the received signal –I/O is false, and the phase signals (–C/D, –I/O, and –MSG) match the contents of the Assert –C/D, Assert –I/O, and Assert –MSG in the Target Command Register.

This bit should also be set during DMA send operations.

Mode Register Address 2 (Read/ Write)

The Mode Register is used to control the operation of the chip. This register decides whether the VL53C80 operates as an Initiator or a Target, whether DMA transfers are being used, whether parity is checked, and whether interrupts are generated on various external conditions. This register may be read to inspect the value of these internal control bits. The operation of these control bits are shown below.



Bit 7 - Block Mode DMA - The Block Mode DMA bit controls the characteristics of the DMA DRQ/–DACK handshake. When this bit is reset (0), and the DMA Mode bit is active (1), the DMA handshake uses the normal interlocked handshake. The rising edge of –DACK shows the end of each byte being transferred. In block mode operations, Block Mode DMA bit set (1) and DMA Mode bit set (1), the end of –IOR or –IOW signifies the end of each byte transferred and –DACK is allowed to remain active throughout the DMA operation. READY can then be used to request the next transfer.

Bit 6 - Target Mode - The Target Mode bit allows the VL53C80 to operate as either an SCSI Bus Initiator, bit reset (0), or as an SCSI bus Target device, bit set (1). In order for the signals –ATN and –ACK to be asserted on the SCSI Bus, the Target Mode bit must be reset (0). In order for the signals –DC, –I/O, –MSG, and –REQ to be asserted on the SCSI Bus, the Target Mode bit should be set (1).

Bit 5 - Enable Parity Checking - The Enable Parity Checking bit decides whether parity errors will be ignored or saved in the parity error latch. If this bit is reset (0), parity will be ignored; if this bit is set (1), parity errors will be saved.

Bit 4 - Enable Parity Interrupt - The Enable Parity Interrupt bit, when set (1), will cause an interrupt (IRQ) to occur if a parity error is detected. A parity interrupt will only be generated if the Enable Parity Checking bit (bit 5) is also enabled (1).

Bit 3 - Enable EOP Interrupt - The Enable EOP Interrupt, when set (1), causes an interrupt to occur when an –EOP (End of Process) signal is received from the DMA controller logic.

Bit 2 - Monitor Busy - The Monitor Busy bit, when true (1) causes an interrupt to be generated for an unplanned loss of –BSY. When the interrupt is generated due to loss of –BSY, the lower six bits of the Initiator Command Register are reset (0) and all signals are removed from the SCSI Bus.

Bit 1 - DMA Mode - The DMA Mode bit is normally used to enable a DMA transfer and must be set (1) prior to

writing ports 5 through 7. Ports 5 through 7 are used to initiate DMA transfers. The Target Mode bit (port 2, bit 6) must be consistent with writes to port 6 and 7 (i.e., set (1) for a write to port 6 and reset (0) for a write to port 7). The control bit Assert Data Bus (port 1, bit 0) must be true (1) for all DMA send operations. In the DMA mode, –REQ and –ACK are controlled automatically.

The DMA Mode bit is not reset when the receipt of an –EOP signal occurs. Any DMA transfer may be stopped by writing a zero (0) into this bit. Care must be taken not to cause –CS and –DACK to become active simultaneously. –BSY must be active to set the DMA Mode bit.

Bit 0 - Arbitrate - The Arbitrate bit is set (1) to start the Arbitration process. Prior to setting this bit, the Output Data Register should contain the proper SCSI device ID value. Only one data bit should be active for SCSI Bus arbitration. The VL53C80 will wait for a bus free condition before entering the arbitration phase. The results of the arbitration phase are determined by reading the status bits LA and AIP (port 1, bits 5 and 6, respectively).

Target Command Register
Address 3 (Read/Write) - When connected as a target device, the Target Command Register allows the MPU to control the SCSI Bus Information Transfer phase and also to assert –REQ simply by writing this register. The Target Mode bit (port 2, bit 6) must be true (1) for bus assertion to occur. The SCSI Bus phases are described in Table 2.

When connected as an Initiator with DMA Mode true and if the phase lines (–I/O, –C/D, and –MSG) do not match the phase bits in the Target Command Register, a phase mismatch interrupt is caused when –REQ goes active. In order to send data as an Initiator, the Assert –I/O, Assert –C/D, and Assert –MSG bits must match the corresponding bits in the Current SCSI Bus Status Register (port 4). The Assert –REQ bit (bit 3) has no meaning when operating as an Initiator.

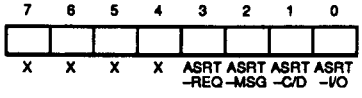
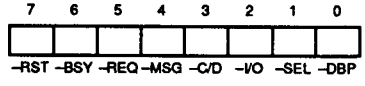


TABLE 2. SCSI INFORMATION TRANSFER PHASES

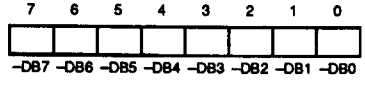
Bus Phase	Assert –I/O	Assert –C/D	Assert –MSG
Data Out	0	0	0
Unspecified	0	0	1
Command	0	1	0
Message Out	0	1	1
Data In	1	0	0
Unspecified	1	0	1
Status	1	1	0
Message In	1	1	1

The VL53C80 uses bit 7 of this register to determine when the last byte of DMA transfer is sent to the SCSI Bus. This flag is needed since the End of DMA bit in the Bus and Status Register only display when the last byte was received from the DMA.

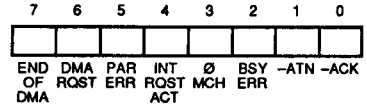
Current SCSI Bus Status Register
Address 4 (Read Only) - The Current SCSI Bus Status Register is a read only register which is used to monitor seven SCSI Bus control signals plus the Data Bus parity bit. An Initiator device can use this register to determine the current bus phase and poll –REQ for pending data transfers. This register may also be used to determine why a certain interrupt occurred. Values for the Current SCSI Bus Status Register are shown below.



Select Enable Register
Address 4 (Write Only) - The Select Enable Register is a write only register which is used as a mask to monitor a signal ID during a selection attempt. The simultaneous occurrence of the correct ID bit, –BSY false, and –SEL true will cause an interrupt. This interrupt can be disabled by resetting all bits in this register. If the Enable Parity Checking bit (port 2, bit 5) is active (1), parity will be examined during selection.



Bus and Status Register
Address 5 (Read Only) - The Bus and Status Register is a read only register which may be used to monitor the remaining SCSI control signals not found in the Current SCSI Bus Status Register (–ATN and –ACK), and six other status bits. Below is a description of each bit of the Bus and Status Register.



Bit 7 - End of DMA Transfer - The End of DMA Transfer bit is set if –EOP, –DACK, and either –IOR or –IOW are both active for at least 100 ns. Since the –EOP signal can occur during the last byte sent to the Output Data Register (port 0), the –REQ and –ACK signals must be monitored to insure that the last byte has been transferred. This bit is reset when the DMA Mode bit is reset (0) in the Mode Register (port 2).

Bit 6 - DMA Request - The DMA Request bit permits the MPU to sample the output pin DRQ. DRQ can be cleared by asserting –DACK or by resetting the DMA Mode bit (bit 1) in the Mode Register (port 2). The DRQ signal does not reset when a phase mismatch interrupt occurs.

Bit 5 - Parity Error - This bit is set if a parity error occurs during a data receive or a device selection. The Parity Error bit can only be set (1) if the Enable

Parity Check bit (port 2, bit 5) is active (1). This bit may be cleared by reading the Reset Parity/Interrupt Register (port 7).

Bit 4 - Interrupt Request Active - This bit is set if an enabled interrupt condition occurs. It reflects the current state of the IRQ output and can be cleared by reading the Reset Parity/Interrupt Register (port 7).

Bit 3 - Phase Match - The SCSI signals, –MSG, –C/D, and –I/O, represent the current information transfer phase. The Phase Match bit indicates whether the current SCSI Bus phase matches the lower three bits of the Target Command Register. Phase Match is continuously updated and is only significant when operating as a bus initiator. A phase match is required for data transfers to occur on the SCSI Bus.

Bit 2 - Busy Error - The Busy Error bit is active if an unexpected loss of the –BSY signal has occurred. This latch is set whenever the Monitor Busy bit (port 2, bit 2) is true and –BSY is false. An unexpected loss of –BSY will disable any SCSI outputs and will reset the DMA Mode bit (port 2, bit 1).

Bit 1 - ATN - This bit reflects the condition of the SCSI Bus control signal –ATN. This signal is normally monitored by the Target device.

Bit 0 - ACK - This bit reflects the condition of the SCSI Bus control signal –ACK. This signal is normally monitored by the Target device.

DMA REGISTERS

Three write only registers are used to initiate all DMA activity. They are Start DMA Send (port 5), Start DMA Target Receive (port 6) and Start DMA Initiator Receive (port 7). Simply writing these registers starts the DMA transfers. Data presented to the VL53C80 on signals D0 through D7 during the register write is meaningless and has no effect on the operation. Prior to writing these registers, the Block Mode DMA bit (bit 7), the DMA Mode bit (bit 1) and the Target Mode Bit (bit 6) in the Mode Register (port 2) must be appropriately set. The individual registers are briefly described as follows.

Start DMA Send

Address 5 (Write Only) - This register is written to initiate a DMA send, from the DMA to the SCSI Bus, for either initiator or target role operations. The DMA Mode bit (port 2, bit 1) must be set prior to writing this register.

Start DMA Target Receive

Address 6 (Write Only) - This register is written to initiate a DMA receive, from the SCSI Bus to the DMA, for Target operation only. The DMA Mode bit (bit 1) and the Target Mode bit (bit 6) in the Mode Register (port 2) must both be set (1) prior to writing this register.

Start DMA Initiator Receive

Address 7 (Write Only) - This register is written to initiate a DMA receive, from the SCSI Bus to the DMA, for initiator operation only. The DMA Mode bit (bit 6) must be false (0) in the Mode Register (port 2) prior to writing this register.

Reset Parity/Interrupt

Address 7 (Read Only) - Reading this register resets the Parity Error bit (bit 5), the Interrupt Request bit (bit 4), and the Busy Error bit (bit 2) in the Bus and Status Register (port 5).

ON-CHIP SCSI HARDWARE SUPPORT

The device allows direct control and monitoring of the SCSI Bus by providing a latch for each signal. Portions of the protocol define timings which are much too quick for traditional microprocessors to control. Therefore, hardware support has been provided for DMA transfers, bus arbitration, phase change monitoring, bus disconnection, bus reset, parity generation, parity checking, and device selection/reselection.

Arbitration is performed using a bus free filter to continuously inspect –BSY. If –BSY stays inactive for at least 400 ns, then the SCSI Bus is free, and arbitration may begin. Arbitration starts if the bus is free, –SEL is inactive, and the Arbitration bit (port 2, bit 0) is active. Once arbitration has started (–BSY asserted), an arbitration delay of 2.2 µs should elapse before the Data Bus can be examined to determine if arbitration has been won. This delay is implemented in the control software driver.

The VL53C80 is a clockwise device. Delays such as bus free delay, bus set delay, and bus-settle delay are implemented using gate delays. These delays may differ between devices because of inherent process variations, but are well within the proposed ANSI X3T9.2 specification (Revision 17).

INTERRUPTS

The VL53C80 provides an interrupt output (IRQ) to display a task completion or an unusual bus event. The use of interrupts is optional. They may be disabled by resetting the assigned bits in the Mode Register (port 2) or the Select Enable Register (port 4).

When an interrupt occurs, the Bus and Status Register and the Current SCSI Bus Status Register should be read to determine which condition caused the interrupt. IRQ can be reset simply by reading the Reset Parity/Interrupt Register (port 7) or by an external chip reset (–RESET active for 200 ns).

When the VL53C80 has been correctly initialized, an interrupt will be generated if the chip is selected or reselected, if an –EOP signal occurs during a DMA transfer, if an SCSI Bus reset occurs, if a parity error occurs during a data transfer, if a bus phase mismatch occurs, or if an SCSI Bus disconnection takes place.

Selection/Reselection

The VL53C80 can generate a select interrupt if –SEL is true (1), its device ID is true (1), and –BSY is false for at least one bus-settle delay (400 ns). If –I/O is active, this should be considered a reselect interrupt. The correct ID bit is determined by a match in the Select Enable Register (port 4). Only a single bit match is necessary to generate an interrupt. This interrupt may be disabled by writing zeros (0's) into all bits of the Select Enable Register.

If parity is supported, parity should also be good during the selection phase. Therefore, if the Enable Parity bit (port 2, bit 5) is active then the Parity Error bit should be checked to ensure that a proper selection has occurred. The Enable Parity Interrupt bit need not be set for this interrupt to be generated.

The proposed SCSI specification also requires that no more than two device IDs be active during the selection processor. To ensure this, the Current SCSI Data Register (port 0) should be read.

Values for the Bus and Status Register (port 5) and the Current SCSI Bus Status Register (port 4) are displayed below, respectively.

7	6	5	4	3	2	1	0
0	0	0	1	X	0	X	0
END OF DMA	DMA RQST	PAR ERR	INT RQST ACT	Ø MCH	BSY ERR	–ATN	–ACK

7	6	5	4	3	2	1	0
0	0	0	X	X	X	1	X
–RST	–BSY	–REQ	–MSG	–C/D	–I/O	–SEL	–DBP

End of Process (EOP) Interrupt

An End of Process signal (–EOP) which occurs during a DMA transfer (DMA Mode true) will set the End Of DMA Status bit (port 5, bit 7) and may generate an interrupt if Enable EOP Interrupt bit (port 2, bit 3) is true. The –EOP pulse will not be recognized (End of DMA bit set) unless –EOP, –DACK, and either –IOR or –IOW are simultaneously active for at least 100 ns. DMA transfers can still occur if –EOP was asserted at the correct time. This interrupt can be disabled by resetting the Enable EOP Interrupt bit.

Values for the Bus and Status Register (port 5) and the Current SCSI Bus Status Register (port 4) for this interrupt are shown below, respectively.

7	6	5	4	3	2	1	0
1	0	0	1	0	0	0	X
END OF DMA	DMA RQST	PAR ERR	INT RQST ACT	Ø MCH	BSY ERR	–ATN	–ACK

7	6	5	4	3	2	1	0
0	1	X	X	X	X	0	X
–RST	–BSY	–REQ	–MSG	–C/D	–I/O	–SEL	–DBP

The End Of DMA bit is used to determine when a block transfer is complete. Receive operations are complete when there is no data left in the chip and no additional handshakes occurring. The only exception to this is receiving data as an Initiator and the Target opts to send additional data for the same phase. In this case, –REQ goes active and the new data appears in the Input Data Register. Since a phase mismatch interrupt will not occur, –REQ and –ACK must be sampled to determine that the Target is attempting to send more data.

For send operations, the End Of DMA bit is set when the DMA completes its transfer, but the SCSI transfer may still be in progress. If connected as a Target, –REQ and –ACK should be sampled until both are false. If connected as an Initiator, a phase change interrupt can be used to signal the completion of the previous phase. It is possible for the Target to request more data for the same phase. Then, a phase change will not occur and both –REQ and –ACK must be sampled to determine when the last byte was transferred.

SCSI Bus Reset

The VL53C80 generates an interrupt when the –RST signal changes to true. The device releases all bus signals within a bus clear delay (800 ns) of this transition. This interrupt also occurs after setting the Assert –RST bit (port 1, bit 7). This interrupt cannot be disabled. (Note: –RST is not latched in bit 7 of the Current SCSI Bus Status Register and may not be active when this port is read. For this case, the Bus Reset interrupt may be determined by default.)

Values for the Bus and Status Register (port 5) and the Current SCSI Bus Status Register (port 4) are displayed below, respectively.

7	6	5	4	3	2	1	0
0	X	0	1	X	0	X	X
END OF DMA	DMA RQST	PAR ERR	INT RQST ACT	Ø MCH	BSY ERR	–ATN	–ACK

7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X
–RST	–BSY	–REQ	–MSG	–C/D	–I/O	–SEL	–DBP

Parity Error

An interrupt is generated for a received parity error if the Enable Parity Check (bit 5) and the Enable Parity Interrupt (bit 4) bits are set (1) in the Mode Register (port 2). Parity is checked while reading the Current SCSI Data Register (port 0) and during a DMA receive operation. A parity error can be detected without generating an interrupt by disabling the Enable Parity Interrupt bit and checking the Parity Error flag (port 5, bit 5).

Values for the Bus and Status Register (port 5) and the Current SCSI Bus Status Register (port 4) are displayed below, respectively.

7	6	5	4	3	2	1	0
0	X	1	1	1	0	X	X
END OF DMA	DMA RQST	PAR ERR	INT RQST ACT	Ø MCH	BSY ERR	–ATN	–ACK

7	6	5	4	3	2	1	0
0	1	1	X	X	X	0	X
–RST	–BSY	–REQ	–MSG	–C/D	–I/O	–SEL	–DBP

Bus Phase Mismatch

The SCSI phase lines contain the signals –I/O, –C/D, and –MSG. These signals are compared with the corresponding bits in the Target Command Register: Assert –I/O (bit 0), Assert –C/D (bit 1), and Assert –MSG (bit 2). The comparison continually occurs, and is reflected in the Phase Match bit (bit 3) of the Bus and Status Register (port 5). An interrupt (IRQ) is generated if the DMA Mode bit (port 2, bit 1) is active and a phase mismatch occurs when –REQ transitions from false to true.

A phase mismatch prevents the recognition of –REQ and also removes the chip from the bus during an Initiator send operation. –DB0 through –DB7, and –DBP will not be driven even though the Assert Data Bus bit (port 1, bit 0) is active. This interrupt is only active when connected as an Initiator and may be disabled by resetting the DMA Mode bit. (Note: It is possible for this interrupt to occur when connected as a Target if another device is driving the phase lines to a different state.)

Values for the Bus and Status Register (port 5) and the Current SCSI Bus Status Register (port 4) are displayed below, respectively.

7	6	5	4	3	2	1	0
0	0	0	1	0	0	X	0
END OF DMA	DMA RQST	PAR ERR	INT RQST ACT	Ø MCH	BSY ERR	–ATN	–ACK

7	6	5	4	3	2	1	0
0	1	X	X	X	X	0	X
–RST	–BSY	–REQ	–MSG	–C/D	–I/O	–SEL	–DBP

Loss of –BSY
When the Monitor Busy bit (bit 2) in the Mode Register (port 2) is active, an interrupt will be generated if the –BSY signal goes false for at least one bus-settle delay (400 ns). This interrupt may be disabled by resetting the Monitor Busy bit. Values are displayed below for the Bus and Status Register and Current SCSI Bus Status Register, respectively.

7	6	5	4	3	2	1	0
0	0	0	1	X	1	0	0
END OF DMA	DMA RQST	PAR ERR	INT RQST ACT	Ø MCH	BSY ERR	–ATN	–ACK

7	6	5	4	3	2	1	0
0	0	0	X	X	X	0	0
–RST	–BSY	–REQ	–MSG	–C/D	–I/O	–SEL	–DBP

RESET CONDITIONS
There are three reset situations that apply to the VL53C80:

Hardware Chip Reset
When the signal –RST is active for at least 200 ns, the VL53C80 device is re-initialized and all internal logic and control registers are cleared. This is only a chip reset, and does not cause and SCSI Bus reset condition.

SCSI Bus Reset (–RST) Received
When an SCSI –RST signal is detected, an IRQ interrupt is generated and a chip reset occurs. All internal logic and registers are cleared, except for the IRQ interrupt latch and the Assert –RST bit (bit 7) in the Initiator Command Register (port 1). (Note: The –RST signal may be sampled by reading the Current SCSI Bus Status Register (port 4). This signal is not latched and may not be present when this port is read.)

SCSI Bus Reset (–RST) Issued
If the MPU sets the Assert –RST bit (bit 7) in the Initiator Command Register (port 1), the –RST signal goes active on the SCSI Bus and an internal reset occurs. All internal logic and registers are cleared except for the IRQ interrupt latch and the Assert –RST bit (bit 7) in the Initiator Command Register (port 1). The –RST signal continues to be active until the Assert –RST bit is reset or until a hardware reset occurs.

DATA TRANSFERS
Data may be transferred between SCSI Bus devices in one of four modes:
1) Programmed I/O
2) Normal DMA
3) Block Mode DMA
4) Pseudo DMA.

The following sections describe these modes in detail. (Note: For all data transfer operations –DACK and –CS can never be active at the same time).

Programmed I/O Transfers
Programmed I/O is the most basic form of data transfer. The –REQ and –ACK handshake signals are individually examined and asserted by reading and writing the appropriate register bits. This type of transfer is usually used when transferring small blocks of data (e.g. command blocks or message and status bytes).

An initiator send operation will begin by setting the –C/D, –I/O, and –MSG bits in the Target Command Register to the correct state so that a phase match exists. In addition to the phase match condition, it is necessary for the Assert Data Bus bit (port 1, bit 0) to be true and the received I/O signal to be false for the VL53C80 to send data.

For every transfer, the data is loaded to the Output Data Register (port 0). The MPU then waits for the –REQ bit (port 4, bit 5) to become active. Once –REQ goes active, the Phase Match bit (port 5, bit 3) is checked and the Assert –ACK bit (port 1, bit 4) is set. The –REQ bit is sampled until it becomes false and the MPU resets the Assert –ACK bit to complete the transfer.

Normal DMA Mode
DMA transfers are usually used for large block transfers. The SCSI chip outputs a DMA request (DRQ) whenever it is ready for a byte transfer. External DMA logic uses this DRQ signal to generate –DACK and an –IOR or an –IOW pulse to the VL53C80. DRQ becomes inactive when –DACK is asserted and –DACK goes inactive some time after the minimum read or write pulse width. This process is repeated for every byte. In this mode, –DACK should not be allowed to cycle unless a transfer is occuring.

Block Mode DMA
Popular DMA controllers such as the 9517A provide a Block Mode DMA transfer. This type of transfer allows the DMA controller to transfer blocks of data without giving up the use of the Data Bus to the MPU after each byte is transferred. This way, faster transfer rates are achieved by eliminating the repetitive access and release of the MPU Bus.

If the Block Mode DMA bit (port 2, bit 7) is active, the VL53C80 begins the transfer by asserting DRQ. The DMA controller then asserts –DACK for the duration of the block transfer. DRQ becomes inactive for the remainder of the transfer. The READY output can be used to control the transfer rate.

Non-block mode DMA transfers terminate when –DACK goes false, whereas Block Mode transfers end when –IOR or –IOW becomes inactive. DMA transfers may be started sooner in a Block Mode transfer.

To obtain the best performance in Block Mode operation, the DMA logic should use the normal DMA mode interlocking handshake. READY is available to throttle the DMA transfer, but DRQ is 30 to 40 ns faster than READY, and may be used to start the cycle sooner.

The methods described under "Halting a DMA Operation" apply for all DMA operations.

Pseudo DMA Mode
In order to avoid monitoring and asserting the request/acknowledge handshake signals for programmed I/O transfers, the system may be designed to implement a pseudo DMA mode. This mode initiated by programming the VL53C80 to operating in the DMA mode, by using the MPU to emulate the DMA handshake. DRQ may be detected by polling the DMA Request bit (bit 6) in the Bus and Status Register (port 5), by sampling the signal through an external port or by using it to cause a MPU interrupt. Once DRQ is detected, the MPU can perform a read or write data transfer. This MPU read/write is externally decoded to generate the correct –DACK and –IOR or –IOW signals.

Frequently, external decoding logic is needed to generate the VL53C80 –CS signal. This same logic may be used to generate –DACK at no extra system cost and provide an increased performance in programmed I/O transfers.

Halting a DMA Operation

The –EOP signal is one way to halt a DMA transfer. A bus phase mismatch or a reset of the DMA Mode bit (port 2, bit 1) can also end a DMA cycle for the current bus phase.

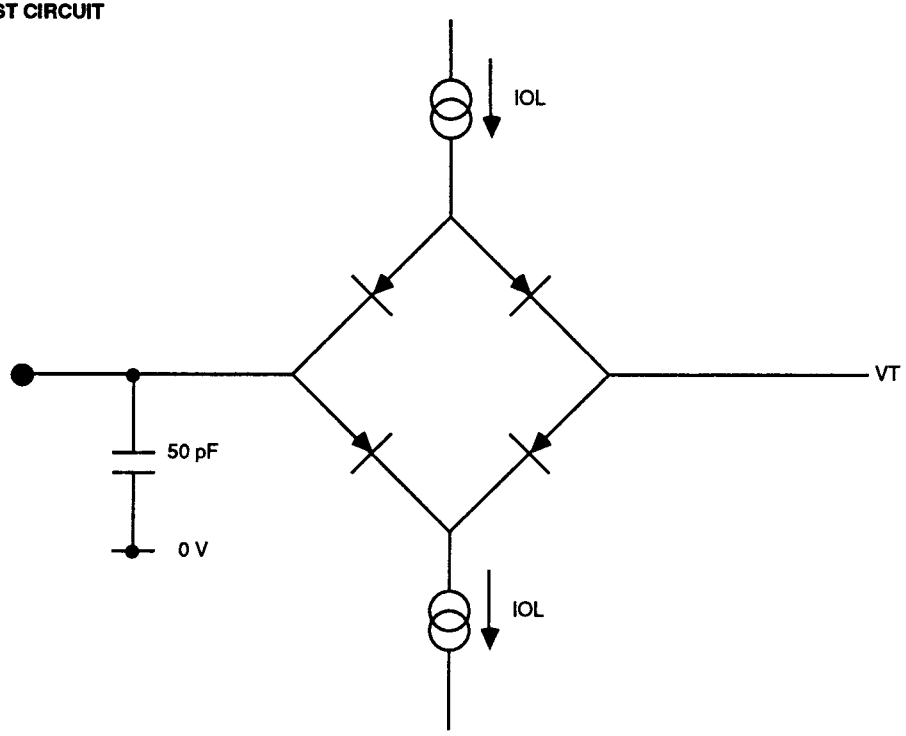
Using the –EOP Signal - If –EOP is used, it should be asserted for at least 100 ns while –DACK and –IOR or –IOW are both active. If either–IOR or –IOW are not active, an interrupt will be generated, but the DMA activity will continue. The –EOP signal does not reset the DMA Mode bit. The –EOP signal can occur during the last byte sent to the Output Data Register (port 0). The –REQ and –ACK signals should be monitored to ensure that the last byte has transferred.

Bus Phase Mismatch Interrupt - A bus phase mismatch interrupt may be used to halt the transfer if operating as an Initiator. Using this method frees the host from maintaining a data length counter and frees the DMA logic from providing the –EOP signal. If performing an Initiator send operation, the VL53C80 requires –DACK to cycle before –ACK goes inactive. Since phase changes cannot occur if –ACK is active, either –DACK must be cycled after the last byte is sent or the DMA Mode bit must be reset in order to receive the phase mismatch interrupt.

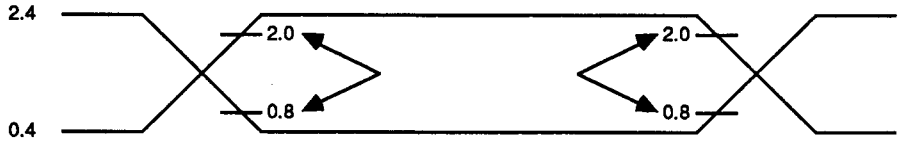
Resetting the DMA Mode Bit - A DMA operation may be stopped at any time simply by resetting the DMA Mode bit. It is recommended that the DMA Mode bit be reset after receiving an –EOP or bus phase mismatch interrupt. The DMA Mode bit must then be set before writing any of the start DMA register for later bus phases.

If resetting the DMA Mode bit is used instead of –EOP for Target role operation, then care must be exercised to reset this bit at the proper time. When receiving data as a Target device, the DMA Mode bit must be reset once the last DRQ is received and before –DACK is asserted to prevent an additional –REQ from taking place. Resetting this bit causes DRQ to go inactive. The last byte received remains in the Input Data Register and may be obtained either by performing a normal MPU read or by cycling –DACK or –IOR. Frequently, –EOP is easier to use when operating as a Target device.

SWITCHING TEST CIRCUIT



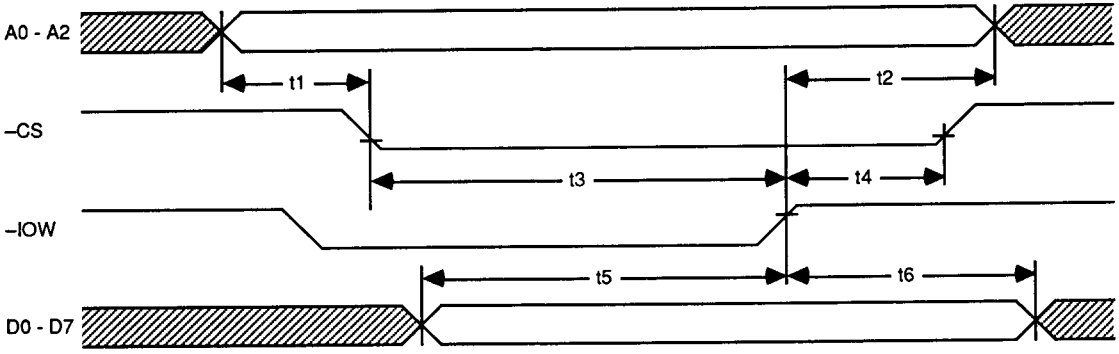
SWITCHING TEST WAVEFORM



SWITCHING CHARACTERISTICS/WAVEFORMS

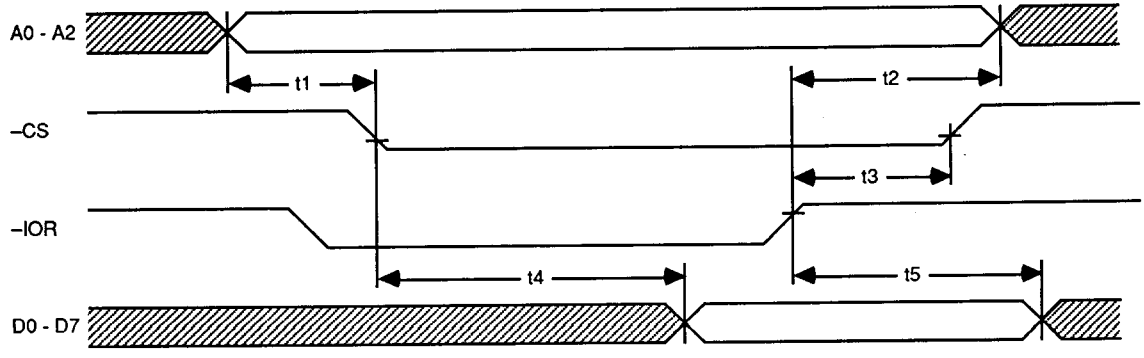
CPU WRITE

Symbol	Description	Min	Max	Units	Condition
t1	Address Setup to Write Enable	20		ns	Write Enable Occurs When –IOW and –CS
t2	Address Hold from End Write Enable	20		ns	Write Enable Occurs When –IOW and –CS
t3	Write Enable Width	70		ns	Write Enable Occurs When –IOW and –CS
t4	Chip Select Hold from End of –IOW	0		ns	
t5	Data Setup to End of Write Enable	50		ns	Write Enable Occurs When –IOW and –CS
t6	Data Hold Time from End of –IOW	30		ns	



CPU READ

Symbol	Description	Min	Max	Units	Condition
t1	Address Setup to Read Enable	20		ns	Read Enable Occurs When –IOR and –CS
t2	Address Hold from End Read Enable	20		ns	Read Enable Occurs When –IOR and –CS
t3	Chip Select Hold from End of –IOR	0		ns	
t4	Data Access Time from Read Enable		130	ns	Read Enable Occurs When –IOR and –CS
t5	Data Hold Time from End of –IOR	20		ns	

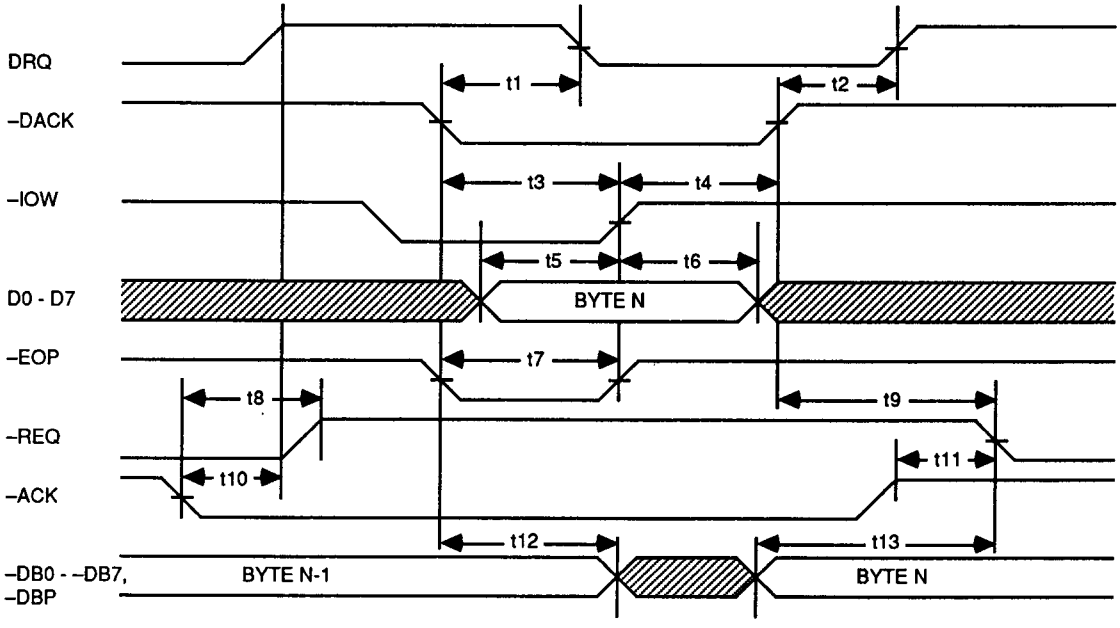


SWITCHING CHARACTERISTICS/WAVEFORMS (Cont.)

DMA WRITE (NON-BLOCK MODE) TARGET SEND

Symbol	Description	Min	Max	Units	Condition
t1	DRQ False from –DACK True		130	ns	
t2	–DACK False to DRQ True	30		ns	
t3	Write Enable Width	100		ns	Write Enable Occurs When –IOW and –DACK
t4	DACK Hold from End of –IOW	0		ns	
t5	Data Setup to End of Write Enable	50		ns	Write Enable Occurs When –IOW and –DACK
t6	Data Hold Time from End of –IOW	40		ns	
t7	Width of –EOP Pulse (Note)	100		ns	
t8	–ACK True to –REQ False	25	125	ns	
t9	–REQ from End of –DACK (–ACK False)	30	150	ns	
t10	–ACK True to DRQ True (Target)	15	110	ns	
t11	–REQ from End of –ACK (–DACK False)	20	150	ns	
t12	Data Hold from Write Enable	15		ns	
t13	Data Setup to –REQ True (Target)	60		ns	

Note: –EOP, –IOW, and –DACK must be concurrently true for at least t7 for proper recognition of the –EOP pulse.

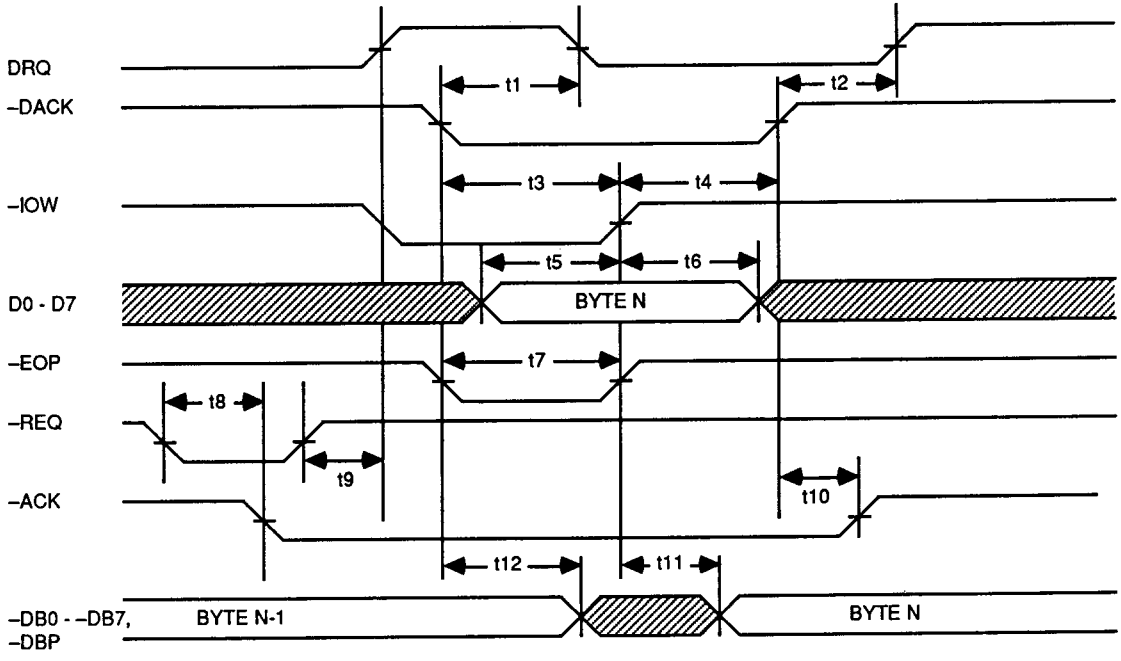


SWITCHING CHARACTERISTICS/WAVEFORMS (Cont.)

DMA WRITE (NON-BLOCK MODE) INITIATOR SEND

Symbol	Description	Min	Max	Units	Condition
t1	DRQ False from –DACK True		130	ns	
t2	–DACK False to DRQ True	30		ns	
t3	Write Enable Width	100		ns	Write Enable Occurs When –IOW and –DACK
t4	–DACK Hold from End of –IOW	0		ns	
t5	Data Setup to End of Write Enable	50		ns	Write Enable Occurs When –IOW and –DACK
t6	Data Hold Time from End of –IOW	40		ns	
t7	Width of –EOP Pulse (Note)	100		ns	
t8	–REQ True to –ACK True	20	160	ns	
t9	–REQ False to DRQ True	20	110	ns	
t10	–DACK False to –ACK False	25	150	ns	
t11	–IOW False to Valid SCSI Data		100	ns	
t12	Data Hold from Write Enable	15		ns	

Note: –EOP, –IOW, and –DACK must be concurrently true for at least t7 for proper recognition of the –EOP pulse.

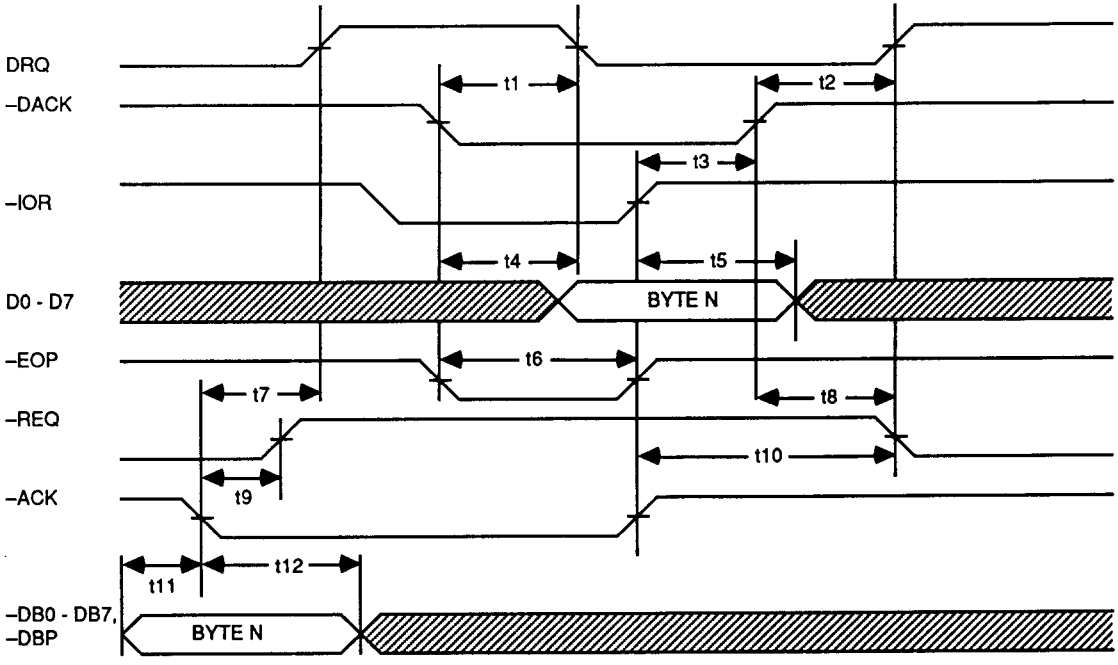


SWITCHING CHARACTERISTICS/WAVEFORMS (Cont.)

DMA READ (NON-BLOCK MODE) TARGET RECEIVE

Symbol	Description	Min	Max	Units	Condition
t1	DRQ False from –DACK True		130	ns	
t2	–DACK False to DRQ True	30		ns	
t3	–DACK Hold Time from End of –IOR	0		ns	
t4	Data Access Time from Read Enable		115	ns	Read Enable Occurs When –IOR and –DACK
t5	Data Hold Time from End of –IOR	20		ns	
t6	Width of –EOP Pulse (Note)	100		ns	
t7	–ACK True to DRQ True	15	110	ns	
t8	–DACK False to –REQ True (–ACK False)	30	150	ns	
t9	–ACK True to –REQ False	25	125	ns	
t10	–ACK False to –REQ True (–DACK False)	20	150	ns	
t11	Data Setup Time to –ACK	20		ns	
t12	Data Hold Time from –ACK	50		ns	

Note: –EOP, –IOR, and –DACK must be concurrently true for at least t6 for proper recognition of the –EOP pulse.

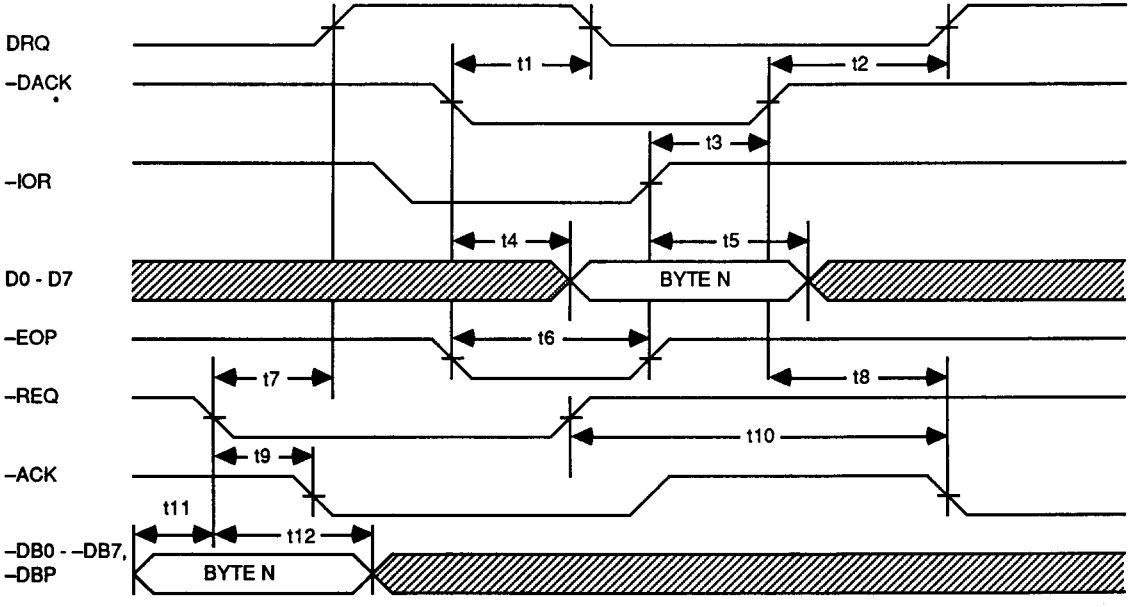


SWITCHING CHARACTERISTICS/WAVEFORMS (Cont.)

DMA READ (NON-BLOCK MODE) INITIATOR RECEIVE

Symbol	Description	Min	Max	Units	Condition
t1	DRQ False from –DACK True		130	ns	
t2	–DACK False to DRQ True	30		ns	
t3	–DACK Hold Time from End of –IOR	0		ns	
t4	Data Access Time from Read Enable		115	ns	Read Enable Occurs When –IOR and –DACK
t5	Data Hold Time from End of –IOR	20		ns	
t6	Width of –EOP Pulse (Note)	100		ns	
t7	–REQ True to DRQ True	20	150	ns	
t8	–DACK False to –ACK False (–REQ False)	25	160	ns	
t9	–REQ True to –ACK True	20	160	ns	
t10	–REQ False to –ACK False (–DACK False)	15	140	ns	
t11	Data Setup Time to –REQ	20		ns	
t12	Data Hold Time from –REQ	50		ns	

Note: –EOP, –IOR, and –DACK must be concurrently true for at least t6 for proper recognition of the –EOP pulse.

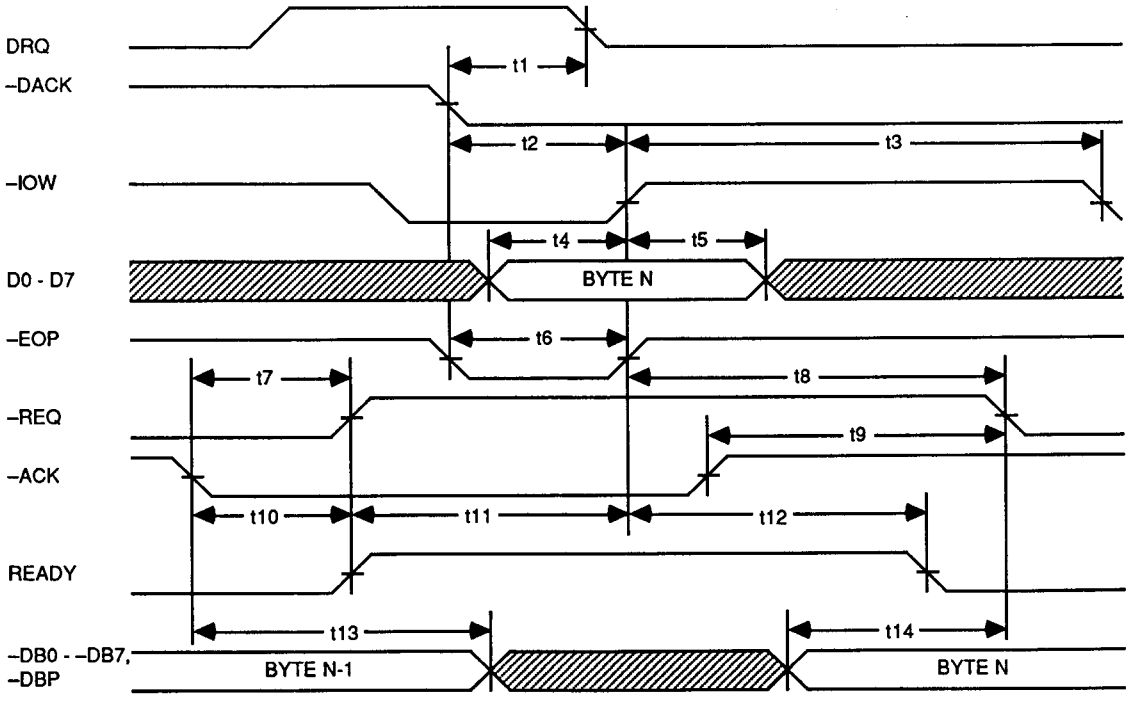


SWITCHING CHARACTERISTICS/WAVEFORMS (Cont.)

DMA WRITE (BLOCK MODE) TARGET SEND

Symbol	Description	Min	Max	Units	Condition
t1	DRQ False from –DACK True		130	ns	
t2	Write Enable Width	100		ns	Write Enable Occurs When –IOW and –DACK
t3	Write Recovery Time	120		ns	
t4	Data Setup to End of Write Enable	50		ns	Write Enable Occurs When –IOW and –DACK
t5	Data Hold Time from End of –IOW	40		ns	
t6	Width of –EOP Pulse (Note)	100		ns	
t7	–ACK True to –REQ False	25	125	ns	
t8	–REQ from End of –ACK (–ACK False)	40	180	ns	
t9	–REQ from End of –ACK (–IOW False)	20	170	ns	
t10	–ACK True to READY True	20	140	ns	
t11	READY True to –IOW False	70		ns	
t12	–IOW False to READY False	20	140	ns	
t13	Data Hold from –ACK True	40		ns	
t14	Data Setup to –REQ True	60		ns	

Note: –EOP, –IOW, and –DACK must be concurrently true for at least t6 for proper recognition of the –EOP pulse.

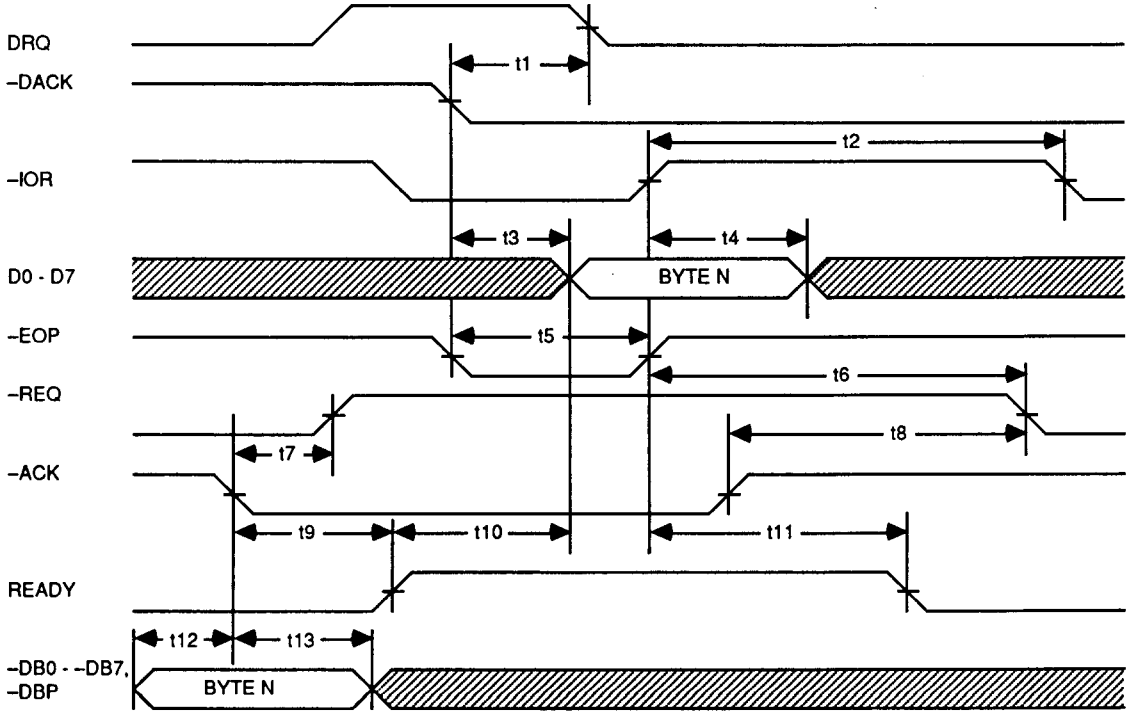


SWITCHING CHARACTERISTICS/WAVEFORMS (Cont.)

DMA READ (BLOCK MODE) TARGET RECEIVE

Symbol	Description	Min	Max	Units	Condition
t1	DRQ False from –DACK True		130	ns	
t2	–IOR Recovery Time	120		ns	
t3	Data Access Time from Read Enable		110	ns	Read Enable Occurs When –IOR and –DACK
t4	Data Hold Time from End of –IOR	20		ns	
t5	Width of –EOP Pulse (Note)	100		ns	
t6	–IOR False to –REQ True (–ACK False)	30	190	ns	
t7	–ACK True to –REQ False	20	125	ns	
t8	–ACK False to –REQ True (–IOR False)	20	170	ns	
t9	–ACK True to READY True	20	140	ns	
t10	READY true to Valid Data		50	ns	
t11	–IOR False to READY False	20	140	ns	
t12	Data Setup Time to –ACK	20		ns	
t13	Data Hold Time from –ACK	50		ns	

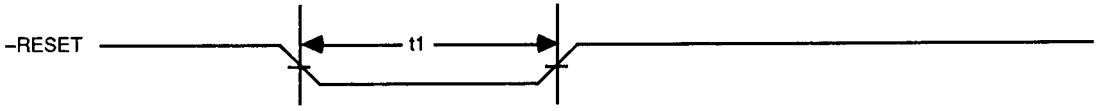
Note: –EOP, –IOR, and –DACK must be concurrently true for at least t5 for proper recognition of the –EOP pulse.



SWITCHING CHARACTERISTICS/WAVEFORMS (Cont.)

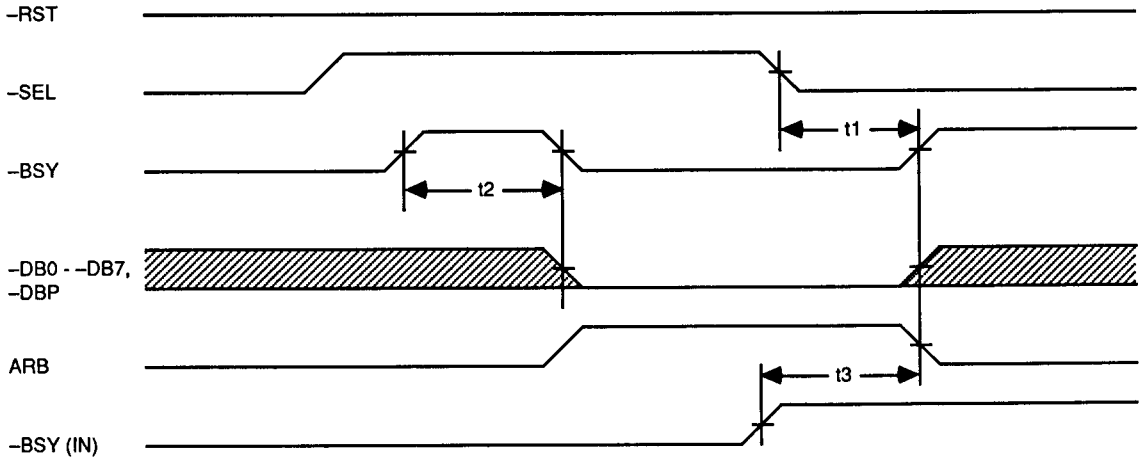
RESET

Symbol	Description	Min	Max	Units	Condition
t1	Minimum Width of Reset	200		ns	



ARBITRATION

Symbol	Description	Min	Max	Units	Condition
t1	Bus Clear from -SEL True		600	ns	
t2	Arbitrate Start from -BSY False	1200	2200	ns	
t3	Bus Clear from -BSY False		1100	ns	



ABSOLUTE MAXIMUM RATINGS

Ambient Operating Temperature	0°C to +70°C
Storage Temperature	–65°C to +150°C
Supply Voltage to Ground Potential	+6 V
Applied Input Voltage	–0.6 V to VCC +0.6 V
Power Dissipation	0.8 W

Stresses above those listed may cause permanent damage to the device. These are stress ratings only, functional operation of this device at these or any other conditions above those indicated in this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS: TA = 0°C to +70°C, VCC = 5 V ±5%

Symbol	Parameter	Min	Max	Units	Condition
VIH	High Level Input Voltage	2.0	5.25	V	
VIL	Low Level Input Voltage	–0.3	0.8	V	
IIH	High Level Input Current on:				VIH = 5.25 V, VIL = 0
	SCSI Bus Pins		50	µA	
	All Other Pins		10	µA	
IIL	Low Level Input Current on:				VIH = 5.25 V, VIL = 0
	SCSI Bus Pins		–50	µA	
	All Other Pins		–10	µA	
VOH	High Level Output Voltage	2.4		V	VDD = 4.75 V, IOH = –3.0 mA
VOL	Low Level Output Voltage on:				
	SCSI Bus Pins		0.5	V	VDD = 4.75 V, IOL = 48.0 mA
	All Other Pins		0.5	V	VDD = 4.75 V, IOL = 7.0 mA