APPLICATION NOTE
Upgrading From MK5025 to MK50H25

by Darin Kincaid

The MK50H25 is a pin for pin replacement for the MK5025 with additional features and performance enhancements. Options such as on-chip watch dog timers and pass through of bad CRCs are available by programming previously unused status register bits. It is important to note that even with the added options, the functionality and pin out of the MK5025 and MK50H25 are identical and the designer should not experience any difficulty or change of software substituting the MK50H25 for any revision of MK5025. Changes to software or hardware should only be required if some of the new features of the MK50H25 are to be used. The MK50H25 product has all the features of the older MK5025 with the following additions:

1. Optional 5 SYSCLK DMA cycle selectable by CYCLE bit in CSR2, in addition to the standard MK5025 type DMA cycle. This allows for better DMA performance and better bus utilization.

2. Optional Extended Initialization Block to allow use of a 16-bit timer prescaler. (selectable by EIBEN bit in CSR2).

3. Optional separate Abort Frames received error counter which will count received aborted frames separate from received frames with bad CRC (enabled by FCSER bit in IADR+16).

4. Optional Transmit Hold-off mechanism (enabled by XHOLD bit in CSR4) which will hold off the transmitter from transmitting the start of a frame until a XHOLD watermark in the Transmit FIFO has been reached.

5. Option to allow received frames to be DMA'ed to memory aligned to odd-byte boundaries (enabled by ROBA bit in CSR4). This feature can facilitate the process of stripping odd-byte headers off of received frames, so that the data following the header will be even-byte aligned in memory.

6. Optional TCLK and RCLK Watchdog Timers to facilitate detection of the disconnection of a cable or a line break in which data clocks are lost. (Selectable by bits 11-15 in CSR4).

7. Option to pass through the entire CRC to memory for received good or bad frames. (CRC Pass through is enabled by FCSEN bit and bad frame reception enabled by RBFCS bit, both in IADR+16.)

8. Independently selectable Receive Interrupt Disable selectable by bit RINTD in IADR+16. (this is in addition to the TINTD option that already exixted on the MK5025).

MK50H25 B01 Changes vs MK50H25 A07/A09 & MK5025 C04

1. The MK50H25 B01 fixes a problem when the MK5025 C04 is used in transparent mode for receiving data chaining (i.e. received frame spans multiple buffers), the MCNT value written by the MK5025 C04 to the descriptor(s) of the chained-on buffers will be a positive value, not 2's complement. (The MK5025 C03 and the MK50H25 B01 writes all MCNT values in 2's complement, as documented in the Data Sheet.) NOTE: This action only occurs in Transparent mode with receive data chaining.

2. There is a glitch on the MK50H25 B01 /HOLD output at the point in time that the DAL0-15 I/O pins transition from tri-state to active at the beginning of a DMA transfer. This glitch has been significantly reduced from what it was on the MK50H25 A07 and A09 revisions, but is still more than is seen on a MK5025 C04.

3. The MK50H25 B01 Self Test contains more internal tests than the Self Test of the MK5025 C04 because of the aditional features of the MK50H25 that are tested, but the MK50H25 B01 Self Test will return to the device to the same state upon completion as does the MK5025 C04 Self Test. NOTE: The MK5025 C04 and MK50H25 B01 have different internal firmware, so a clock by clock (SYSCLK) timing comparison of the same basic operations (i.e. data transmission and reception, self test, etc) will not be the exactly the same between the two devices, but the devices will meet the data sheet timing.

Differences Between MK50H25 A07, A09, and B01 Revisions

Attached are two Errata Sheets. One is the MK50H25 A07 Errata, and the other is the MK50H25 A09 Errata. If you compare these two Errata sheets, you will see that items 1 - 5 on the A07 Errata were fixed on the A09 device. The MK50H25 B01 device fixed item 1 and made significant improvements on item 2 of the revision A09 device.

The items that were fixed in the MK50H25 B01 are as follows:

1. The MK50H25 problem of corrupting the first word of a 65 or 66 byte frame to be transmitted when attempting to transmit that 65 or 66 byte frame immediately after transmitting any frame larger than 64 bytes with XHOLD enabled and FIFO Watermark (FWM) setting of 9 words.

2. The MK50H25 glitch on the /HOLD output at the point in time that the DAL0-15 I/O pins transition from tri-state to active at the beginning of a DMA transfer, has been significantly reduced from what it was on the A07 and A09 revisions.

3. The MK50H25 firmware was modified so that the state of the device when completing Self Test would be equivalent to that of the MK5025 upon completing Self Test, for backward compatibility.

The items that were fixed in the MK50H25 A09 are as follows:

1. The T1 timer in MK50H25 A07 may inadvertently be started in Transparent Mode, although no explicit primitive was issued to cause this action. The expiry of T1 will then cause an unexpected Provider Primitive 8 to be issued by the MK50H25

2. In Protocol Mode (X.25, etc.), the MK50H25 A07 will give a MISS indication (if no buffers are available) for a frame received while in a Local Busy state. It should just ignore the frame
received while in Local Busy.

3. In Protocol Mode (X.25, etc.), the MK50H25 A07 T1 timer is stopped upon reception of a good I frame in Remote Busy state. It should keep T1 going to keep polling with RR/P=1 until a RR is received rather than an RNR or I frame back from the remote end.

4. The MK50H25 A07 in 5 cycle DMA Burst mode with receive data chaining has the potential of writing data one word beyond the end of the current buffer boundary before chaining the next Rx buffer.

5. The Receive FIFO of the MK50H25 A07 has been determined to have a possible problem of corruption of the first word (2 bytes) of received data in a received frame under the conditions described in item 5 of the MK50H27 A07 Errata Sheet.

MK50H25 A09 ERRATA
November 1996

The following is a list of differences in operation between the MK50H25 Revision A09 and the information in the MK50H25 Technical Manual. Since the XHOLD function is not available on the MK5025, Errata point 1 is not applicable to those directly converting applications from the MK5025 to the MK50H25.

1. The MK50H25 exhibits a problem corrupting the first word of a 65 or 66 byte frame to be transmitted when attempting to transmit that 65 or 66 byte frame immediately after transmitting any frame larger than 64 bytes with XHOLD enabled and FIFO Watermark (FWM) setting of 9 words. This problem occurs only with 65 & 66 byte frames when XHOLD is enabled and the FWM setting is 9 words. This problem will not be seen if XHOLD = 0, or if FWM is other than 9 words or for any other frame sizes.

Possible work-arounds:

a. Use a FWM setting other than 9 words.

b. Modify the driver software providing frames to the MK50H25 Transmit descriptor ring so that after writing the two's complement of 65 or 66 to the MCNT field in the descriptor ring it will wait until the OWNA bit has been cleared (OWNA=0) for the previous Tx descriptor. After verifying that the previous descriptor OWNA has been cleared, the OWNA bit of the descriptor for the 65 or 66 byte frame may be set to allow the MK50H25 to transmit that frame. This modification should allow the Tx FIFO to clear before the 65 or 66 byte frame begins to be loaded into it to be transmitted, and thus avoid the problem. (This work-around will work well for Protocol mode, but may not work in Transparent mode at slow data rates).

c. A similar work-around would be for the driver software to immediately set the DTX bit in CSR0 upon writing the two's complement of 65 or 66 to MCNT, and delay clearing DTX until after a time defined as follows:

Tdelay = (64 bytes x 8 bits/byte) / TCLK
where TCLK is Tx data rate in bits/sec

Setting DTX=1 will disable the transmitter so that it will not transmit any more frames after the one in progress. Waiting Tdelay before clearing DTX will allow the time necessary for the Tx FIFO to clear before the next Tx frame is loaded in to the FIFO to be transmitted, thus avoiding the problem. (This work-around will work for both Transparent and Protocol modes at any data rate)

d. Set XHOLD = 0.

2. The MK50H25 A09 may exhibit a glitch on the /HOLD output at the point in time that the DAL0-15 I/O pins transition from tri-state to active following the assertion of the HLDA input by the host processor

granting the bus to the MK50H25. The glitch will occur approximately 15-30 nS after the rising edge of SYSCLK. This glitch may have an amplitude as high as 2.4 V and a duration of as much as 4 nS depending upon board layout and device decoupling. This glitch should not create any problems in sytems that only sample the HOLD pin on the rising edge of SYSCLK. However, in systems that asynchronously monitor HOLD, this glich has the possiblity of causing the system to see it as a release of HOLD, which will in turn cause many problems due to an inadvertent early termination of a MK50H25 DMA cycle.

Sugessted solution:

a. Synchronously sample HOLD on the rising edge of SYSCLK

MK50H25 A07 ERRATA
October 1995

The following is a list of differences in operation between the MK50H25 Revision A07 and the expected operation of the MK50H25.

1. The T1 timer may inadvertently be started in Transparent Mode, although no explicit primitive was issued to cause this action. The expiry of T1 will then cause an unexpected Provider Primitive 8 to be issued by the MK50H25

2. In Protocol Mode (X.25, etc.), the MK50H25 will give a MISS indication (if no buffers are available) for a frame received while in a Local Busy state. It should just ignore the frame received while in Local Busy.
3. In Protocol Mode (X.25, etc.), the MK50H25, T1 timer is stopped upon reception of a good I frame in Remote Busy state. It should keep T1 going to keep polling with RR/P=1 until a RR is received rather than an RNR or I frame back from the remote end.

4. The MK50H25 in 5 cycle DMA Burst mode with receive data chaining has the potential of writing data one word beyond the end of the current buffer boundary before chaining on the next receive buffer.

5. The Receive FIFO of the MK50H25 A07 has been determined to have a possible problem of corruption of the first word (2 bytes) of received data in a received frame. If the corruption in question extends to the internal RX FIFO "tag bits" associated with the first word of received frame data, the first word can be seen by the firmware as being a good or bad end of frame which will cause it to be treated as if it were a separate frame of 1 or 2 bytes (only 2 bytes written into the receive buffer), with the next descriptor buffer containing the remaining data of that received frame. If the problem occurs, it will only occur when a frame is received while the RX FIFO is empty. Because the problem is due to the RX FIFO, it will occur regardless of DMA burst setting, but will be seen externally only as corrupted data written into the receive buffer. Due to its nature, this problem does not occur in all devices, and if seen, it tends to occur in those devices processed to obtain higher operating speeds (i.e. 33 MHz)

6. The MK50H25 exhibits a problem corrupting a 65 or 66 byte frame to be transmitted when attempting to transmit back to back 65 & 66 byte frames with XHOLD enabled and FIFO Watermark (FWM) setting of 9 words. This problem occurs only with 65 & 66 byte frames when XHOLD is enabled and the FWM setting is 9 words. This problem will not be seen if XHOLD = 0, or if FWM is other than 9 words or for any other frame sizes.

Product Change Notice
September 10, 1996

By the end of 1996 we will upgrade the MK5025 family to 0.8 micron CMOS technology MK50H25Q product that gives higher performance and more operating options. The MK50H25 is qualified for production by SGS-Thomson.

If samples are needed to confirm the MK50H25Q16 operation, please notify your SGS-Thomson sales representative.

Differences - new MK50H25 Rev A09 and old MK5025 Rev C03 or C04
The MK50H25 product has all the features of the older MK5025 with the following additions:
We've increased the MK5025 on-chip ROM address space to 6K bits on the MK50H25 to add more operating options. Options such as on-chip watch dog timers and pass through of bad CRCs are available by programming previously unused status register bits. It is important to note that with the added options the functionality and pin out of the MK5025 and MK50H25 are identical and the designer should not experience any difficulty or change of software substituting the MK50H25Q16 for any revision of MK5025Q10 .

Transparent Mode
The MK50H25Q16 operates in the transparent mode identically to the MK5025Q. It is capable of faster data rates and up to 16 MHz SYSCLK rates. Verifying this information in actual applications will insure a smooth upgrade program for the customer.

Protocol Mode
There is no erratum known to exist between MK5025 Rev C03, C04 and MK50H25 protocols.

Deliveries
MK50H25Q Rev A09 samples are available for final approval to complete this qualification effort. Our plan is to upgrade all deliveries from MK5025 Rev C03 or Rev C04 to MK50H25Q16 by the end of December 1996.

Product Change Notice
March 11, 1996

In September of 1996 we will upgrade the entire MK5025 family to 0.8 micron CMOS technology MK50H25Q product that gives higher performance at lower cost. The operation of the MK50H25Q16 should be as good or better than the MK5025Q10 you currently use. However, If applications assistance is needed please advise. The MK50H25 has been qualified for production by SGS-Thomson.

Enclosed with this letter are 5 samples of the MK50H25Q16 to begin the upgrade of the older MK5025Q10 or MK5021Q10 used by your company.

Differences - new MK50H25Q16 Rev A09 vs old MK5025 Rev C03 or C04
The MK50H25 product has all the features of the older MK5025 with the following additions:
We've increased the MK5025 on-chip ROM address space to 6K bits on the MK50H25 to add more operating options. Options such as on-chip watch dog timers and pass through of bad CRCs are available by programming previously unused status register bits. It is important to note the functionality and pin out of the MK5025 and MK50H25 is identical. For verification of data, enclosed is a Technical Manual for the MK50H25.

Transparent Mode
The MK50H25Q16 operates in the transparent mode identically to the MK5025Q10. It is capable of faster data rates and SYSCLK rates. Verifying this information in actual applications will insure a smooth upgrade program

Protocol Mode
The MK50H25Q16 continues to support the protocols found in Rev C04 (MK5025Q10/09). The older MK5025 Rev C03 does not support GOSIP but the Rev C04 and MK50H25 Rev A09 does.

Deliveries
MK50H25 Rev A09 production will begin phase in immediately to customers approving the samples. We will complete the upgrade of all customers by October 1, 1996 and only MK50H25 product will be shipping by years' end.

Order Part Number
MK50H25Q16. Please specify Rev A09 at the time of ordering.