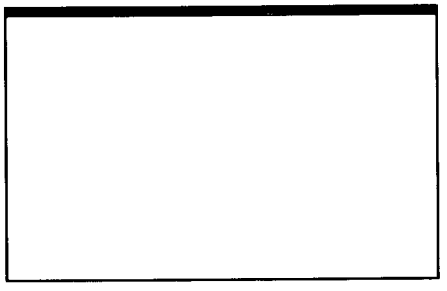
DYMEC

A Subsidiary of
SILICON TRANSISTOR CORP.

MODEL

3520

Wideband, Fast-settling Operational Amplifier



Description

Featuring a full differential input, 450MHz gain-bandwidth product, and a 325V/µs slew rate, the **Model 3520** FET input operational amplifier is specifically designed for conditioning of wideband data signals and pulses. A single compensation capacitor allows the performance of the amplifer to be tailored to the application by optimizing the bandwidth, slew rate or settling time. With a ±10V step settling time of 250ns to ±0.01% and a ±50mA output current drive at ±10V, the **3520** is a logical choice for use in video instrumentation, radar processing, high-speed test equipment, pulse amplifiers and data conversion products.

Stability over temperature for offset is ±20µV/°C with ±2mV maximum initial offset voltage. Input bias current is 100pA maximum. Open loop gain is 100dB, and common mode rejection is 85dB.

Physically, the **3520** utilizes thin-film hybrid and laser-trimming technology which permits precision tracking and tight control over dc parameters, and which produces the initial performance that is then guaranteed for the device. The completed amplifier is packaged in a 14-pin DIL ceramic case. Operating temperature for rated performance of the **3520** in this configuration is 0°C to +70°C.

Features

- ☐ **Fast Settling Time**
  250ns to 0.01%, ±10V step
- ☐ **High Slew Rate**
  325V/µs
- ☐ **450MHz Gain-Bandwidth Product**
- ☐ **High Output Drive Capacity**
  ±50mA at ±10V
- ☐ **Low Offset Drift**
  ±20µV/°C
- ☐ **Convenient Package**
  14-pin ceramic DIL

Applications

- ☐ **Video Instrumentation**
- ☐ **Radar Signal Processing**
- ☐ **High-speed Test Equipment**
- ☐ **Pulse Amplifiers**
- ☐ **Fast A/D and D/A Converters**
- ☐ **Sample-and-Hold Amplifiers**

Specifications

All Specifications Guaranteed at 25°C Unless Otherwise Noted

Analog Input

Input Voltage Range

Common Mode Voltage

±10V minimum, ±12V typical

Maximum Differential Voltage

±20V minimum, ±22V typical

Common Mode Rejection

74dB minimum, 85dB typical

Input Offset Voltage (V_{os})

±1.0mV typical, ±2.0mV maximum; after 5 minutes warm-up; nulling input offset will change tempco by 3µV/°C/mV of nulled offset

Input Bias Current (I_{bias})

10pA typical, 100pA maximum

Input Offset Current

2pA typical, 20pA maximum

Input Impedance (Differential)

$10^{10}\Omega$ || 5pF

Input Impedance (Common Mode)

$10^{10}\Omega$ || 5pF

Input Voltage Noise

100nV/√Hz, F_o= 1Hz to 20Hz

Open-Loop Gain

100dB typical, R_L=2KΩ

Dynamic Response

Gain-Bandwidth Product

___MHz minimum, 450MHz typical; C_c=0, A_{cl}=1000

Small Signal Unity Gain

___MHz minimum, 80MHz typical; C_c=10pF, A_{cl}=-1

Full Power Bandwidth

5MHz minimum; V_{in}=±10V

Slew Rate

300V/µs minimum, 325V/µs typical

Settling Time

65ns typical, 70ns maximum, to 1%, 10V step;
120ns typical, 130ns maximum, to 0.1%, 10V step;
200ns typical, 250ns maximum, to 0.01%, 10V step

Rated Output

Output Voltage

±10.5V minimum, with R_L=200Ω

Output Current

±50mA minimum, ±55mA typical; short circuit protected to ground

Impedance, Open-Loop

50Ω, nominal

Maximum Capacitive Load

50pF maximum

Stability

Offset Voltage - Drift

±20µV/°C typical, ±50µV/°C maximum

Offset Voltage - PS Sensitivity

1mV/V maximum

Input Bias Current (I_{bias}) Drift

Doubles every 10°C

Power Requirements

Rated Performance

+15V, ±3%

18mA typical (quiescent)

-15V, ±3%

18mA typical (quiescent)

Operating

±12V to ±18V

Environmental & Mechanical

Rated Performance

0°C to+70°C

Storage Temperature Range

-55°C to +125°C

$\theta_{junction\text{-}ambient}$

140°C/W typical

Dimensions

0.810" x 0.500" x 0.215" seated height maximum
(20.57 x 12.70 x 5.46 mm)

Package

14-pin ceramic

Grounding (continued)

power returns, as well as reducing stray signal pick up. The ground plane should connect all areas of the pattern side of the printed circuit board that are not otherwise used for signal, control or power conductors.

Each of the power supply leads should be bypassed to ground as near to the amplifier pins as possible using a parallel combination of 10µF tantalum and 0.1µF ceramic capacitors.

To obtain a good signal ground in inverting applications, the non-inverting input (pin 4) should be grounded, rather than being connected to a bias compensating resistor. An offset error will result, but due to the low resistor values used and the small bias current, the error will be minimal.

Single-point grounding is recommended if a ground plane is not used, or if point-to-point wiring techniques are employed. The input signal, load and power supply returns should all be connected at the same physical point. This will eliminate any common current or ground loops, and will in turn eliminate unwanted signal modulation, feedback or oscillations.

Compensation

An external frequency compensation capacitor is used to optimize the bandwidth, slew rate or settling time of the **3520** for a particular application. The primary compensation capacitor C_C is connected between pins 10 and 12. Typical values bewteen 0pF and 10pF are recommended, with lower values required for

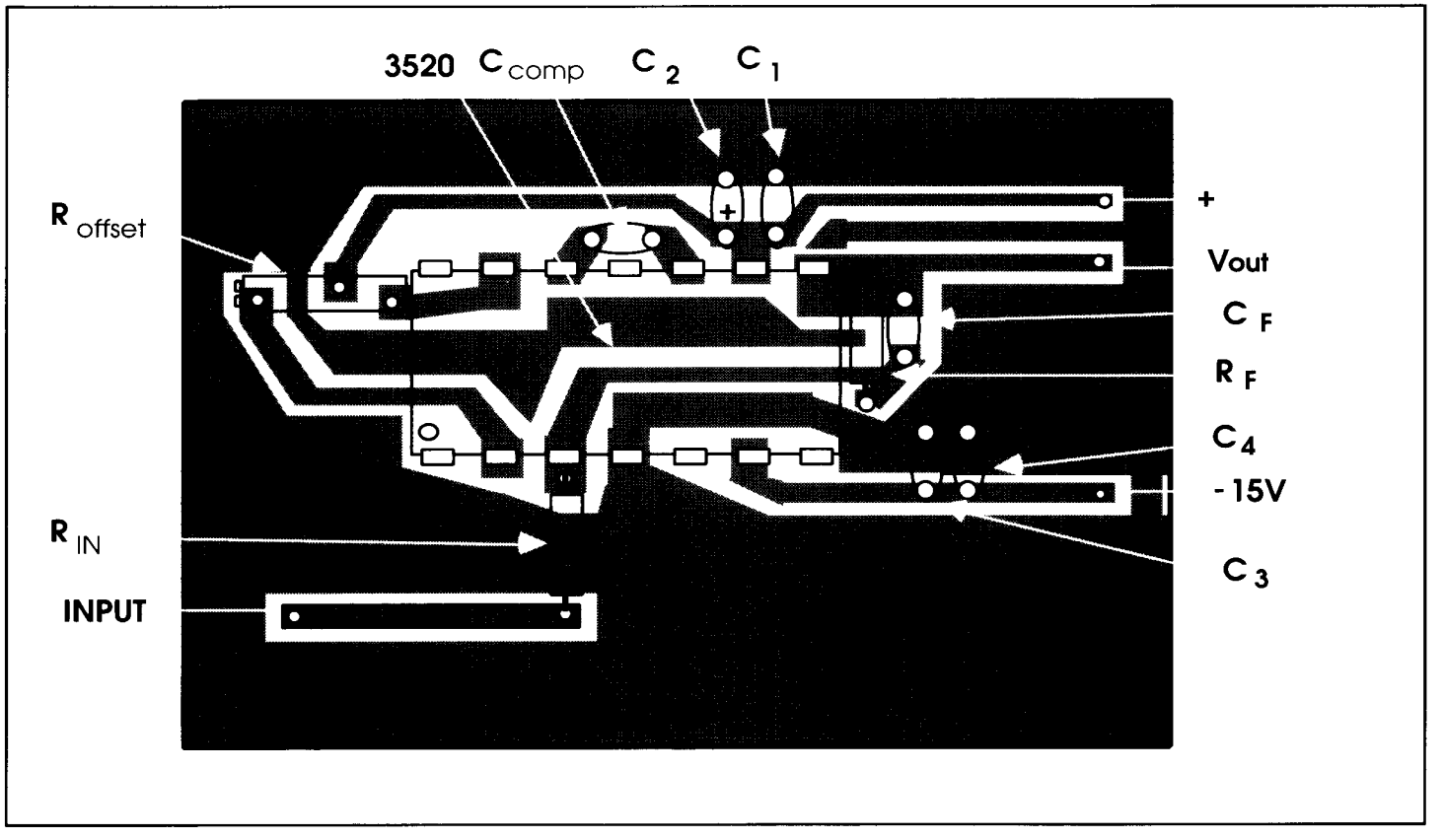


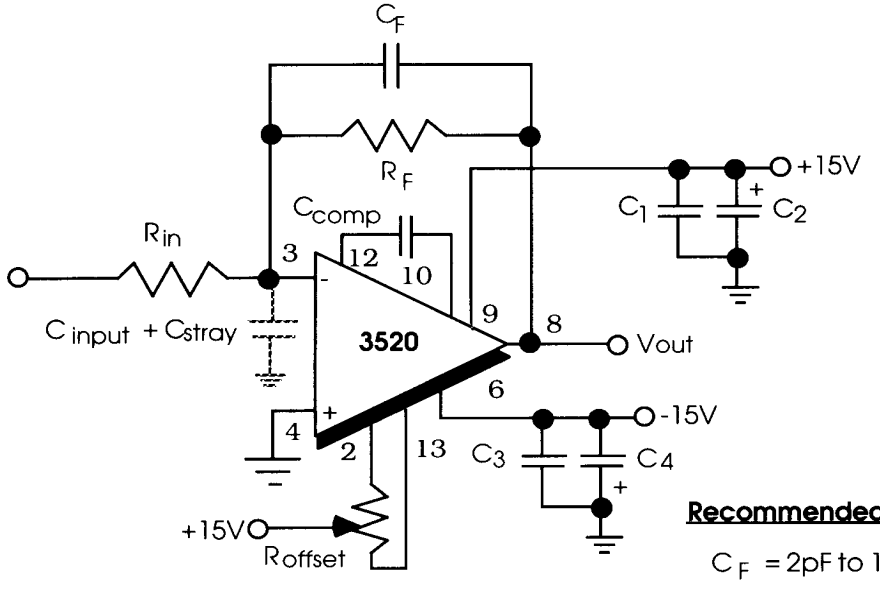
Figure 2. Typical Printed Circuit Board Layout

Layout Precautions

Because the **3520** has a gain-bandwidth product approaching 500MHz, it is imperative that high frequency techniques be used when laying out the circuit if the full performance of the amplifier is to be obtained. Of all wiring precautions, grounding is the most important; please refer to the section on grounding that follows. The mechanical layout of the circuit is also critical. All component leads and signal traces should be as short as possible, especially those connected to the inverting input (pin 3). Wide printed circuit board conductors should be used to provide low resistance, low inductance connections; these should be as short as possible. In general, the entire circuit should occupy as small an area as possible. Stray capacitances should be minimized, especially at high impedance nodes such as the input terminals of the amplifier. Stray signal coupling from the output to the input or to the offset null pins should be minimized. Use low resistor values, typically less than 5.6KΩ, such that the time constants formed with the circuit capacitances will not limit the performance of the amplifier.

Grounding

A ground plane and good grounding techniques should be used with the **3520** as with all high frequency circuits. The ground plane provides a low resistance, low inductance, common return path for all signal and



Recommended Component Values

C_F = 2pF to 10pF = C_{input} + C_{stray}

C_{comp} = 0pF to 10pF

C_1 , C_3 = 0.1µF ceramic

C_2 , C_4 = 10µF Tantalum

R_{offset} = 10KΩ, linear pot.

Figure 1. Typical Circuit Configuration and Recommended Component Values

larger closed-loop gains. At a closed-loop gain of 1000, no compensation capacitor is required.

The combination of input and stray capacitances and input and feedback resistances will form a zero that will affect the frequency response of the circuit. A small (2pF to 5pF) capacitor across the feedback resistance (C_F) equal to the sum of C_{input} and C_{stray} will compensate for this zero. The capacitance value is dependent on the closed-loop gain and circuit layout.

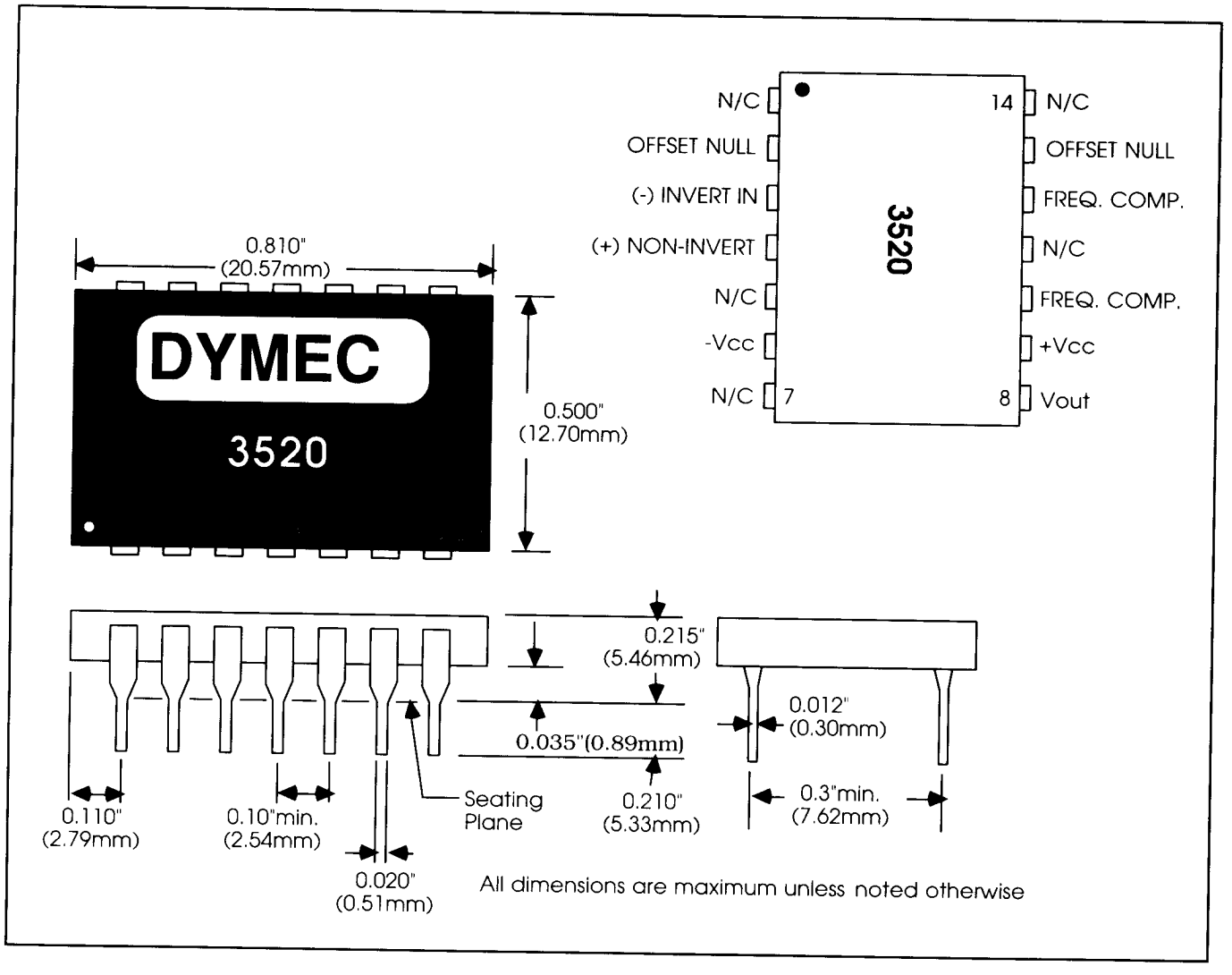
Short Circuit Protection

The **3520** output is short circuit protected to ground. Damage may result if any of the compensation or offset null pins are shorted to either ground or the negative supply. To avoid damage, do not plug in or remove the **3520** from the circuit with power applied.

Offset Voltage Adjustment

The offset voltage of the **3520** may be adjusted to zero by connecting a 10KΩ linear potentiometer between pins 2 and 13, with the wiper connected to the positive power supply. The leads connecting the potentiometer to the amplifier pins should be extremely short to avoid stray capacitance and stray signal pick-up. To prevent oscillation, stray coupling from the output to either input pin should be avoided. For each microvolt of offset voltage adjusted, the offset voltage temperature drift will change by ±0.003μV/°C.

Mechanical Dimensions & Pinout



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Printed in U.S.A.

8 Lowell Avenue ☐ Winchester, MA 01890 ☐ 800-225-1151
(617) 729-7870 ☐ TWX: (710) 348-6596

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