

# M64897GP

## PLL Frequency Synthesizer with DC/DC Converter for PC

REJ03F0167-0200

Rev.2.00

Jun 14, 2006

### Description

The M64897GP is a semiconductor integrated circuit consisting of PLL frequency synthesizer for TV/VCR/PC using I<sup>2</sup>C BUS control. It contains the prescaler with operating up to 1.3 GHz, 4 band drivers and DC/DC converter for Tuning voltage.

### Features

- Built-in DC/DC converter for Tuning voltage
- 4 integrated PNP band drivers ( $I_O = 30 \text{ mA}$ ,  $V_{\text{sat}} = 0.2 \text{ V Typ.}@V_{\text{CC1}}$  to 10 V)
- Built-in prescaler with input amplifier ( $f_{\text{max}} = 1.3 \text{ GHz}$ )
- PLL lock/unlock status display out put (Built-in pull up resistor)
- X'tal 4 MHz is used to realize 3 type of tuning steps (Divider ratio 1/512, 1/640, 1/1024)
- Software compatible with M64894
- Built-in Power on reset system
- Small Package (SSOP)

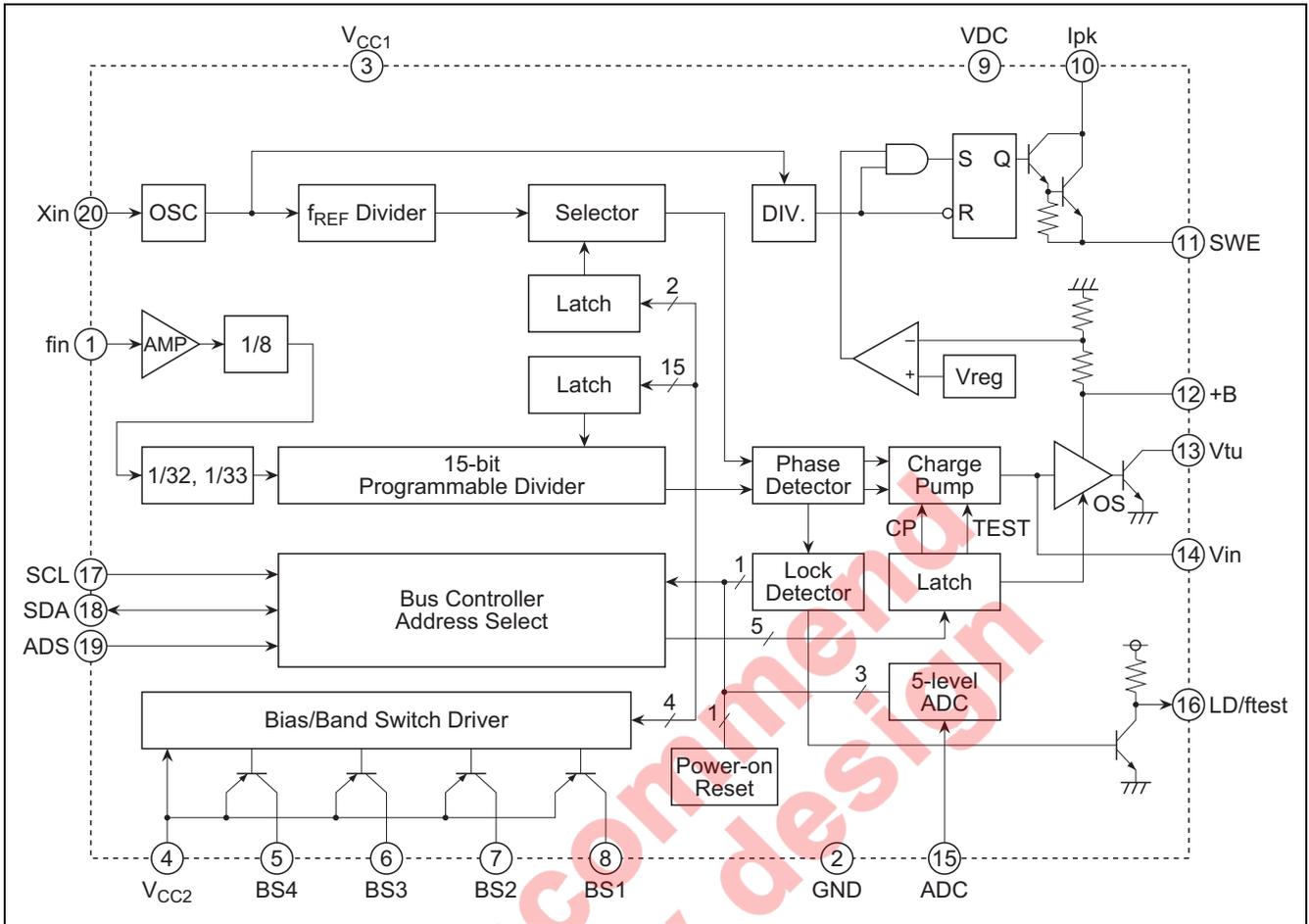
### Application

PC, TV, VCR tuners

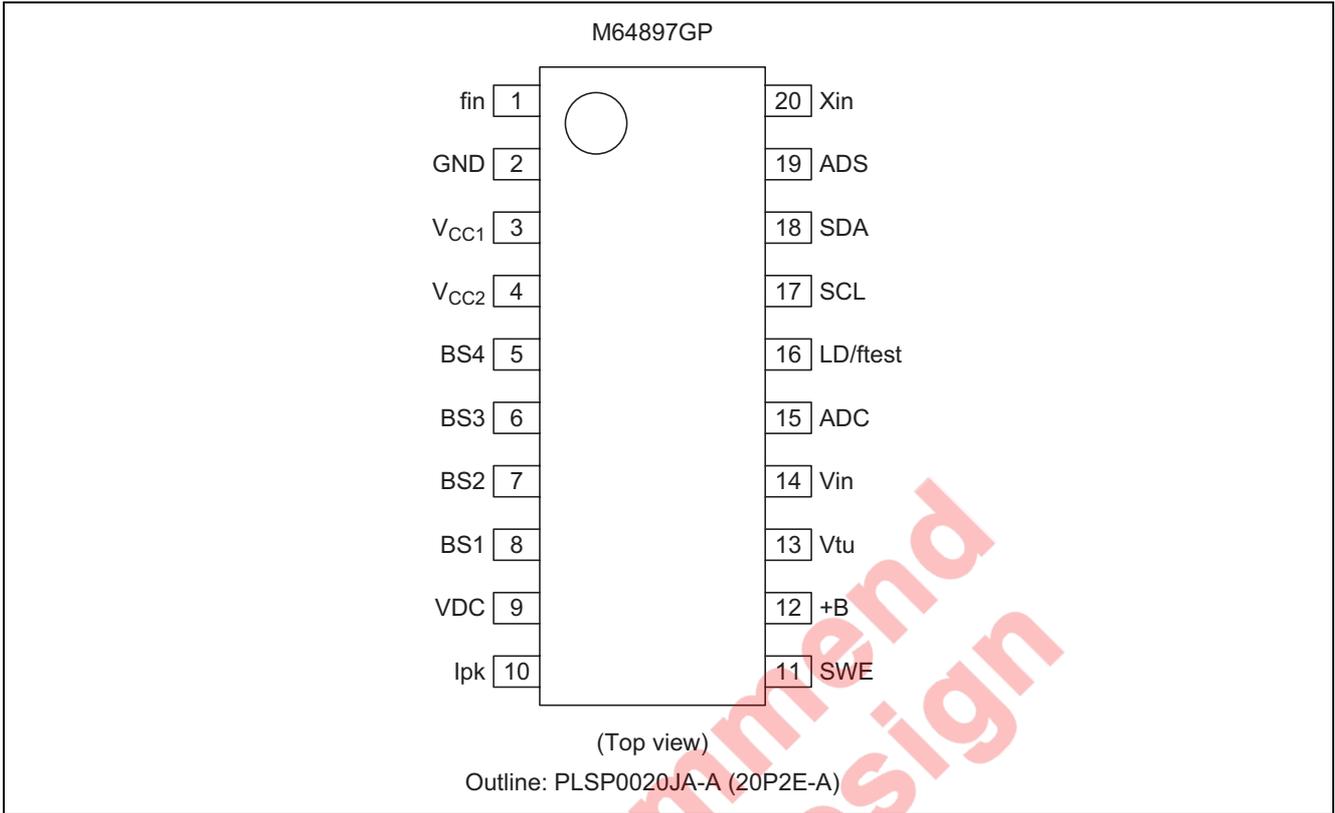
### Recommended Operating Condition

- Supply voltage range
  - $V_{\text{CC1}} = 4.5 \text{ to } 5.5 \text{ V}$
  - $V_{\text{CC2}} = V_{\text{CC1}}$  to 10 V
- Rated supply voltage
  - $V_{\text{CC1}} = 5 \text{ V}$
  - $V_{\text{CC2}} = V_{\text{CC1}}$

Block Diagram



### Pin Arrangement



Not recommended for new design

## Pin Description

Pin No.	Symbol	Pin name	Function
1	fin	Prescaler input	Input for the VCO frequency.
2	GND	GND	Ground to 0 V.
3	V <sub>CC1</sub>	Power supply voltage 1	Power supply voltage terminal. 5.0 V ± 0.5 V
4	V <sub>CC2</sub>	Power supply voltage 2	Power supply for band switching, V <sub>CC1</sub> to 10 V
5	BS4	Band switching outputs	PNP open collector method is used. When the band switching data is "H", the output is ON. When it is "L", the output is OFF.
6	BS3		
7	BS2		
8	BS1		
9	VDC	DC/DC power supply voltage	DC/DC power supply voltage terminal. 5.0 V ± 0.5 V
10	lpk	Peak current detect	When potential difference with VDC terminal becomes more than 0.33 V by current limiting detector of DC/DC converter, the listing rises with off.
11	SWE	Switching output	DC/DC converter oscillator output.
12	+B	Power supply voltage	Power supply voltage for tuning voltage.
13	Vtu	Tuning output	This supplies the tuning voltage.
14	Vin	Filter input (Charge pump output)	This is the output terminal for the LPF input and charge pump output. When the phase of the programmable divider output (f 1/N) is ahead compared to the reference frequency (f <sub>REF</sub> ), the "source" current state becomes active. If it is behind, the "sink" current becomes active. If the phases are the same, the high impedance state becomes active.
15	LD/ftest	Lock detect/Test port	Lock detector output. When loop of phase locked loop locked it, it rises with "H" level in "L" level or unlock. In control byte data input, the programmable freq. divider output and reference freq. output is selected by the test mode.
16	ADC	AD converter input	A/D conversion of the input voltage.
17	SCL	Clock input	Data is read into the shift register when the clock signal falls..
18	SDA	Data input	Input for band SW and programmable freq. divider set up. In lead mode, it outputs lock detector output and power down flag and a state of 5 level A/D converter.
19	ADS	Address switching input	Chip address sets it up with the input condition of terminal.
20	Xin	This is connected to the crystal oscillator	4.0 MHz crystal oscillator is connected.

## Absolute Maximum Ratings

(Ta = -20°C to +75°C, unless otherwise noted)

Item	Symbol	Ratings	Unit	Condition
Supply Voltage 1	V <sub>CC1</sub>	6.0	V	Pin 3
Supply voltage 2	V <sub>CC2</sub>	10.8	V	Pin 4
Input voltage	V <sub>I</sub>	6.0	V	Not to exceed V <sub>CC1</sub>
Output voltage	V <sub>O</sub>	6.0	V	f <sub>REF</sub> output
Voltage applied when the band output is OFF	V <sub>B<sub>SOFF</sub></sub>	10.8	V	
Band output current	I <sub>B<sub>SON</sub></sub>	40.0	mA	Per 1 band output circuit
ON the time when the band output is ON	t <sub>B<sub>SON</sub></sub>	10	s	40 mA per 1 band output circuit 3 circuits are pn at same time.
Power dissipation	P <sub>d</sub>	255	mW	Ta = 75°C
Operating temperature	T <sub>opr</sub>	-20 to +75	°C	
Storage temperature	T <sub>stg</sub>	-40 to +125	°C	

## Recommended Operating Conditions

(Ta = -20°C to +75°C, unless otherwise noted)

Item	Symbol	Ratings	Unit	Conditions
Supply voltage 1	V <sub>CC1</sub>	4.5 to 5.5	V	Pin 3
Supply voltage 2	V <sub>CC2</sub>	V <sub>CC1</sub> to 10.0	V	Pin 4
Operating frequency (1)	f <sub>opr1</sub>	4.0	V	Crystal oscillation circuit
Operating frequency (2)	f <sub>opr2</sub>	80 to 1300	MHz	
Band output current 5 to 8	I <sub>BDL</sub>	0 to 30	mA	Normally 1 circuit is on. 2 circuits on at the same time is max. It is prohibited to have 3 or more circuits turned on at the same time.

## Electrical Characteristics

(Ta = -20°C to +75°C, unless otherwise noted, V<sub>CC1</sub> = 5.0 V, V<sub>CC2</sub> = 9.0 V)

Item	Symbol	Test Pin	Limits			Unit	Test Conditions	
			Min.	Typ.	Max.			
Input terminals	"H" input voltage	V <sub>IH</sub>	17 to 18	3.0	—	V <sub>CC1</sub> + 0.3	V	
	"L" input voltage	V <sub>IL</sub>	17 to 18	—	—	1.5	V	
	"H" input current	I <sub>IH</sub>	17 to 18	—	—	10	μA	V <sub>CC1</sub> = 5.5V, V <sub>i</sub> = 4.0V
	"L" input current	I <sub>IL</sub>	17, 18	—	-4/-14	-10/-30	μA	V <sub>CC1</sub> = 5.5V, V <sub>i</sub> = 0.4V
SDA output	"L" output voltage	V <sub>OL</sub>	18	—	—	0.4	μA	V <sub>CC1</sub> = 5.5V, I <sub>c</sub> = 3mA
	Leak current	I <sub>LO</sub>	18	—	—	10	μA	V <sub>CC1</sub> = 5.5V, V <sub>O</sub> = 5.5V
Lock output	"H" output voltage	V <sub>OH</sub>	16	5.0	—	—	V	V <sub>CC1</sub> = 5.5V
	"L" output voltage	V <sub>OL</sub>	16	—	0.3	0.5	V	V <sub>CC1</sub> = 5.5V
Band SW	Output voltage	V <sub>BS</sub>	5 to 8	11.6	11.8	—	V	V <sub>CC2</sub> = 9V, I <sub>o</sub> = -30mA
	Leak current	I <sub>olk1</sub>	5 to 8	—	—	-10	μA	V <sub>CC2</sub> = 9V, Band SW is OFF V <sub>O</sub> = 0V
Tuning output	Output voltage "H"	V <sub>toH</sub>	13	30.5	—	—	V	+B = 31V
	Output voltage "L"	V <sub>toL</sub>	13	—	0.2	0.4	V	+B = 31V
Charge pump	"H" output current	I <sub>CPO</sub>	14	—	270	370	μA	V <sub>CC1</sub> = 5.0V, V <sub>O</sub> = 2.5V
	Leakage current	I <sub>CPLK</sub>	14	—	—	50	nA	V <sub>CC1</sub> = 5.0V, V <sub>O</sub> = 2.5V
Supply current 1	I <sub>CC1</sub>	3	—	20	30	mA	V <sub>CC1</sub> = 5.5V	
Supply current 2	4 circuits OFF	I <sub>CC2A</sub>	4	—	—	0.3	mA	V <sub>CC2</sub> = 9V
	1 circuits ON, Output open	I <sub>CC2B</sub>	4	—	4.0	6.0	mA	V <sub>CC2</sub> = 9V
	Output current 30 mA	I <sub>CC2C</sub>	4	—	34.0	36.0	mA	V <sub>CC2</sub> = 9V, I <sub>o</sub> = -30mA
DC/DC Converter								
Supply current (action)	I <sub>CCdc</sub>	9	—	1.3	3.0	mA	V <sub>CC1</sub> = 5.5V	
Output voltage	V <sub>do</sub>	12	28	31	35	V	V <sub>CC1</sub> = 5.5V	
OSC frequency	f <sub>OSC</sub>	11	—	571	—	kHz	V <sub>CC1</sub> = 5.5V	
Current limit detect voltage	V <sub>ipk</sub>	10	—	330	—	mV	V <sub>CC1</sub> = 5.5V	

Note: The typical values are at V<sub>CC1</sub> = 5.0 V, V<sub>CC2</sub> = 9.0 V, Ta = +25°C.

## Switching Characteristics

( $T_a = -20^{\circ}\text{C}$  to  $+75^{\circ}\text{C}$ , unless otherwise noted,  $V_{CC1} = 5.0\text{ V}$ ,  $V_{CC2} = 9.0\text{ V}$ )

Item	Symbol	Test Pin	Limits			Unit	Test Conditions	
			Min.	Typ.	Max.			
Prescaler operating frequency	$f_{opr}$	1	80	—	1300	MHz	$V_{CC1} = 4.5$ to $5.5\text{V}$ $V_{in} = V_{inmin}$ to $V_{inmax}$	
Operation input voltage	$V_{in}$	1	-24	—	4	dBm	$V_{CC1} = 4.5$ to $5.5\text{V}$	850 to 100MHz
			-27	—	4			100 to 950MHz
			-15	—	4			950 to 1300MHz
Clock pulse frequency	$f_{SCL}$	17	0	—	100	kHz	$V_{CC1} = 4.5$ to $5.5\text{V}$	
Bus free time	$t_{BUF}$	18	4.7	—	—	$\mu\text{s}$	$V_{CC1} = 4.5$ to $5.5\text{V}$	
Data hold time	$t_{HDSTA}$	17	4	—	—	$\mu\text{s}$	$V_{CC1} = 4.5$ to $5.5\text{V}$	
SCL low hold time	$t_{LOW}$	17	4.7	—	—	$\mu\text{s}$	$V_{CC1} = 4.5$ to $5.5\text{V}$	
SCL high hold time	$t_{HIGH}$	17	4	—	—	$\mu\text{s}$	$V_{CC1} = 4.5$ to $5.5\text{V}$	
Set up time	$t_{SUSTA}$	17, 18	4.7	—	—	$\mu\text{s}$	$V_{CC1} = 4.5$ to $5.5\text{V}$	
Data hold time	$t_{HDDAT}$	17, 18	0	—	—	s	$V_{CC1} = 4.5$ to $5.5\text{V}$	
Data set up time	$t_{SUDAT}$	17, 18	250	—	—	ns	$V_{CC1} = 4.5$ to $5.5\text{V}$	
Rise time	$t_R$	17, 18	—	—	1000	ns	$V_{CC1} = 4.5$ to $5.5\text{V}$	
Fall time	$t_F$	17, 18	—	—	300	ns	$V_{CC1} = 4.5$ to $5.5\text{V}$	
Set up time	$t_{SUSTO}$	17, 18	4	—	—	$\mu\text{s}$	$V_{CC1} = 4.5$ to $5.5\text{V}$	

Not recommended  
for new designs

### Method of Setting Data

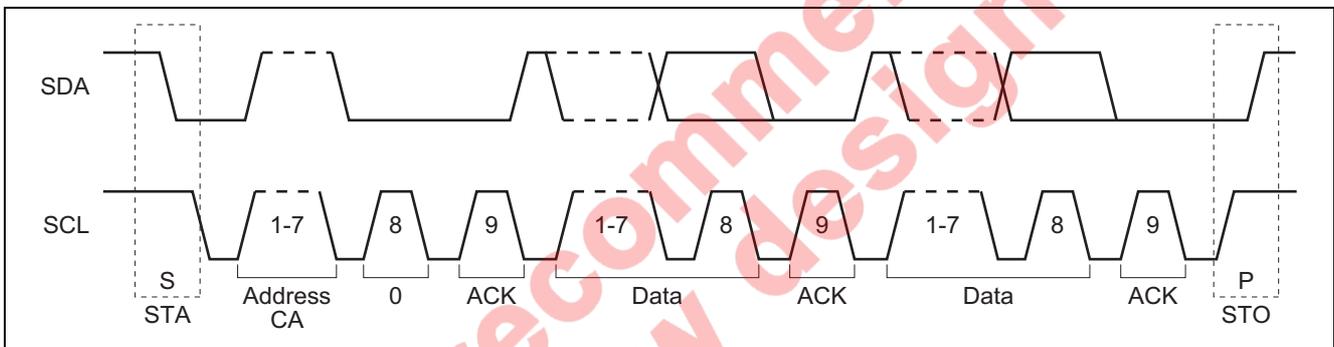
The input information to consist of 2 or data of 4 bytes to lead to chip address is received in I<sup>2</sup>C bus receiver. It shows a definition of bus protocol admitted in the following.

1_STA	CA	CB	BB	STO		
2_STA	CA	D1	D2	STO		
3_STA	CA	CB	BB	D1	D2	STO
4_STA	CA	D1	D2	CB	BB	STO

- STA : Start condition
- STO : Stop condition
- CA : Chip address
- CB : Control data byte
- BB : Band SW data byte
- D1 : Divider data byte
- D2 : Divider data byte

The information of 5 bytes necessary for circuit operation is chip address and control data, band SW data of 2 bytes and divider byte of 2 bytes. After the chip address input, 2 or data of 4 bytes are received.

Function bit is contained the first and the third data byte to distinguish between divider data and control data, band data, and "0" goes ahead of divider data, and "1" goes ahead of control data, band SW data.



### Write Mode Format

Byte	MSB								LSB
Address byte	1	1	0	0	0	MA1	MA0	0	A
Divider byte 1	0	N14	N13	N12	N11	N10	N9	N8	A
Divider byte 2	N7	N6	N5	N4	N3	N2	N1	N0	A
Control byte 1	1	X	T2	T1	T0	RSa	RSb	OS	A
Band SW byte	X	X	X	X	BS4	BS3	BS2	BS1	A

### Read Mode Format

Byte	MSB								LSB
Address byte	1	1	0	0	0	MA1	MA0	1	A
Status byte 1	POR	FL	X	X	X	A2	A1	A0	A

## Data Cording Example

### Write Mode Format Example

Byte	MSB								LSB	Condotion in Data Setting
Address byte	1	1	0	0	0	1	1	0	1	ADS input $V_{CC1}$
Divider byte 1	0	1	0	0	0	0	0	0	1	Divider ratio $N = 16544$
Divider byte 2	1	0	1	0	0	0	0	0	1	
Control byte 1	1	1	0	0	0	0	1	0	1	$f_{REF}$ divider ratio 1/1024
Band SW byte	0	0	0	0	1	0	0	0	1	BS4 output ON

Note:  $f_{VCO} = N \cdot 8 \cdot f_{REF} = 16544 \cdot 8 \cdot (4 \text{ MHz}/1024) = 517 \text{ MHz}$

### Read Mode Format Example (Loop locked)

Byte	MSB								LSB	Condotion in Data Setting
Address byte	1	1	0	0	0	1	1	1	1	ADS Applied voltage $0.9 V_{CC1}$ to $V_{CC1}$
Status byte	0	1	1	1	1	0	1	1	1	ADS Applied voltage $0.45 V_{CC1}$ to $0.6 V_{CC1}$

Use data input for "1" so that the data of Read mode and Write mode return ACK signal "0" to micro computer in 9 bits of each byte.

## Test Mode Data Set Up Method

### Test Mode Bit Set Up

X : Random, 0 or 1. normal "0"

MA1, MA0 : Programmable address bit

Address Input Voltage	MA1	MA0
0 to $0.1 V_{CC1}$	0	0
Always valid	0	1
$0.4 V_{CC1}$ to $0.6 V_{CC1}$	1	0
$0.9 V_{CC1}$ to $V_{CC1}$	1	1

Note: N14 to N0: How to set dividing ratio of the programmable the divider

$$\text{Dividing ratio} = N14 (2^{14} = 16384) + \dots + N0 (2^0 = 1)$$

Therefore, the range of divider N is 1,024 to 32,768

$$\text{Example) } f_{VCO} = f_{REF} \cdot 8 \cdot N$$

$$= 3.90625 \cdot 8 \cdot N$$

$$= 31.25 \cdot N \text{ (kHz)}$$

### T2, T1, T0: Setting Up for The Test Mode

T2	T1	T0	Charge Pump	Pin 12 Condition	Mode
0	0	X	Normal operation	ADC input	Normal operation
0	1	X	High impedance	ADC input	Test mode
1	1	0	Sink	ADC input	Test mode
1	1	1	Source	ADC input	Test mode
1	0	0	High impedance	$f_{REF}$ output	Test mode
1	0	1	High impedance	$f1/N$ output	Test mode

**RSa, RSb: Set Up for The Reference Frequency Divider Ratio**

RSa	RSb	Divider Ratio
1	1	1/512
0	1	1/1024
X	0	1/640

**OS: Set Up The Tuning Amplifier**

OS	Tuning Voltage Output	Mode
0	ON	Normal
1	OFF	Test

POR : Power on reset flag. "1" output at reset

FL : Lock detector flag. "1" output at locked, "0" output at unlocked

**A2, A1, A0: 5 Level A/D Converter Output Data**

ADC Input Voltage	A2	A1	A0
$0.6 \pm V_{CC1}$ to $V_{CC1}$	1	0	0
$0.45 \pm V_{CC1}$ to $0.6 \pm V_{CC1}$	0	1	1
$0.3 \pm V_{CC1}$ to $0.45 \pm V_{CC1}$	0	1	0
$0.15 \pm V_{CC1}$ to $0.3 \pm V_{CC1}$	0	0	1
0 to $0.15 \pm V_{CC1}$	0	0	0

Note: The voltage accuracy allowance range:  $0.03 \pm V_{CC1}$  (V)

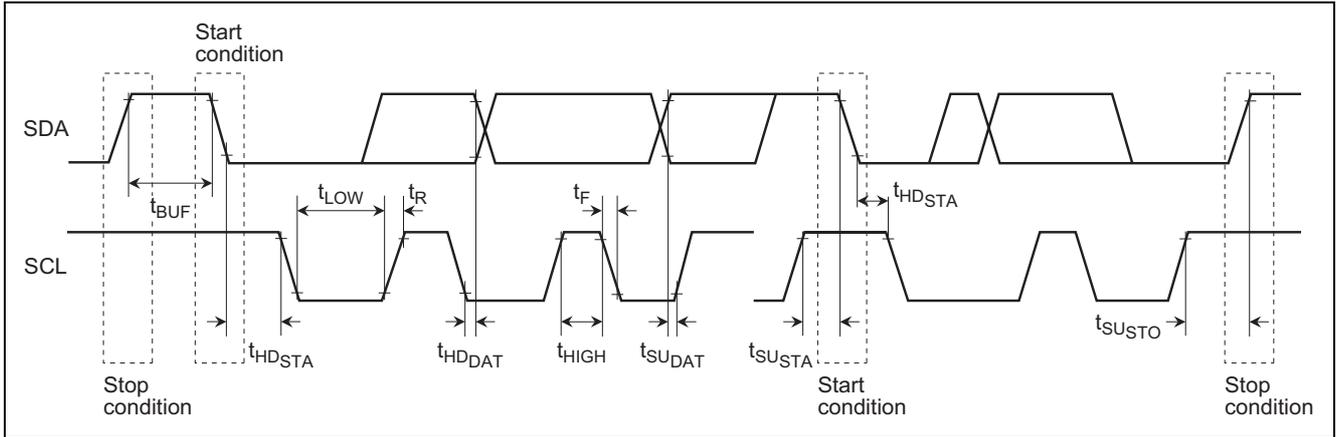
**Power on Reset Operation**

(Initial state the power is turned ON)

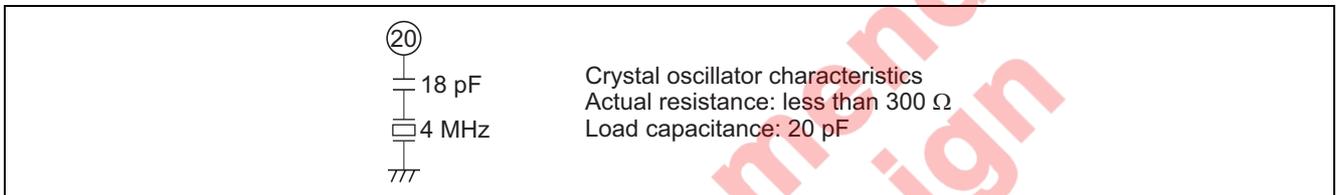
BS4 to BS1 : OFF  
 Charge pump : High impedance  
 Tuning amplifier : OFF  
 Charge pump current : 270  $\mu$ A  
 Frequency division ratio : 1/1024  
 Lock detect : H

Charge pump current is replaced by 70  $\mu$ A when locks it by automatic change facility.

### Timing Diagram

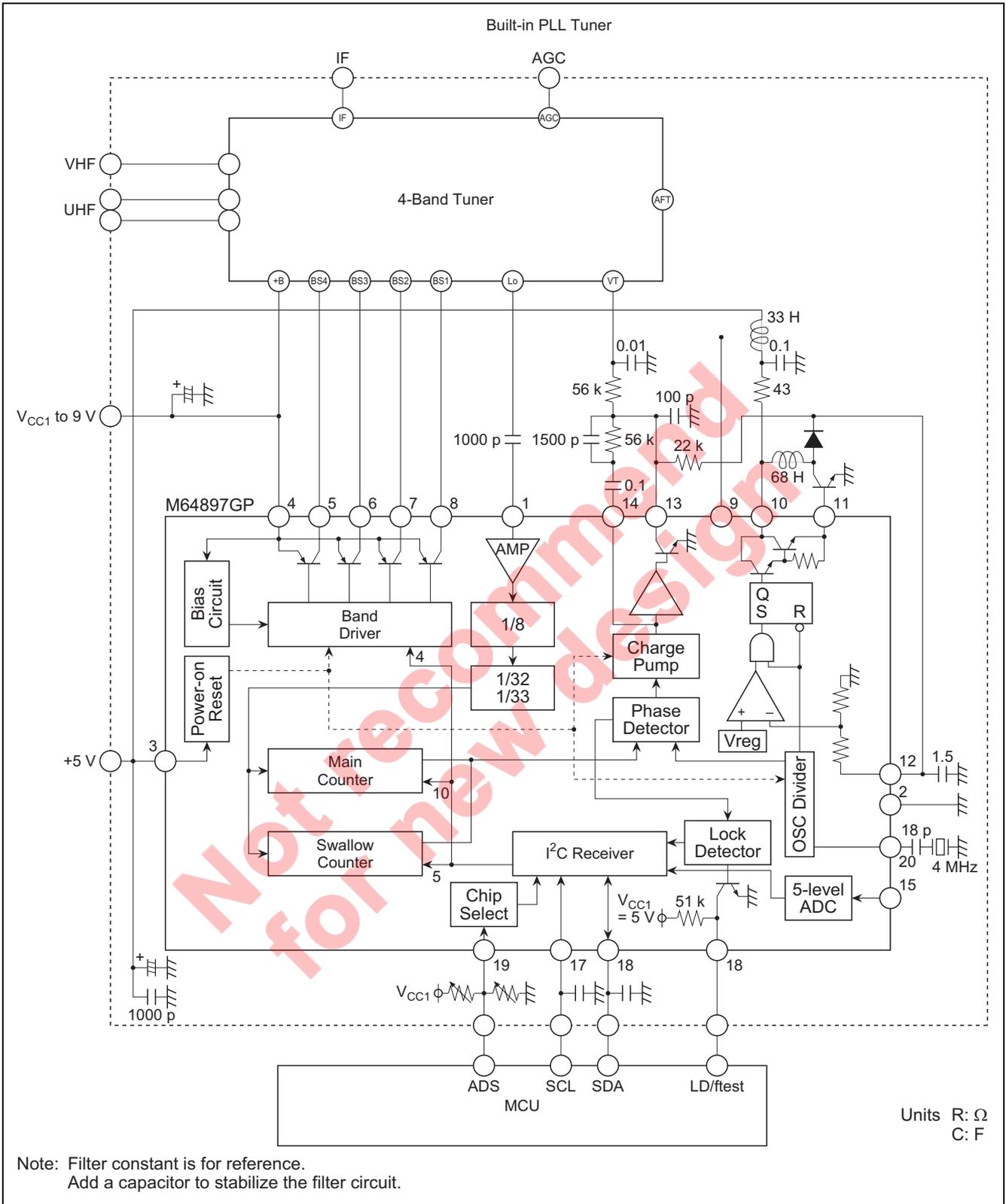


### Crystal Oscillator Connection Diagram



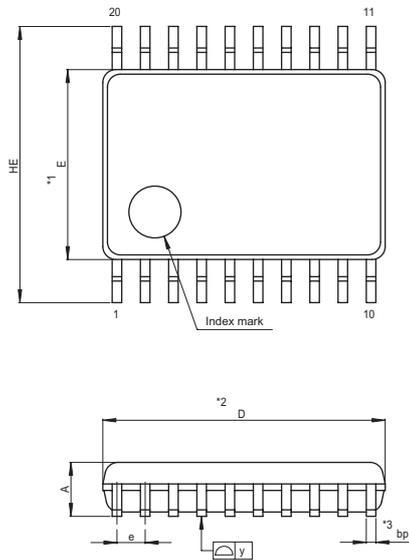
Not recommended for new design

Application Example



Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LSSOP20-4.4x6.5-0.65	PLSP0020JA-A	20P2E-A	0.08g



NOTE)  
 1. DIMENSIONS  $1^*$  AND  $2^*$  DO NOT INCLUDE MOLD FLASH.  
 2. DIMENSION  $3^*$  DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	6.4	6.5	6.6
E	4.3	4.4	4.5
$A_2$	—	1.15	—
A	—	—	1.45
$A_1$	0	0.1	0.2
$b_p$	0.17	0.22	0.32
c	0.13	0.15	0.2
$\theta$	0°	—	10°
$H_E$	6.2	6.4	6.6
e	0.53	0.65	0.77
y	—	—	0.10
L	0.3	0.5	0.7

Not recommended for new design

Keep safety first in your circuit designs!

1. Renesas Technology Corp. puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage. Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

Notes regarding these materials

1. These materials are intended as a reference to assist our customers in the selection of the Renesas Technology Corp. product best suited to the customer's application; they do not convey any license under any intellectual property rights, or any other rights, belonging to Renesas Technology Corp. or a third party.
2. Renesas Technology Corp. assumes no responsibility for any damage, or infringement of any third-party's rights, originating in the use of any product data, diagrams, charts, programs, algorithms, or circuit application examples contained in these materials.
3. All information contained in these materials, including product data, diagrams, charts, programs and algorithms represents information on products at the time of publication of these materials, and are subject to change by Renesas Technology Corp. without notice due to product improvements or other reasons. It is therefore recommended that customers contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor for the latest product information before purchasing a product listed herein.  
The information described here may contain technical inaccuracies or typographical errors.  
Renesas Technology Corp. assumes no responsibility for any damage, liability, or other loss rising from these inaccuracies or errors.  
Please also pay attention to information published by Renesas Technology Corp. by various means, including the Renesas Technology Corp. Semiconductor home page (<http://www.renesas.com>).
4. When using any or all of the information contained in these materials, including product data, diagrams, charts, programs, and algorithms, please be sure to evaluate all information as a total system before making a final decision on the applicability of the information and products. Renesas Technology Corp. assumes no responsibility for any damage, liability or other loss resulting from the information contained herein.
5. Renesas Technology Corp. semiconductors are not designed or manufactured for use in a device or system that is used under circumstances in which human life is potentially at stake. Please contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor when considering the use of a product contained herein for any specific purposes, such as apparatus or systems for transportation, vehicular, medical, aerospace, nuclear, or undersea repeater use.
6. The prior written approval of Renesas Technology Corp. is necessary to reprint or reproduce in whole or in part these materials.
7. If these products or technologies are subject to the Japanese export control restrictions, they must be exported under a license from the Japanese government and cannot be imported into a country other than the approved destination.  
Any diversion or reexport contrary to the export control laws and regulations of Japan and/or the country of destination is prohibited.
8. Please contact Renesas Technology Corp. for further details on these materials or the products contained therein.



**RENESAS SALES OFFICES**

<http://www.renesas.com>

Refer to "<http://www.renesas.com/en/network>" for the latest and detailed information.

**Renesas Technology America, Inc.**

450 Holger Way, San Jose, CA 95134-1368, U.S.A  
Tel: <1> (408) 382-7500, Fax: <1> (408) 382-7501

**Renesas Technology Europe Limited**

Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.  
Tel: <44> (1628) 585-100, Fax: <44> (1628) 585-900

**Renesas Technology (Shanghai) Co., Ltd.**

Unit 204, 205, AZIACenter, No.1233 Lujiazui Ring Rd, Pudong District, Shanghai, China 200120  
Tel: <86> (21) 5877-1818, Fax: <86> (21) 6887-7898

**Renesas Technology Hong Kong Ltd.**

7th Floor, North Tower, World Finance Centre, Harbour City, 1 Canton Road, Tsimshatsui, Kowloon, Hong Kong  
Tel: <852> 2265-6688, Fax: <852> 2730-6071

**Renesas Technology Taiwan Co., Ltd.**

10th Floor, No.99, Fushing North Road, Taipei, Taiwan  
Tel: <886> (2) 2715-2888, Fax: <886> (2) 2713-2999

**Renesas Technology Singapore Pte. Ltd.**

1 Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632  
Tel: <65> 6213-0200, Fax: <65> 6278-8001

**Renesas Technology Korea Co., Ltd.**

Kukje Center Bldg. 18th Fl., 191, 2-ka, Hangang-ro, Yongsan-ku, Seoul 140-702, Korea  
Tel: <82> (2) 796-3115, Fax: <82> (2) 796-2145

**Renesas Technology Malaysia Sdn. Bhd**

Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No.18, Jalan Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia  
Tel: <603> 7955-9390, Fax: <603> 7955-9510