HM644332

2K Entry TAG Memory for Cache Sub System

The HM644332 TAGM is a 2048-entry tag memory fabricated with CMOS technology. It supports compact cache systems with 2-way or 4-way set associativity and a high level of performance for 32-bit microprocessor systems, when used together with fast static RAMs as data RAMs.

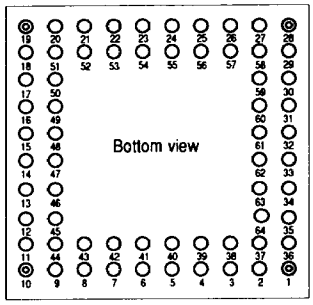
Features

- Programmable organization: 512-entry × 4-way or 1024-entry × 2-way
- Memory organization: 512 words × 98 bits
  98 bits = (20 tag bits + 1 parity bit + 2 validity bits) × 4 ways + 6 LRU bits
- Fast access time: 25/30 ns max from address inputs, 18 ns max from tag data inputs
- Single + 5 V supply
- TTL-compatible inputs and outputs
- LRU (least recently used) replacement algorithm
- Purge functions (all purge and partial purge)
- Internal parity generator/checker
- 64-pin pin-grid-array

Ordering Information

	Access Time		
Part No.	**From Address**	**From Tag Data**	**Package**
HM644332G-25	25 ns	18 ns	64-pin PGA
HM644332G-30	30 ns	18 ns	

Pin Arrangement

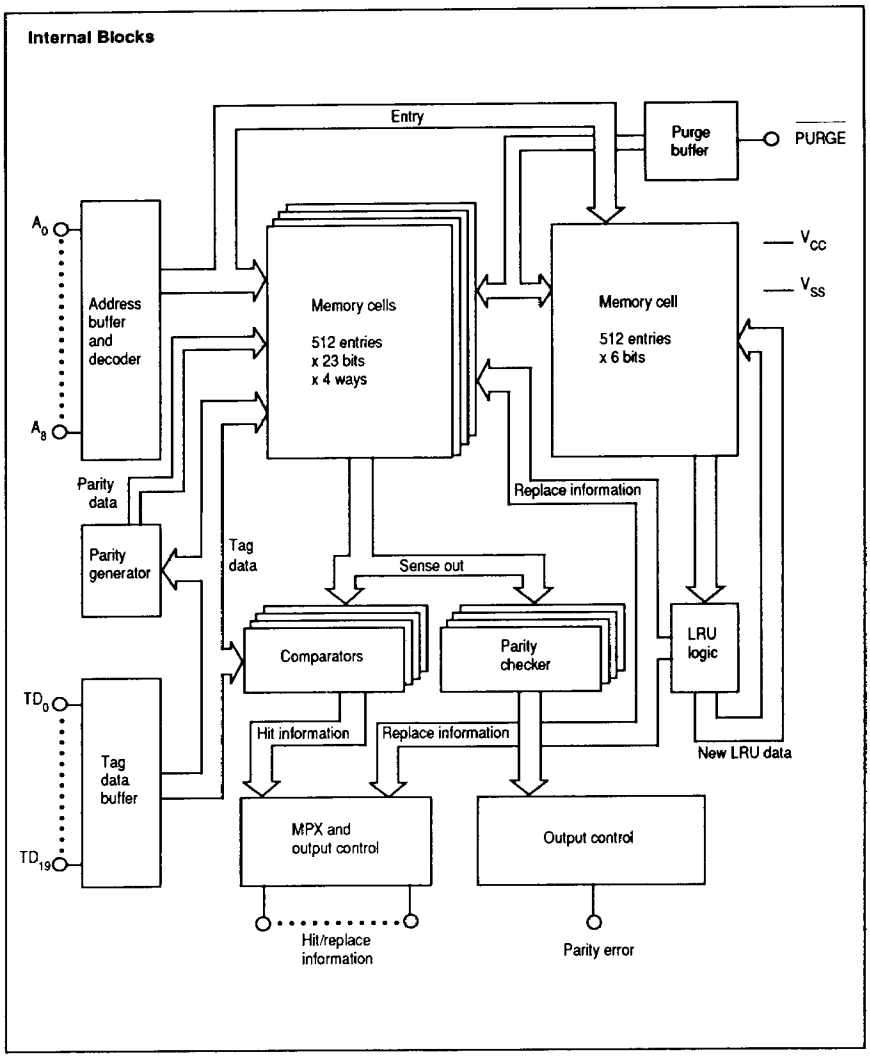


Pin No.	Function	Pin No.	Function	Pin No.	Function
1	N.C.	23	A_4	45	TD_6
2	$\overline{MHIT}$	24	A_5	46	TD_9
3	HIT_0/REP_0	25	A_7	47	V_{CC}
4	HIT_2/REP_2	26	A_9	48	TD_{13}
5	HIT_3/REP_3	27	N.C.	49	TD_{15}
6	TD_0	28	N.C.	50	TD_{17}
7	TD_2	29	$\overline{PINV}$	51	TD_{19}
8	EXTH	30	SBLK	52	A_0
9	MHENBL	31	SB_1	53	A_2
10	N.C.	32	$\overline{INH}$	54	V_{SS}
11	TD_7	33	$\overline{INVL}$	55	A_6
12	TD_8	34	$\overline{SET}$	56	A_8
13	TD_{10}	35	H/$\overline{R}$	57	$\overline{PURGE}$
14	TD_{11}	36	$\overline{HIT}$	58	MODE
15	TD_{12}	37	$HC_0/\overline{RC_0}$	59	$\overline{VINV}$
16	TD_{14}	38	$HC_1/\overline{RC_1}$	60	SB_0
17	TD_{16}	39	HIT_1/REP_1	61	V_{CC}
18	TD_{18}	40	V_{SS}	62	$\overline{WRITE}$
19	N.C.	41	TD_1	63	RLATCH
20	N.C.	42	TD_3	64	$\overline{PERR}$
21	A_1	43	TD_4		
22	A_3	44	TD_5		

Pin Description

Symbol	Pin Name	Pin No.	I/O	Function
MODE	Mode	58	I	Mode selection MODE = H: 512-entry x 4-way MODE = L: 1024-entry x 2-way
A_0–A_9	Address	52, 21, 53, 22, 23, 24, 55, 25, 56, 26	I	Address inputs: A_9 is not used for 4-way; fix it to H or L
TD_0–TD_{19}	Tag Data	6, 41, 7, 42–45, 11, 12, 46, 13, 14, 15, 48, 16, 49, 17, 50, 18, 51	I	Tag information
$\overline{PURGE}$	Purge	57	I	All purge is done when $\overline{PURGE}$ = L
$\overline{INVL}$	Invalidate	33	I	Partial purge: V bit of specified address is forced to 0 (L)
SBLK	Way Select Enable	30	I	Enables external way selection in replacement and invalidation cycles
SB_0, SB_1	External Way Address	60, 31	I	External way address input: Enabled when SBLK = H
$\overline{WRITE}$	Write	62	I	Enables write
$\overline{SET}$	Set	34	I	Timing pulse Read cycle: Updates LRU Write cycle: Stores tag, sets V bits to H, and updates LRU Partial purge cycle: Shifts LRU and sets V bits to L
$\overline{INH}$	Inhibit	32	I	Inhibits all functions except all purge
H/R	Hit/Replace Selection	35	I	Output selection H/R = H: Hit information H/R = L: Replace information
RLATCH	Replace Latch	63	I	Latch control for replace information
$\overline{PINV}$	Parity Inversion	29	I	Used for testing only
$\overline{VINV}$	Validity Inversion	59	I	Used for testing only
MHENBL	$\overline{MHIT}$ Enable	9	I	Enables $\overline{MHIT}$ output
EXTH	External Hit Control	8	I	Forces $\overline{MHIT}$ output to L
$\overline{HIT}$	Hit	36	O	Hit output: NOR of HIT_0 to HIT_3
HC_0/RC_0 HC_1/RC_1	Hit/Replace Code	37, 38	O	Coded output of hit or replace information
HIT_0/REP_0– HIT_3/REP_3	Hit/Replace	3, 39, 4, 5	O	Uncoded output of hit or replace information
$\overline{PERR}$	Parity Error	64	O	Indicates parity error
$\overline{MHIT}$	Modified Hit	2	O	Hit output modified by MHENBL and EXTH
V_{CC}	Power	47, 61	I	Connects to + 5V power supply
V_{SS}	Ground	40, 54	I	Connects to ground

Block Diagrams



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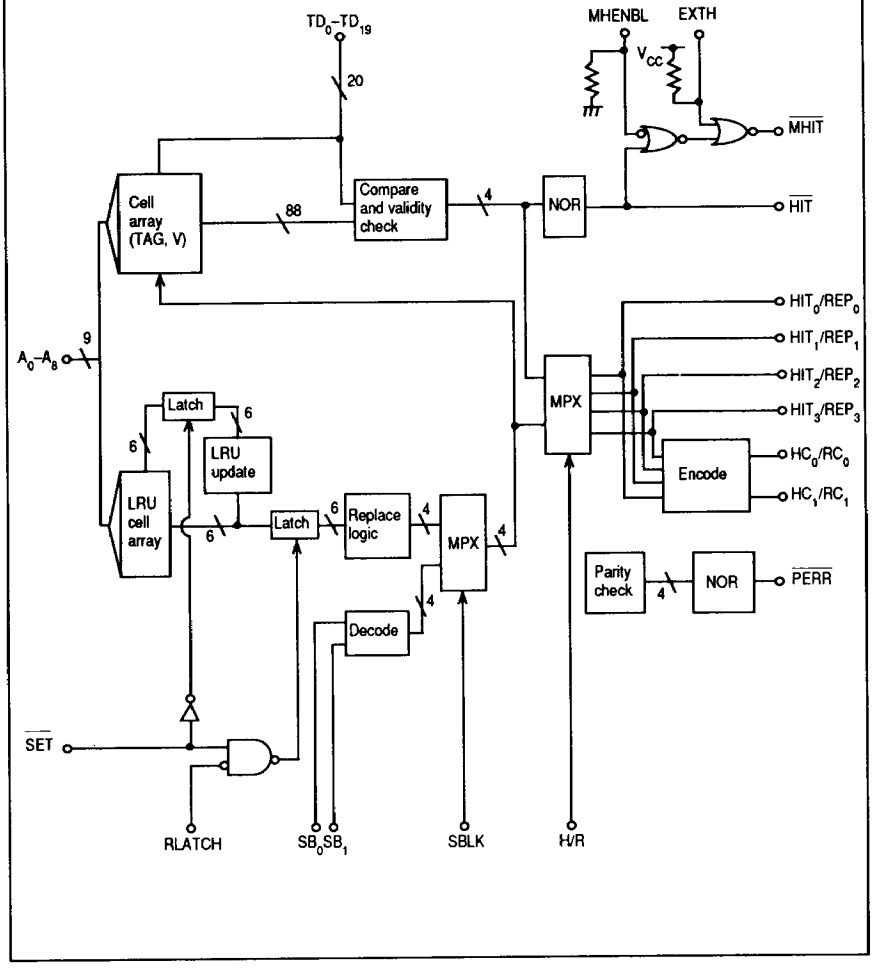
Output Control Block



Function Tables

1. Basic Functions (all combinations not listed below are inhibited)

Input					Tag Info.	Control Info.		LRU	
$\overline{INH}$	$\overline{PURGE}$	$\overline{SET}$	$\overline{WRITE}$	$\overline{INVL}$	Tag Bits	P Bit (Parity)	V Bits (Validity)	LRU Bits	Function Mode
L	H	×	×	×	No change	No change	No change	No change	Inhibit*3
H	H	H	×	×	No change	No change	No change	No change	Tag read
H	H	⊓	H	H	No change	No change	No change	No change*1 or updated	Tag read
H	H	⊓	L	H	TD_0–TD_{19}	Set	H	Updated	Tag write
×	L	H	×	×	Undefined	Undefined	L (All)	Initialized	All purge
H	H	⊓	H	L	No change	No change	No change L*2	No change*1 or shifted*4	Partial purge

×: H or L

Notes: *1 When SBLK = L and there is no hit, LRU is not changed.
*2 When SBLK = L and there is no hit, the V bits are not changed.
*3 In inhibit mode, HIT and PERR outputs are H but all other outputs are L.
*4 Shifted means that the partially-purged way becomes the least recently used way.

2. Hit or Replace Information Output

Input		Internal Information*1, *2				Output							
MODE	A_9	hit_0/ rep_0	hit_1/ rep_1	hit_2/ rep_2	hit_3/ rep_3	HIT_0/ REP_0	HIT_1/ REP_1	HIT_2/ REP_2	HIT_3/ REP_3	HC_0/ RC_0	HC_1/ RC_1	$\overline{HIT}$*3	Mode
H	×	L	L	L	L	L	L	L	L	L	L	H	4-way
H	×	H	L	L	L	H	L	L	L	L	L	L	
H	×	L	H	L	L	L	H	L	L	H	L	L	
H	×	L	L	H	L	L	L	H	L	L	H	L	
H	×	L	L	L	H	L	L	L	H	H	H	L	
L	L	L	×	L	×	L	L	L	L	L	L	H	2-way
L	L	H	×	L	×	H	L	L	L	L	L	L	
L	L	L	×	H	×	L	L	H	L	L	H	L	
L	H	×	L	×	L	L	L	L	L	L	L	H	
L	H	×	H	×	L	L	H	L	L	H	L	L	
L	H	×	L	×	H	L	L	L	H	H	H	L	

×: H or L

Notes: *1 Internal information rep_0 to rep_3 is determined by on-chip LRU logic when SBLK = L.
When SBLK = H, the internal information is determined by external signals SB_0 and SB_1.
*2 Correct operation is not guaranteed if 2 or more ways are hit at the same time.
*3 $\overline{HIT}$ output is valid when H/R = H.

3. Partial Purge ($\overline{INVL}$ = L)

Input					Internal Info.				Purged Way				$\overline{SET}$	
MODE	A_9	SBLK	SB_0	SB_1	hit_0	hit_1	hit_2	hit_3	0	1	2	3	LRU	Mode
H	×	L	×	×	L	L	L	L	—	—	—	—	No change	4-way
H	×	L	×	×	H	L	L	L	Q	—	—	—	Shifted	
H	×	L	×	×	L	H	L	L	—	Q	—	—	Shifted	
H	×	L	×	×	L	L	H	L	—	—	Q	—	Shifted	
H	×	L	×	×	L	L	L	H	—	—	—	Q	Shifted	
H	×	H	L	L	×	×	×	×	Q	—	—	—	Shifted	
H	×	H	H	L	×	×	×	×	—	Q	—	—	Shifted	
H	×	H	L	H	×	×	×	×	—	—	Q	—	Shifted	
H	×	H	H	H	×	×	×	×	—	—	—	Q	Shifted	
L	L	L	×	×	L	×	L	×	—	—	—	—	No change	2-way
L	L	L	×	×	H	×	L	×	Q	—	—	—	Shifted	
L	L	L	×	×	L	×	H	×	—	—	Q	—	Shifted	
L	L	H	L	L	×	×	×	×	Q	—	—	—	Shifted	
L	L	H	L	H	×	×	×	×	—	—	Q	—	Shifted	
L	H	L	×	×	×	L	×	L	—	—	—	—	No change	
L	H	L	×	×	×	H	×	L	—	Q	—	—	Shifted	
L	H	L	×	×	×	L	×	H	—	—	—	Q	Shifted	
L	H	H	H	L	×	×	×	×	—	Q	—	—	Shifted	
L	H	H	H	H	×	×	×	×	—	—	—	Q	Shifted	

Note: Correct operation is not guaranteed if 2 or more ways are hit at the same time.

4. Parity Error and V Bits*1

pen	vn_0	vn_1	PEn	Hit Info.*2 (n: 0 to 3)
L	L	L	L	—
L	L	H	H	Hit
L	H	L	H	Hit
L	H	H	L	Hit
H	L	L	L	—
H	L	H	H	Hit
H	H	L	H	Hit
H	H	H	H	Hit

pen: Internal parity error in way n
vn_0/vn_1: Duplicate validity bits.
PEn: Determined by the following equation:

$$PEn = (vn_0 + vn_1) \cdot pen + (vn_0 \oplus vn_1)$$

Notes: *1 $\overline{PERR}$ is the NOR of PE0 to PE3.
*2 Output information when internal hit is valid.

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Supply Voltage	V_{CC}	–0.5 to +7.0	V
Input Voltage at Any Pin Relative to V_{SS}	V_{in}	–3.0 to +7.0	V
Output Voltage at Any Pin Relative to V_{SS}	V_{out}	–0.5 to +7.0	V
Output Current	I_{out}	±20	mA
Power Dissipation	P_T	1.5	W
Operating Temperature	T_{opr}	–10 to +85	°C
Storage Temperature	T_{stg}	–65 to +125	°C

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended DC Operating Conditions (T_a = 0 to +70°C)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC} *1	4.5	5.0	5.5	V
Input Low Voltage	V_{IL} *1	–0.5 *2	—	0.8	V
Input High Voltage	V_{IH} *1	2.2	—	6.0	V

Notes: *1 All voltages are relative to V_{SS}.

*2 –3.0 V for pulse width of 20 ns or less.

DC and Operating Characteristics (T_a = 0 to +70°C, V_{CC} = 5 V ±10%, V_{SS} = 0 V)

Item	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Operating Power Supply Current	I_{CC}	Min. cycle, I_{out} = 0 mA	—	—	200	mA
		Cycle = 100 ns, I_{out} = 0 mA	—	—	180	mA
Input Leakage Current	I_{IL}	V_{in} = V_{SS} to V_{CC}	–10	—	10	µA
Output Voltage	V_{OL}	I_{OL} = 8 mA	—	—	0.4	V
	V_{OH}	I_{OH} = –4 mA	2.4	—	—	V

Capacitances (T_a = 25°C, f = 1 MHz)

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Input Capacitance	C_{in}	V_{in} = 0 V	—	—	10	pF
Output Capacitance	C_{out}	V_{out} = 0 V	—	—	TBD	pF

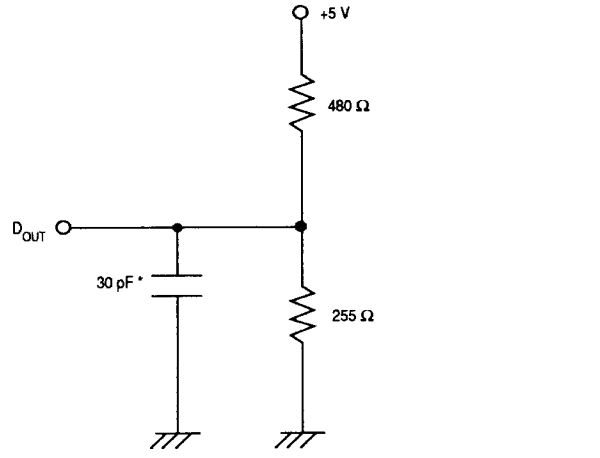
Note: These parameters are sampled, not 100% tested.

AC Characteristics (T_a = 0 to +70°C, V_{CC}= 5 V ±10%, V_{SS}=0V, unless otherwise noted)

AC Test Conditions

- Input pulse levels: 0 V to 3.0 V
- Input pulse rise and fall times: 0 ns to 5 ns (time between 0.8 V and 2.2 V)
- Input and output timing reference levels: 1.5 V
- Output load: See figure.

Output Load



*Including scope and jig

1. Tag Read Cycle (MODE = H or L, $\overline{\text{PURGE}}$ = H, $\overline{\text{WRITE}}$ = H, $\overline{\text{INVL}}$ = H, $\overline{\text{PINV}}$ = H or L, $\overline{\text{VINV}}$ = H or L, $\overline{\text{INH}}$ = H)

		HM644332G-25		HM644332G-30		
Item	Symbol	Min.	Max.	Min.	Max.	Unit
Read Cycle Time	t_{RC}	50	—	50	—	ns
Address Valid to $\overline{\text{HIT}}$, $\overline{\text{HC}}_n$, $\overline{\text{HIT}}_n$	t_{AH}	—	25	—	30	ns
Address Valid to $\overline{\text{MHIT}}$	t_{AMH}	—	27	—	32	ns
Tag Data Valid to $\overline{\text{HIT}}$, $\overline{\text{HC}}_n$, $\overline{\text{HIT}}_n$	t_{TH}	—	18	—	18	ns
Tag Data Valid to $\overline{\text{MHIT}}$	t_{TMH}	—	20	—	20	ns
$\overline{\text{HIT}}$, $\overline{\text{HC}}_n$, $\overline{\text{HIT}}_n$ Hold Time	t_{HH}	0	—	0	—	ns
Address Valid to $\overline{\text{RC}}_n$, $\overline{\text{REP}}_n$	t_{AR}	—	35	—	40	ns
Address Valid to $\overline{\text{PERR}}$	t_{AP}	—	35	—	40	ns
Address Setup Time for $\overline{\text{SET}}$	t_{AS}	25	—	25	—	ns
Tag Data Setup Time for $\overline{\text{SET}}$	t_{TS}	25	—	25	—	ns
$\overline{\text{SET}}$ Pulse Width	t_{SW}	20	—	20	—	ns
$\overline{\text{SET}}$ Recovery Time	t_{SR}	5	—	5	—	ns
RLATCH Setup Time	t_{RLS}	10	—	10	—	ns
$\overline{\text{RC}}_n$, $\overline{\text{REP}}_n$ Hold Time for RLATCH	t_{RH}	0	—	0	—	ns
SBLK, SB_0, SB_1 Setup Time for $\overline{\text{RC}}_n$, $\overline{\text{REP}}_n$	t_{SBR}	—	25	—	25	ns
SBLK, SB_0, SB_1 Hold Time	t_{SBH}	5	—	5	—	ns
$\overline{\text{RC}}_n$, $\overline{\text{REP}}_n$ Hold Time for SBLK, SB_0, SB_1	t_{SH}	0	—	0	—	ns
SBLK, SB_0, SB_1 Setup Time for $\overline{\text{SET}}$	t_{SBS}	25	—	25	—	ns
$\overline{\text{PERR}}$ Hold Time	t_{PH}	0	—	0	—	ns
H/R to Multiplex Output Change	t_{HR}	—	10	—	12	ns
MHENBL, EXTH to $\overline{\text{MHIT}}$ Output	t_{MMH}	—	10	—	12	ns

2. Tag Write Cycle (MODE = H or L, $\overline{PURGE}$ = H, $\overline{WRITE}$ = L, $\overline{INVL}$ = H, H/$\overline{R}$ = L, $\overline{INH}$ = H)

		HM644332G-25		HM644332G-30		
Item	Symbol	Min.	Max.	Min.	Max.	Unit
Write Cycle Time	t_{WC}	50	—	50	—	ns
Address Valid to RC_n, REP_n	t_{AR}	—	35	—	40	ns
Address Setup Time for $\overline{SET}$	t_{AS}	25	—	25	—	ns
Tag Data Setup Time for $\overline{SET}$	t_{TS}	25	—	25	—	ns
$\overline{SET}$ Pulse Width	t_{SW}	20	—	20	—	ns
$\overline{SET}$ Recovery Time	t_{SR}	5	—	5	—	ns
RLATCH Setup Time	t_{RLS}	10	—	10	—	ns
SBLK, SB_0, SB_1 Setup Time for $\overline{SET}$	t_{SBS}	25	—	25	—	ns
SBLK, SB_0, SB_1 Setup Time for RC_n, REP_n	t_{SBR}	—	25	—	25	ns
RC_n, REP_n Hold Time for SBLK, SB_0, SB_1	t_{SH}	0	—	0	—	ns
SBLK Hold Time	t_{SBH}	5	—	5	—	ns
$\overline{PINV}$, $\overline{VINV}$ Setup Time for $\overline{SET}$	t_{IS}	25	—	25	—	ns
$\overline{PINV}$, $\overline{VINV}$ Recovery Time for $\overline{SET}$	t_{IR}	5	—	5	—	ns

3. Partial Purge (MODE = H or L, $\overline{PURGE}$ = H, $\overline{WRITE}$ = H, $\overline{INVL}$ = L, H/$\overline{R}$ = H or L, $\overline{INH}$ = H, RLATCH = L, $\overline{PINV}$ = H or L, $\overline{VINV}$ = H or L)

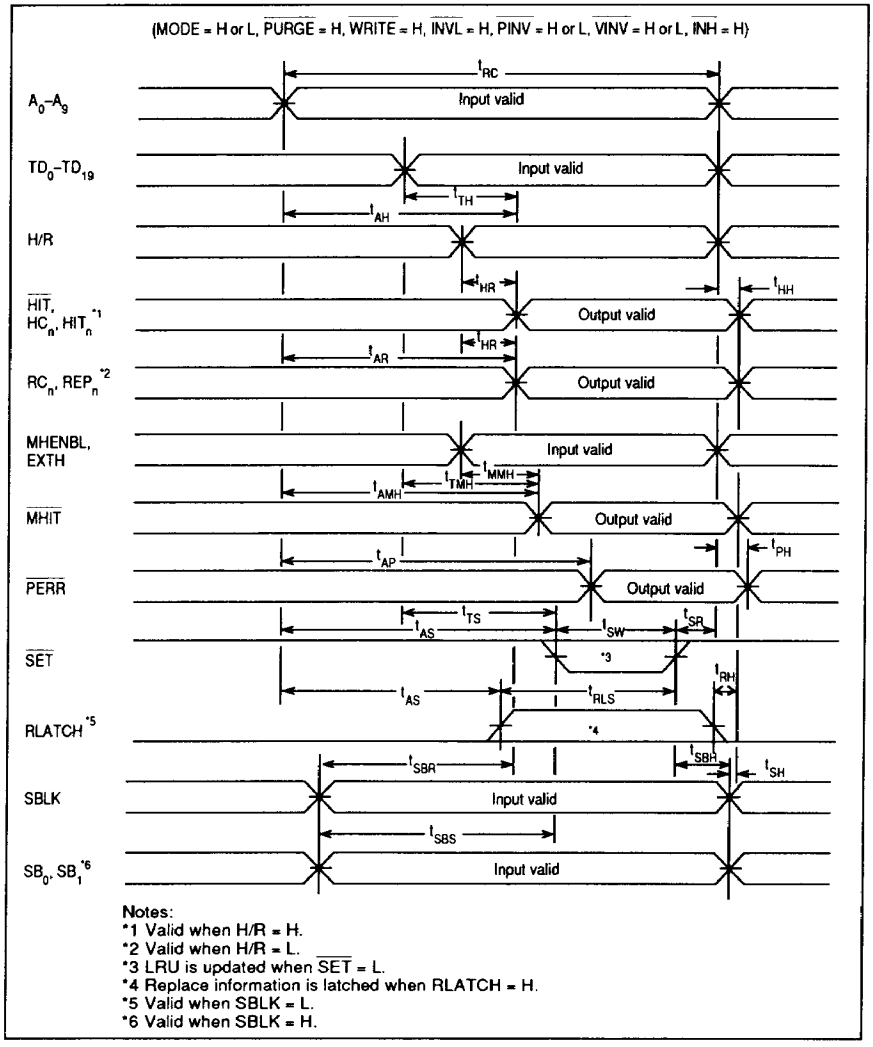
		HM644332G-25		HM644332G-30		
Item	Symbol	Min.	Max.	Min.	Max.	Unit
Partial Purge Cycle	t_{PPC}	50	—	50	—	ns
Address Setup Time for $\overline{SET}$	t_{AS}	25	—	25	—	ns
Tag Data Setup Time for $\overline{SET}$	t_{TS}	25	—	25	—	ns
$\overline{SET}$ Pulse Width	t_{SW}	20	—	20	—	ns
$\overline{SET}$ Recovery Time	t_{SR}	5	—	5	—	ns
SBLK, SB_0, SB_1 Setup Time for $\overline{SET}$	t_{SBS}	25	—	25	—	ns
SBLK, SB_0, SB_1 Hold Time	t_{SBH}	5	—	5	—	ns

4. All Purge ($\overline{SET}$ = H, other control inputs are H or L)

		HM644332G-25		HM644332G-30		
Item	Symbol	Min.	Max.	Min.	Max.	Unit
All Purge Cycle Time	t_{APC}	100	—	100	—	ns
Purge Pulse Width	t_{PPW}	50	—	50	—	ns
Purge Recovery Time	t_{PR}	50	—	50	—	ns

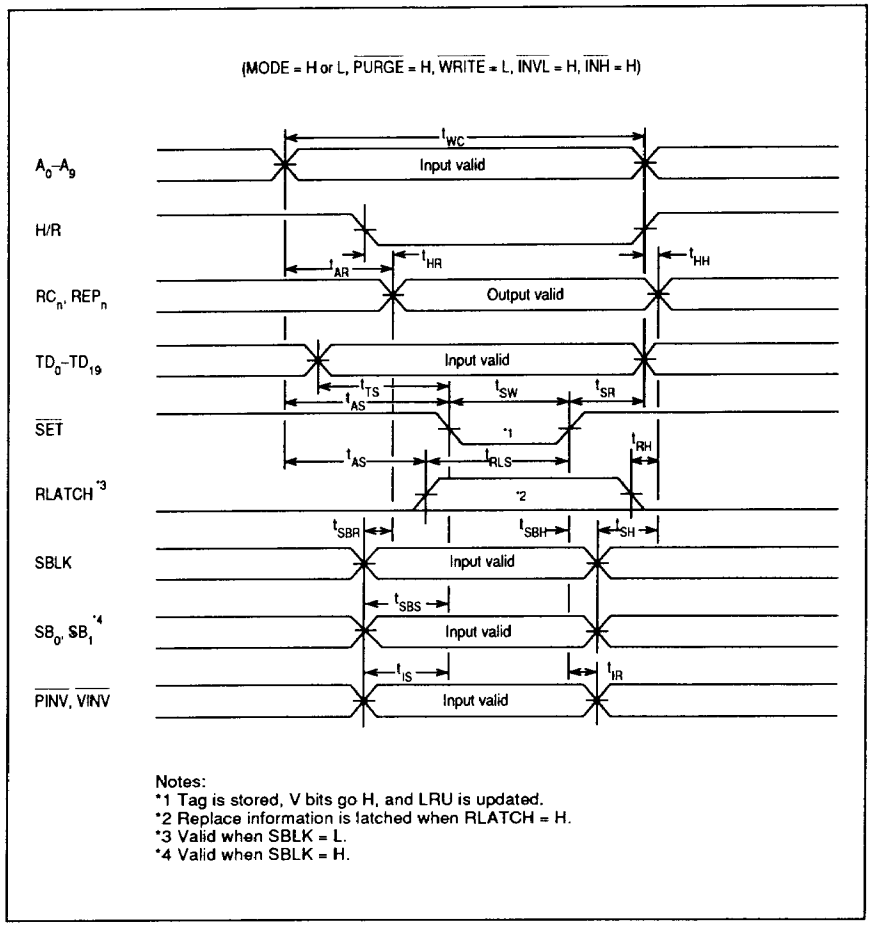
Timing Charts

1. Tag Read Cycle



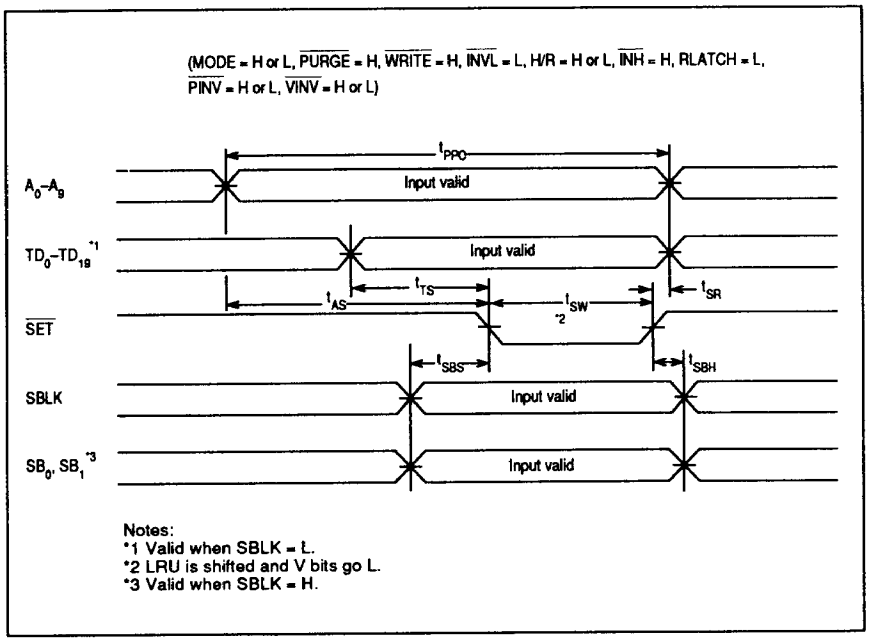
Notes:
*1 Valid when H/R = H.
*2 Valid when H/R = L.
*3 LRU is updated when $\overline{SET}$ = L.
*4 Replace information is latched when RLATCH = H.
*5 Valid when SBLK = L.
*6 Valid when SBLK = H.

2. Tag Write Cycle

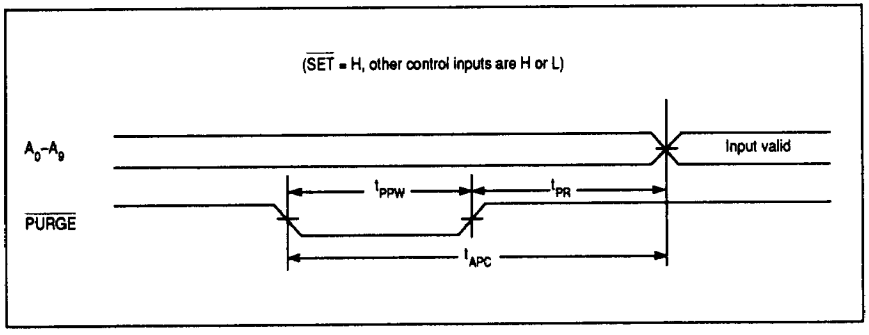


Notes:
*1 Tag is stored, V bits go H, and LRU is updated.
*2 Replace information is latched when RLATCH = H.
*3 Valid when SBLK = L.
*4 Valid when SBLK = H.

3. Partial Purge Cycle



4. All Purge Cycle



Function Description

Tag Read

The TAG input data (TD_0–TD_{19}) and the contents of the addressed location are compared. If they are the same, a hit is assumed. $\overline{HIT}$ goes low and the HCn and HITn outputs indicate the hit way associatively. If there is no hit, the LRU logic of the tag RAM automatically specifies which way is to be replaced.

The replacement information is presented at the RCn and REPn outputs by forcing the H/R input low. These signals will be latched and used for writing data into data memory.

Tag Write

If there is no hit, the tag RAM must be updated. A write operation is performed by setting $\overline{WRITE}$ low and inputting a $\overline{SET}$ pulse. The tag data will be written into the appropriate way by the internal LRU logic.

The way can be also specified externally by using SBLK, SB_0 and SB_1 inputs. In tag write mode, the V bits (validity bits) and the parity bit are set, and the LRU is updated.

All Purge

By asserting the $\overline{PURGE}$ input low, all the V bits are reset and LRU is initialized.

In this operation, the contents of each tag and its parity will not be identified.

Partial Purge

A partial purge operation is performed by setting $\overline{INVL}$ low and inputting a $\overline{SET}$ pulse.

The V bit specified by the address input is reset and the LRU is shifted so that the partially-purged way becomes the least recently used way.

Package Dimensions

Unit: mm (inches)

64-Pin Ceramic PGA