CHAPTER 1. OUTLINE

1.1 FEATURES

- o Serial bus interface: 2 channels
  - . 3-wire/SBI/2-wire/I^2C bus mode: 1 channel
  - . 3-wire mode (built-in automatic transmission/reception function): 1 channel

- o Built-in large-capacity ROM and RAM
  - . uPD78011Y
    - Mask ROM: 8K bytes
    - Internal high-speed RAM: 512 bytes
    - Buffer RAM: 32 bytes
  - . uPD78012Y
    - Mask ROM: 16K bytes,
    - Internal high-speed RAM: 512 bytes
    - Buffer RAM: 32 bytes
  - . uPD78013Y
    - Mask ROM: 24K bytes,
    - Internal high-speed RAM: 1024 bytes
    - Buffer RAM: 32 byte
  - . uPD78014Y
    - Mask ROM: 32K bytes
    - Internal high-speed RAM: 1024 bytes
    - Buffer RAM: 32 bytes
  - . uPD78P014Y
    - PROM: 32K bytes*
    - Internal high-speed RAM: 1024 bytes*
    - Buffer RAM: 32 bytes

*: The capacity of internal PROM and internal high-speed RAM can be changed by means of the memory size switching register.

- o External memory extended space: 64K bytes

- o Instruction execution time changeable from high speed (0.4 us) to ultra-low speed (122 us)

- o Instruction set suited to system control
  - . Bit manipulation possible in all address spaces
  - . Built-in multiply and divide instructions

- o 53 I/O ports

- o 8-bit resolution A/D converter: 8 channels

  . Operational at low voltages (V_{DD} = 2.7 to 6.0 V: Operational in the same voltage range as with CPU)

- o Timer: 5 channels
  - . 16-bit timer/event counter: 1 channel
  - . 8-bit timer/event counter : 2 channels
  - . Clock timer : 1 channel
  - . Watchdog timer : 1 channel

- o 14 vectored interrupts

- o 2 test inputs

- o 2 types of built-in clock oscillator circuits (main system clock and subsystem clock)

- o Operating power supply voltage range: 2.7 to 6.0 V

1.2 APPLICATIONS

Televisions, VCRs, audio equipment, etc.

1.3 ORDERING INFORMATION

Ordering Code	Package	Internal ROM
uPD78011YCW-xxx	64-pin plastic shrink DIP (750 mil)	Mask ROM
uPD78011YGC-xxx-AB8	64-pin plastic QFP (14 x 14 mm)	Mask ROM
uPD78012YCW-xxx	64-pin plastic shrink DIP (750 mil)	Mask ROM
uPD78012YGC-xxx-AB8	64-pin plastic QFP (14 x 14 mm)	Mask ROM
uPD78013YCW-xxx	64-pin plastic shrink DIP (750 mil)	Mask ROM
uPD78013YGC-xxx-AB8	64-pin plastic QFP (14 x 14 mm)	Mask ROM
uPD78014YCW-xxx	64-pin plastic shrink DIP (750 mil)	Mask ROM
uPD78014YGC-xxx-AB8	64-pin plastic QFP (14 x 14 mm)	Mask ROM
uPD78P014YCW	64-pin plastic shrink DIP (750 mil)	One-time programmable PROM
uPD78P014YDW	64-pin DIP with ceramic window (750 mil)	EPROM
uPD78P014YGC-AB8	64-pin plastic QFP (14 x 14 mm)	One-time programmable PROM

1.4 QUALITY GRADE

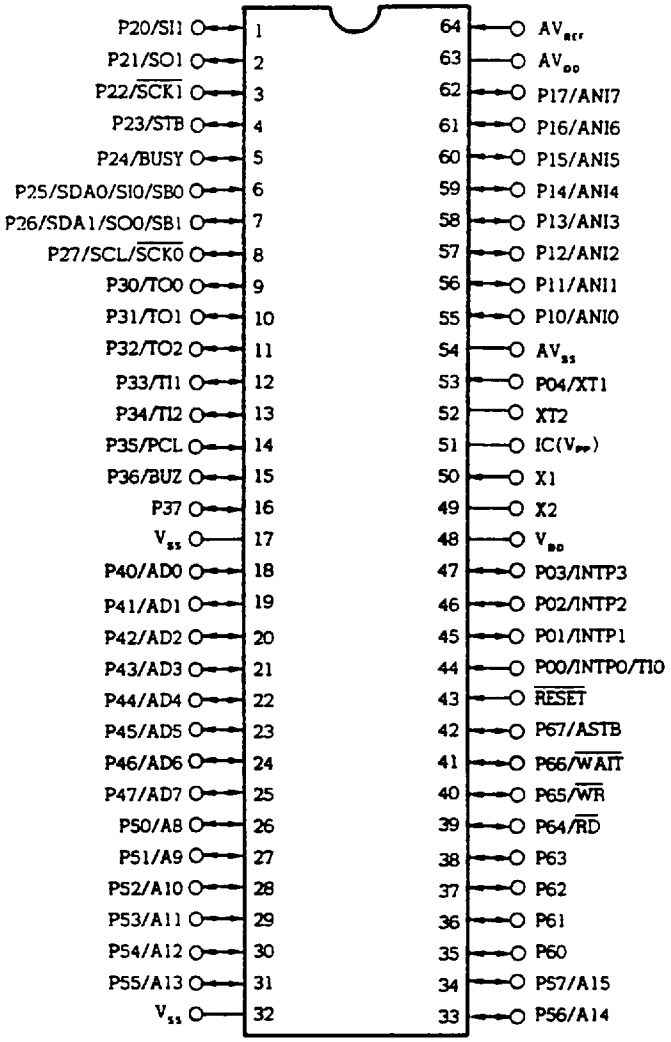
Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

1.5 PIN CONFIGURATION (TOP VIEW)

(1) Normal operating mode

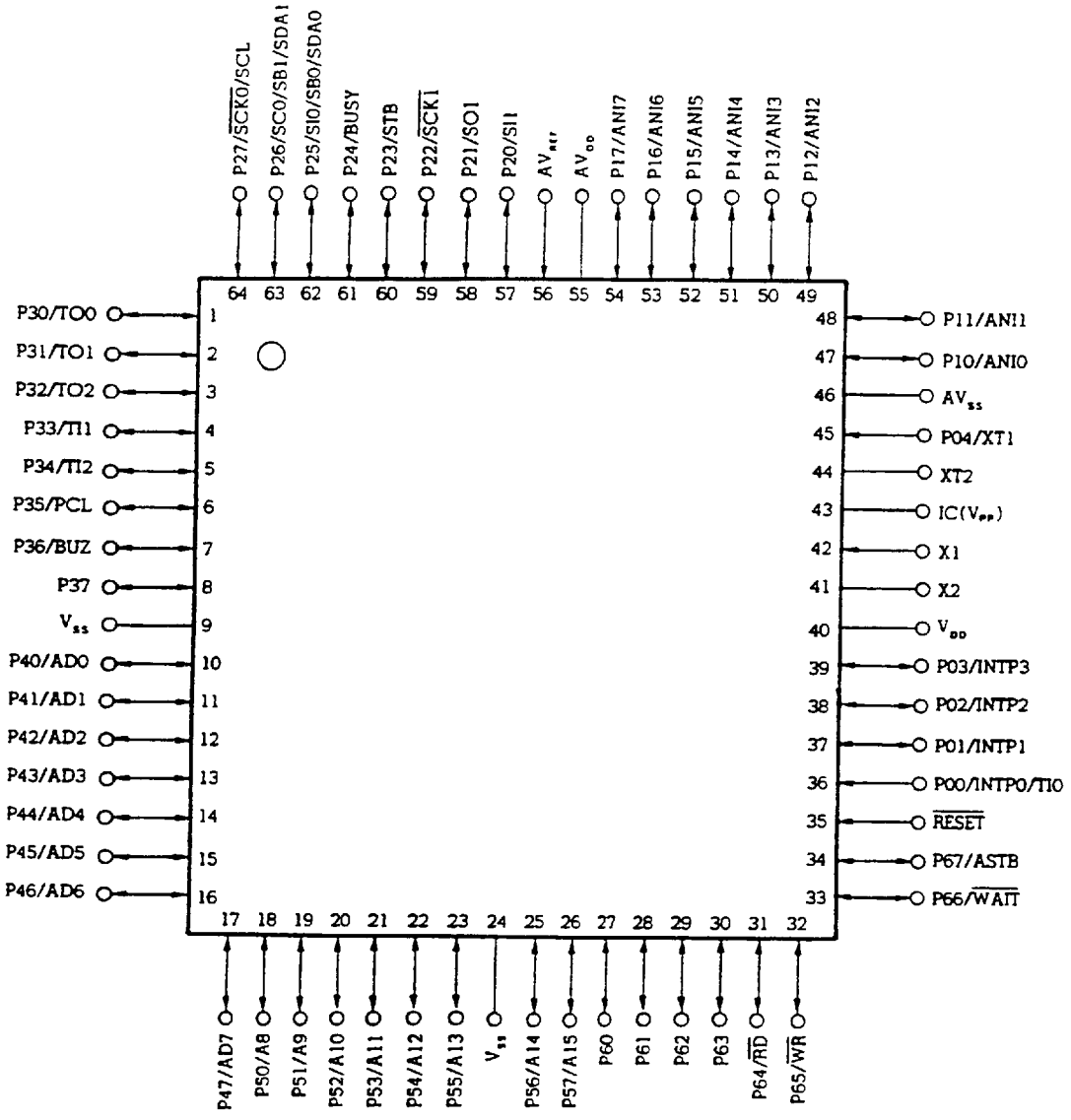
64-pin plastic shrink DIP



NOTE: Be sure to connect IC (Internally Connected) to V_{SS}.

Remarks: Pin connection in parentheses is intended for uPD78P014Y.

64-pin plastic QFP



NOTE: Be sure to connect IC (Internally Connected) to V_{SS}.

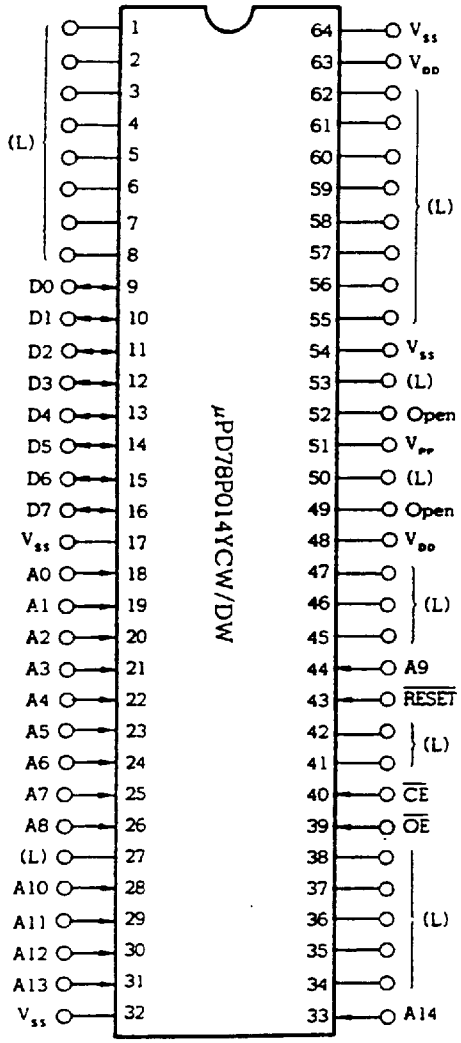
Remarks: Pin connection in parenthesis is intended for uPD78P014Y.

P00 to P04	:	Port0
P10 to P17	:	Port1
P20 to P27	:	Port2
P30 to P37	:	Port3
P40 to P47	:	Port4
P50 to P57	:	Port5
P60 to P67	:	Port6
INTP0 to INTP3	:	Interrupt From Peripherals 0 to 3
TI0 to TI2	:	Timer Input 0 to 2
TO0 to TO2	:	Timer Output 0 to 2
SB0, SB1	:	Serial Bus0, 1
SI0, SI1	:	Serial Input 0, 1
SO0, SO1	:	Serial Output 0, 1
$\overline{SCK0}$, $\overline{SCK1}$	:	Serial Clock 0, 1
SCL	:	Serial Clock
SDA0, SDA1	:	Serial Data 0, 1
PCL	:	Programmable Clock
BUZ	:	Buzzer Clock
STB	:	Strobe
BUSY	:	Busy

AD0 to AD7	:	Address/Data Bus0 to 7
A8 to A15	:	Address Bus 8 to 15
$\overline{RD}$	:	Read Strobe
$\overline{WR}$	:	Write Strobe
$\overline{WAIT}$	:	Wait
ASTB	:	Address Strobe
X1, X2	:	Crystal1, 2 (Main System Clock)
XT1, XT2	:	Crystal1,2 (Subsystem Clock)
$\overline{RESET}$	:	Reset
ANI0 to ANI7	:	Analog Input 0 to 7
AV_{DD}	:	Analog Power Supply
AV_{SS}	:	Analog Ground
AV_{REF}	:	Analog Reference Voltage
V_{DD}	:	Power Supply
V_{PP}	:	Programming Power Supply
V_{SS}	:	Ground
IC	:	Internally Connected

(2) PROM programming mode

64-pin plastic shrink DIP



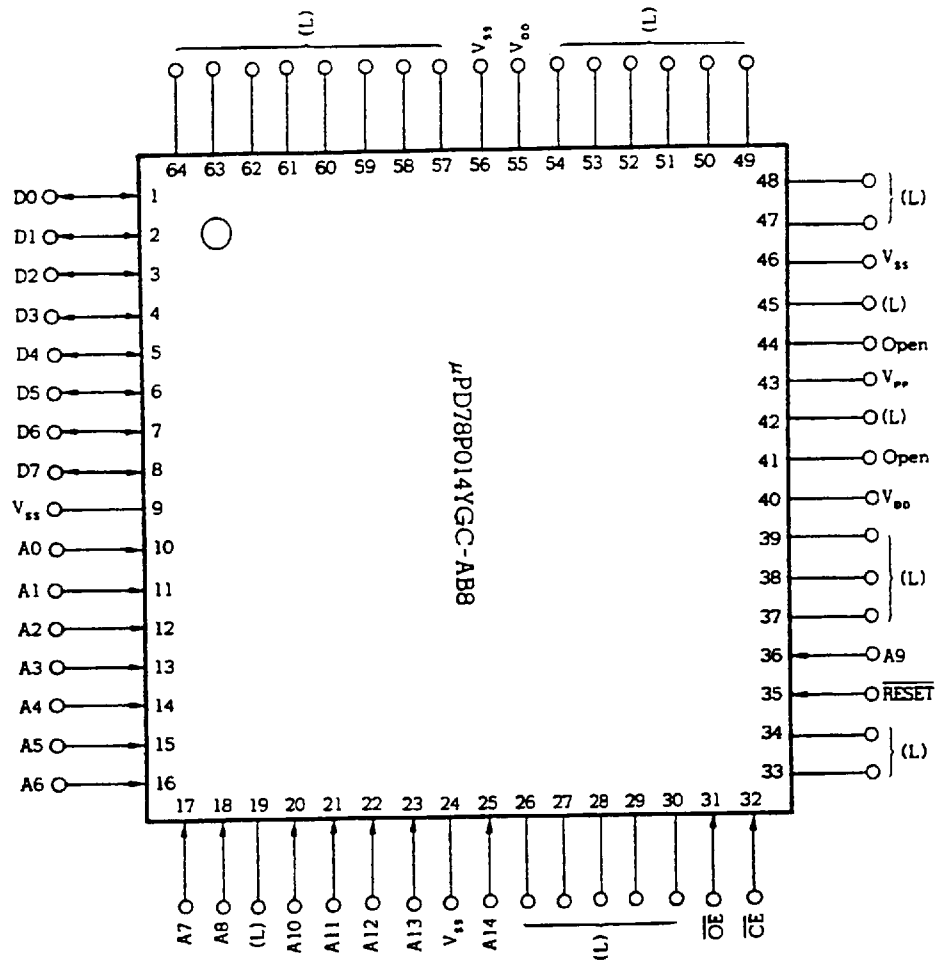
NOTE 1: (L) : Connect individually to V_{SS} via a pull-down resistor (10 kΩ).

2: V_{SS} : Connect to the ground.

3: $\overline{RESET}$: Set to the low level.

4: Open : Do not connect anything.

64-pin plastic QFP



NOTE 1: (L) : Connect individually to V_{SS} via a pull-down resistor (10 kΩ).

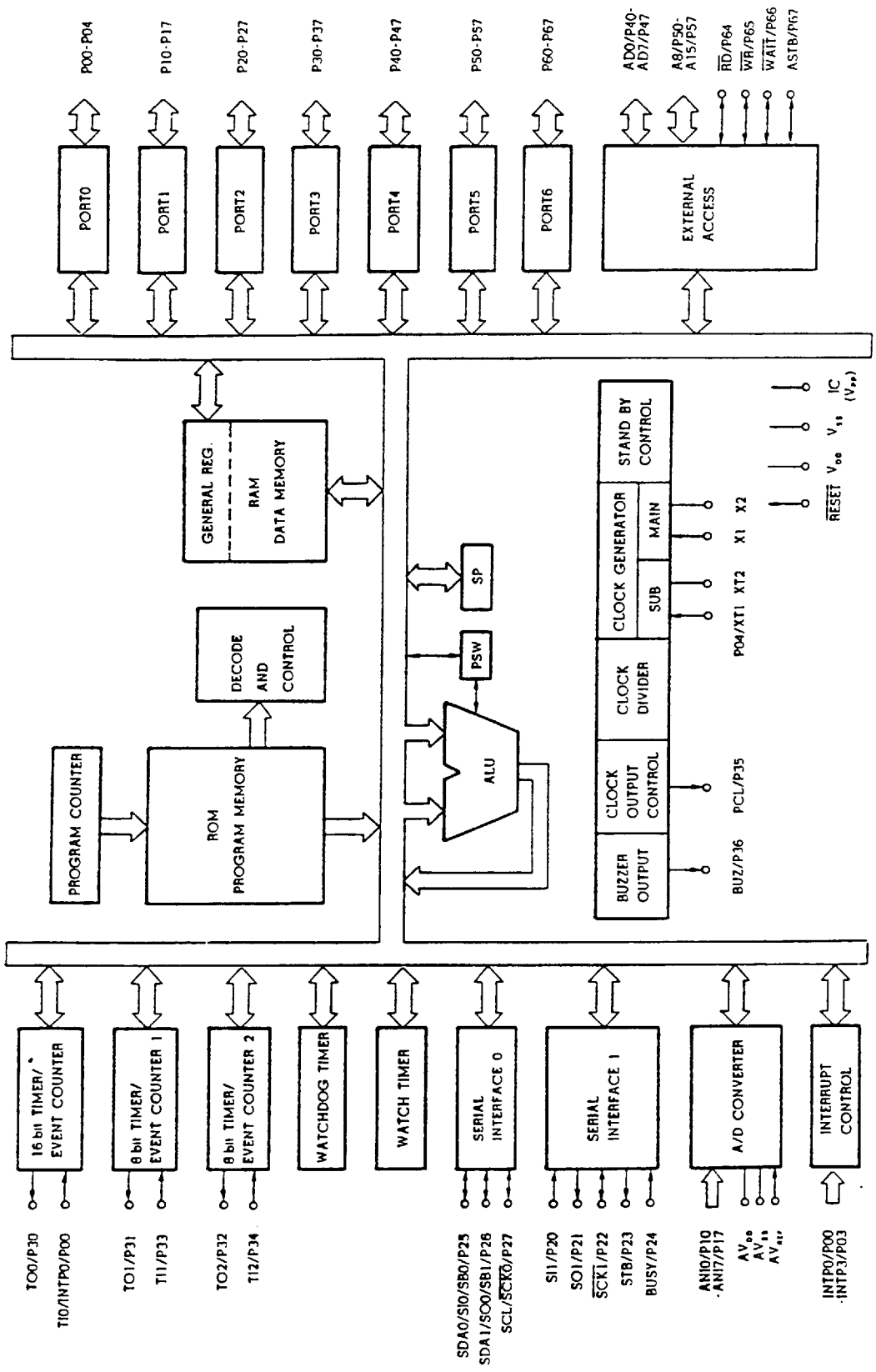
2: V_{SS} : Connect to the ground.

3: $\overline{RESET}$: Set to the low level.

4: Open : Do not connect anything.

A0 to A14:	Address Bus	$\overline{RESET}$:	Reset
D0 to D7 :	Data Bus	V_{DD} :	Power Supply
$\overline{CE}$:	Chip Enable	V_{PP} :	Programming Power Supply
$\overline{OE}$:	Output Enable	V_{SS} :	Ground

1.6 BLOCK DIAGRAM



NOTE 1: The internal ROM and RAM capacities depend on the product.
2: Pin connection in parentheses is intended for the uPD78P014Y.

1.7 OUTLINE OF FUNCTION

Item \ Product Name			uPD 78011Y	uPD 78012Y	uPD 78013Y	uPD 78014Y	uPD 78P014Y
Internal memory	ROM	Configuration	Mask ROM				PROM
		Capacity	8K bytes	16K bytes	24K bytes	32K bytes	32K bytes*
	Internal high-speed RAM	Capacity	512 bytes		1024 bytes		1024 bytes*
	Buffer RAM	Capacity	32 bytes				
Memory space			64K bytes				
General register			8 bits x 8 x 4 banks				
Instruction cycle	With main system clock selected		0.48 us/0.95 us/1.91 us/3.81 us/7.63 us (when operated at 8.38 MHz)				
	With subsystem clock selected		122 us (when operated at 32.768 kHz)				
Instruction set			. 16 bit operation . Multiplication/division (8 bits x 8 bits, 16 bits ÷ 8 bits) . Bit manipulation (set, reset, test, and Boolean operation) . BCD correction and other related operations				
I/O port			. Total : 53 I/O ports . CMOS input : 2 inputs . CMOS input/output: 47 inputs/outputs (Built-in pull-up resistor ON/OFF possible by software: 47 inputs/outputs) . N-ch open-drain inputs/outputs: 4 inputs/outputs (15 V withstand voltage; pull-up resistor incorporated with mask option for mask ROM products only: 4 inputs/outputs)				
A/D converter			. 8-bit resolution x 8 channels . Operational at low voltages: V_{DD} = 2.7 to 6.0 V				

(to be continued)

(cont'd)

Item \ Product Name		uPD 78011Y	uPD 78012Y	uPD 78013Y	uPD 78014Y	uPD 78P014Y
Serial interface		. 3-wire/SBI/2-wire/I^2C bus mode selection possible: 1 channel . 3-wire mode (with built-in automatic transmit/receive functions with a maximum of 32 bytes): 1 channel				
Timer		. 16-bit timer/event counter: 1 channel . 8-bit timer/event counter : 2 channels . Clock timer : 1 channel . Watchdog timer : 1 channel				
Timer output		. 3 outputs: (14-bit PWM generation possible from one output)				
Clock output		32.7 kHz, 65.5 kHz, 131 kHz, 262 kHz, 524 kHz, 1.05 MHz (when operated at 8.38 MHz with main system clock and 32.768 kHz with subsystem clock)				
Buzzer output		2 kHz, 4 kHz, 8 kHz (when operated at 8.38 MHz with main system clock)				
Vectored interrupt	Maskable interrupt	Internal: 8, external: 4				
	Non-maskable interrupt	Internal: 1				
	Software interrupt	Internal: 1				
Test input		Internal: 1, external: 1				
Operating power supply voltage range		V_{DD} = 2.7 to 6.0 V				
Package		. 64-pin plastic shrink DIP (750 mil) . 64-pin plastic QFP (14 x 14 mm) . 64-pin ceramic shrink DIP with window (750 mil) (uPD78P014Y only)				

*: The capacity of internal PROM and internal high-speed RAM can be be changed by means of the memory size switching register.

CHAPTER 2. PIN FUNCTION

2.1 PIN FUNCTION LIST

2.1.1 PORT PINS

Pin Name	Input/ Output	Function		Dual-Function Pin
P00	Input	Port 0. 5-bit input/ output port.	Input only	INTP0/ TI0
P01	Input/ output		Input/output specifiable bit-wise. If used as an input port, a pull-up resistor can be connected by software.	INTP1
P02				INTP2
P03				INTP3
P04*1	Input		Input only	XT1
P10 to P17	Input/ output	Port 1. 8-bit input/output port. Input/output specifiable bit-wise. If used as an input port, a pull-up resistor can be connected by software*2		ANI0 to ANI7
P20	Input/ output	Port 2. 8-bit input/output port. Input/output specifiable bit-wise. If used as an input port, a pull-up resistor can be connected by software.		SI1
P21				SO1
P22				$\overline{SCK1}$
P23				STB
P24				BUSY
P25				SI0/SB0/ SDA0
P26				SO0/SB1/ SDA1
P27				$\overline{SCK0}$/SCL

(to be continued)

(cont'd)

Pin Name	Input/ Output	Function		Dual-Function Pin
P30	Input/ output	Port 3. 8-bit input/output port. Input/output specifiable bit-wise. If used as an input port, a pull-up resistor can be connected by software.		TOO
P31				TO1
P32				TO2
P33				TI1
P34				TI2
P35				PCL
P36				BUZ
P37				—
P40 to P47	Input/ output	Port 4. 8-bit input/output port. Input/output specifiable in 8-bit units. If used as an input port, a pull-up resistor can be connected by software. Test flag (KRIF) is set to 1 by falling edge detection.		AD0 to AD7
P50 to P57	Input/ output	Port 5. 8-bit input/output port. LED direct drive capability. Input/output specifiable bit-wise. If used as an input port, a pull-up resistor can be connected by software.		A8 to A15
P60	Input/ output	Port 6. 8-bit input/output port. Input/output specifiable bit-wise.	N-ch open-drain input/ output port. On-chip pull-up resistor specifiable by mask option for mask ROM products only. LED direct drive capability.	—
P61				
P62				
P63				
P64			If used as an input port, a pull-up resistor can be connected by software.	$\overline{RD}$
P65				$\overline{WR}$
P66				$\overline{WAIT}$
P67				ASTB

*1: When using the P04/XT1 pin as an input port, disconnect the feedback resistor of the subsystem clock oscillator circuit with bit 6 of the processor control resistor (FRC).

2: When using the P10/ANI0 to P17/ANI7 pin as an analog input of the A/D converter, a pull-up resistor is automatically disconnected.

2.1.2 NON-PORT PINS

Pin Name	Input/ Output	Function	Dual-Function Pin
INTP0	Input	Valid edges (rising edge, falling edge and both rising and falling edges) specifiable External interrupt input	P00/TI0
INTP1			P01
INTP2			P02
INTP3		Falling edge detected external interrupt input	P03
SI0	Input	Serial interface serial data input	P25/SB0 SDA0
SI1			P20
SO0	Output	Serial interface serial data output	P26/SB1 SDA1
SO1			P21
SB0	Input/ output	Serial interface serial data input/output	P25/SI0 SDA0
SB1			P26/SO0 SDA0
SDA0			P25/SB0/ SI0
SDA1			P26/SB1/ SO0
$\overline{SCK0}$	Input/ output	Serial interface serial clock input/output	P27/SCL
$\overline{SCK1}$			P22
SCL			P27/$\overline{SCK0}$
STB	Output	Serial interface automatic transmit/receive strobe output	P23
BUSY	Input	Serial interface automatic transmit/receive busy input	P24

(to be continued)

(cont'd)

Pin Name	Input/ Output	Function	Dual-Function Pin
TI0	Input	External count clock input to timer	P00/ INTP0
TI1			P33
TI2			P34
TO0	Output	Timer output	P30
TO1			P31
TO2			P32
PCL	Output	Clock output (for main system clock and subsystem clock trimming)	P35
BUZ	Output	Buzzer output	P36
AD0 to AD7	Input/ output	Lower address/data bus for external memory expansion	P40 to P47
A8 to A15	Output	Higher address bus for external memory expansion	P50 to P57
$\overline{RD}$	Output	Strobe signal output for external memory read operation	P64
$\overline{WR}$		Strobe signal output for external memory write operation	P65
$\overline{WAIT}$	Input	Wait insertion for external memory access	P66
ASTB	Output	Strobe output to externally latch the address information which is output to ports 4 and 5 for external memory access	P67
ANI0 to ANI7	Input	A/D converter analog input	P10 to P17
AV_{REF}	Input	A/D converter reference voltage input	—
AV_{DD}	—	A/D converter analog power supply	—
AV_{SS}	—	A/D converter ground potential	—
$\overline{RESET}$	Input	System reset input	—

(to be continued)

(cont'd)

Pin Name	Input/ Output	Function	Dual-Function Pin
X1	Input	Crystal connection for main system clock oscillation	—
X2	—		—
XT1	Input	Crystal connection for subsystem clock oscillation	P04
XT2	—		—
V_{DD}	—	Positive power supply	—
V_{PP}	—	High-voltage application for program write/ verify	—
V_{SS}	—	Ground potential	—
IC	—	Internal connection	—

2.1.3 PROM PROGRAMMING MODE PINS

Pin Name	Input/ Output	Function
$\overline{\text{RESET}}$	Input	PROM programming mode setting. When +5 V or 12.5 V is applied to the V_{PP} pin or a low level voltage is applied to the $\overline{\text{RESET}}$ pin, the PROM programming mode is set.
V_{PP}	Input	High-voltage application for PROM programming mode setting and program write/verify.
A0 to A14	Input	Address bus
D0 to D7	Input/ output	Data bus
$\overline{\text{CE}}$	Input	PROM enable input/program pulse input
$\overline{\text{OE}}$	Input	Read strobe input to PROM
V_{DD}	—	Positive power supply
V_{SS}	—	Ground potential

2.2 DESCRIPTION OF PIN FUNCTIONS

2.2.1 P00 TO P04 (PORT 0)

These ports are 5-bit input/output ports. Besides serving as input/output ports, they function for an external interrupt input, an external count clock input to the timer, a capture trigger signal input and crystal connection for subsystem clock oscillation.

The following operating modes can be specified bit-wise.

(1) Port mode

P00 and P04 function as input-only ports and P01 to P03 function as input/output ports.

P01 to P03 can be specified for input or output ports bit-wise with a port 0 mode register. When they are used as input ports, a pull-up resistor can be connected to them with a pull-up resistor option register.

(2) Control mode

In this mode, these ports function for an external count clock input to the timer and crystal connection for subsystem clock oscillation.

(a) INTP0 to INTP3

INTP0 to INTP2 are external interrupt input pins which can specify valid edges (rising edge, falling edge and both rising and falling edges). INTP0 becomes a 16-bit timer/event counter capture trigger signal input pin with a valid edge input. INTP3 serves as a falling edge-detected external interrupt input pin.

(b) TI0

Pin for external count clock input to the timer

(c) XT1

Crystal connect pin for subsystem clock oscillation

2.2.2 P10 TO P17 (PORT 1)

8-bit input/output ports. Besides serving as input/output ports, they function for A/D converter analog input.

The following operating modes can be specified bit-wise.

(1) Port mode

These ports function as 8-bit input/output ports. They can be specified for input or output ports bit-wise with a port mode register 1. If used as an input port, pull-up resistor can be connected to these ports with a pull-up resistor option register.

(2) Control mode

These ports function as A/D converter analog input pins. The pull-up resistor is automatically disconnected from the pins specified for analog input.

2.2.3 P20 TO P27 (PORT 2)

8-bit input/output ports. Besides serving as input/output ports, they function for data input/output to/from the serial interface, clock input/output, busy input for automatic transmission/reception and strobe output functions.

The following operating modes can be specified bit-wise.

(1) Port mode

These ports function as 8-bit input/output ports. They can be specified for input or output ports bit-wise with a port mode register 2. When they are used as input ports, a pull-up resistor can be connected to them with a pull-up resistor option register.

(2) Control mode

These ports function for serial interface data input/output, clock input/output, busy input for automatic transmission/reception and strobe output.

(a) SI0, SI1, SO0 and SO1

Serial interface serial data input/output pins

(b) SDA0 and SDA1

Serial interface serial data input/output pins

(c) $\overline{\text{SCK0}}$ and $\overline{\text{SCK1}}$

Serial interface serial clock input/output pins

(d) SCL

Serial interface serial clock input/output pins

(e) SB0 and SB1

NEC standard serial bus interface input/output pins

(f) BUSY

Serial interface automatic transmit/receive busy input pins

(g) STB

Serial interface automatic transmit/receive strobe output pins.

NOTE: When the P22/$\overline{SCK1}$ and P27/$\overline{SCK0}$/SCL pins are used for serial clock output, set PM22 and PM27 to 0 and the output latch to 1.

2.2.4 P30 TO P37 (PORT 3)

8-bit input/output ports. Besides serving as input/output ports, they function for timer input/output, clock output and buzzer output.

The following operating modes can be specified bit-wise.

(1) Port mode

These ports function as 8-bit input/output ports. They can be specified bit-wise for input or output ports with port mode register 3. When they are used as input ports, a pull-up resistor can be connected to them with a pull-up resistor option register.

(2) Control mode

These ports function for timer input/output, clock output and buzzer output.

(a) TI1 and TI2

Pin for external clock input to the timer

(b) TO0 to TO2

Timer output pins

(c) PCL

Clock output pin

(d) BUZ

Buzzer output pin

2.2.5 P40 TO P47 (PORT 4)

8-bit input/output ports. Besides serving as input/output ports, they function the address/data bus function.

Test flag (KRIF) is set to 1 by falling edge detection.

The following operating modes can be specified in 8-bit units.

(1) Port mode

These ports function as 8-bit input/output ports. They can be specified for input or output ports in 8-bit units with memory expansion register. When they are used as input ports, a pull-up resistor can be connected to them with a pull-up resistor option register.

(2) Control mode

These ports function as lower address/data bus pins (AD0 to AD7) in the external memory expansion mode. A pull-up resistor is automatically disconnected from the pins used as address/data bus.

2.2.6 P50 TO P57 (PORT 5)

8-bit input/output ports. Besides serving as input/output ports, they function the address bus function.

They can directly drive LEDs.

The following operating modes can be specified bit-wise.

(1) Port mode

These ports function as 8-bit input/output ports. They can be specified for input or output ports bit-wise with a port mode register 5. When they are used as input ports, a pull-up resistor can be connected to them with a pull-up resistor option register.

(2) Control mode

These ports function as higher address bus pins (A8 to A15) in the external memory expansion mode. The pull-up resistor is automatically disconnected from the pins used as address bus.

2.2.7 P60 TO P67 (PORT 6)

8-bit input/output ports. Besides serving as input/output ports, they carry out the control function in the external memory expansion mode.

P60 to P63 can directly drive the LEDs.

The following operating modes can be specified bit-wise.

(1) Port mode

These ports function as 8-bit input/output ports. They can be specified for input or output ports bit-wise with a port mode register 6.

P60 to P63 are N-ch open-drain. Mask ROM products can incorporate a pull-up resistor with mask option.

When P64 to P67 are used as input ports, a pull-up resistor can be connected to them with a pull-up resistor option register.

(2) Control mode

These ports function as control signal output pins ($\overline{RD}$, $\overline{WR}$, $\overline{WAIT}$ and ASTB) in the external memory expansion mode. The pull-up resistor is automatically disconnected from the pins used for control signal output.

NOTE: When no external wait is used in the external memory expansion mode, P66 can be used as an input/output port.

2.2.8 AV_{REF}

A/D converter reference voltage input pin

2.2.9 AV_{DD}

A/D converter analog power supply pin

2.2.10 AV_{SS}

A/D converter ground potential pin

2.2.11 $\overline{\text{RESET}}$

Low-level active system reset input pin

2.2.12 X1 AND X2

Crystal resonator connect pins for main system clock.
For external clock supply, input it to X1 and the reverse signal to X2.

2.2.13 XT1 AND XT2

Crystal resonator connect pins for subsystem clock oscillation.
For external clock supply, input it to XT1 and the reverse signal to X2.

2.2.14 V_{DD}

Positive power supply pin

2.2.15 V_{SS}

Ground potential pin

2.2.16 V_{PP} (uPD78P014Y ONLY)

High-voltage apply pin for PROM programming mode setting and program write/verify

2.2.17 IC (MASK ROM PRODUCTS ONLY)

Internal connect pin

2.3 INPUT/OUTPUT CIRCUIT AND RECOMMENDED CONDITIONS OF UNUSED PINS

Table 2-1 shows the input/output circuit types of pins and the recommended conditions of unused pins.

Refer to Figure 2-1 for the configuration of the input/output circuit of each type.

Table 2-1 Pin Input/Output Circuit Types

Pin Name	Input/Output Circuit Type	Input/Output	Recommended Connection of Unused Pins
P00/INTP0/TI0	2	Input	Connect to V_{DD}.
P01/INTP1	8-A	Input/output	Input : Connect to V_{SS}. Output: Open
P02/INTP2			
P03/INTP3			
P04/XT1	1	Input	Connect to V_{SS}.
P10/ANI0 to P17/ANI7	9-B	Input/output	Input : Connect to V_{DD} or V_{SS}. Output: Open
P20/SI1	8-A	Input/output	Input : Connect to V_{DD} or V_{SS}. Output: Open
P21/SO1	5-A		
P22/$\overline{SCK1}$	8-A		
P23/STB	5-A		
P24/BUSY	8-A		
P25/SI0/SB0 SDA0	10-A		
P26/SO0/SB1 SDA1			
P27/$\overline{SCK0}$/SCL			

(to be continued)

Table 2-1 Pin Input/Output Circuit Types (cont'd)

Pin Name	Input/Output Circuit Type	Input/Output	Recommended Connection of Unused Pins
P30/TO0	5-A	Input/output	Input : Connect to V_{DD} or V_{SS}. Output: Open
P31/TO1			
P32/TO2			
P33/TI1	8-A		
P34/TI2			
P35/PCL	5-A		
P36/BUZ			
P37			
P40/AD0 to P47/AD7	5-B	Input/output	Input : Connect to V_{SS}. Output: Open
P50/A8 to P57/A15	5-A	Input/output	Input : Connect to V_{DD} or V_{SS}. Output: Open
P60 to P63 (mask ROM product)	13-B		
P60 to P63 (uPD78P014Y)	13		
P64/$\overline{RD}$	5-A		
P65/$\overline{WR}$			
P66/$\overline{WAIT}$			
P67/ASTB			
$\overline{RESET}$	2	Input	—
XT2	—	—	Open
AV_{REF}			Connect to V_{SS}.
AV_{DD}			Connect to V_{DD}.
AV_{SS}			Connect to V_{SS}.
IC			

Figure 2-1 Pin Input/Output Circuit List

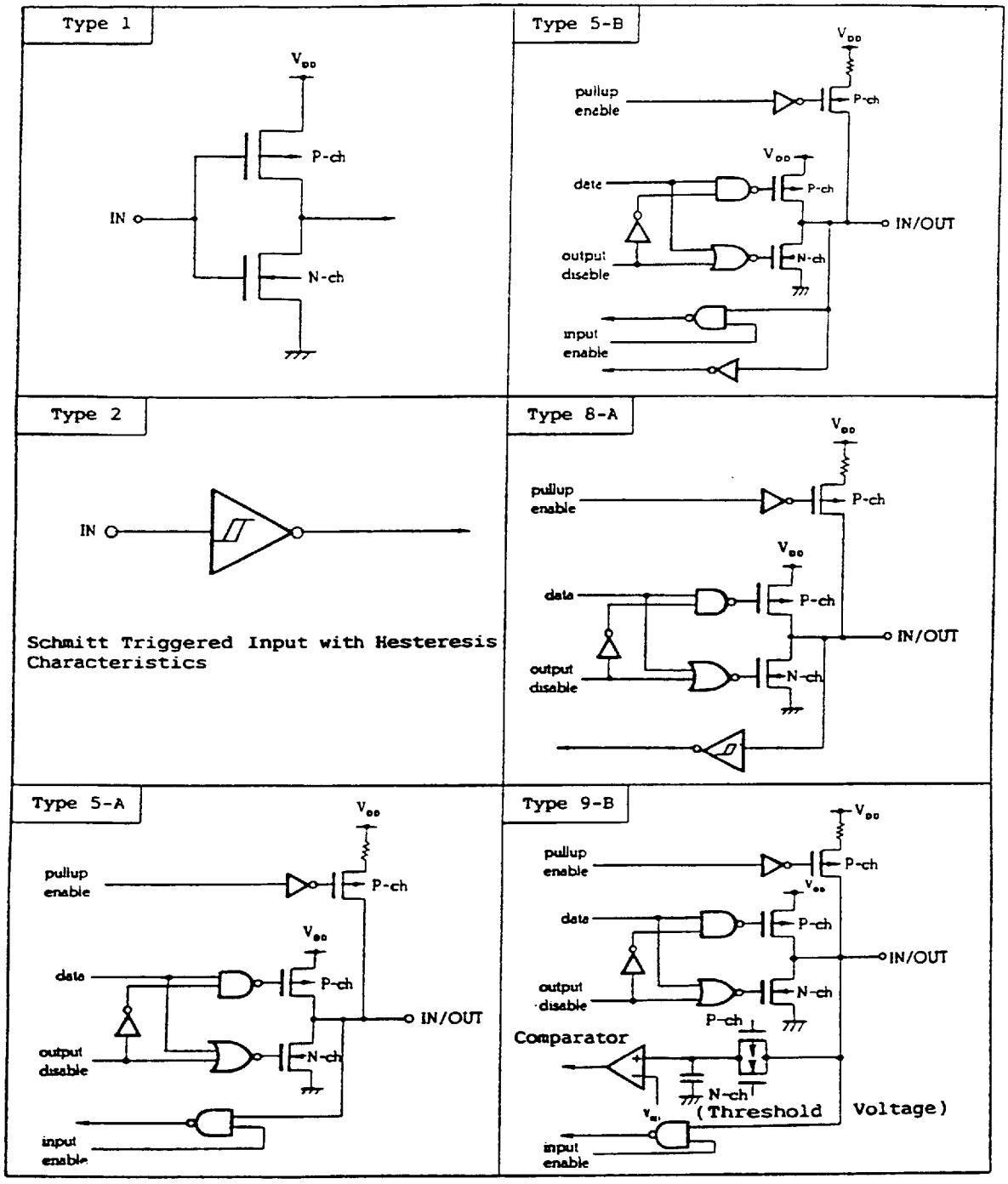


Figure 2-1 Pin Input/Output Circuit List (cont'd)