

## ASSP for Graphics Control

# Graphics Display Controller

## MB86292

### ■ DESCRIPTION

The MB86292 is an evolved version of the Fujitsu MB86290A graphics controller designed for use in a car navigation system or amusement equipment. The MB86292 is a graphics display controller with an on-chip geometry processor and digital video capture facility. It can be connected to FCRAM.

Connecting the MB86292 to FCRAM which has lower latency upon a paging error speeds up the random access to memory, resulting in faster display and drawing. In addition, integrating the geometry processor reduces the CPU load, thereby improving the performance of the entire system.

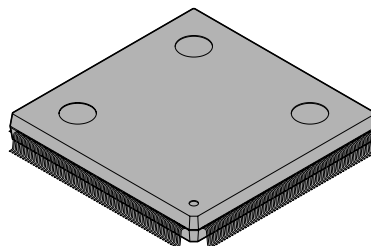
### ■ FEATURES

- Operating frequency : 100 MHz (External clock of 14.32 MHz Max)
- Geometry processor : Capable of executing operations for geometric transformation and surface front/rear evaluation.
- Memory block : Capable of connecting SDRAM and FCRAM
- Video capture block : Embedded facility to capture digital video images, for example, from TV, capable of easily implementing "Picture in Picture" and video graphics superimposing.
- Host interface : Enables direct connection to various CPUs (Fujitsu SparcLite, Hitachi SH3/4 or NEC V83x) .

*(Continued)*

### ■ PACKAGE

256-pin plastic QFP



(FPT-256P-M09)

*(Continued)*

- Drawing features :
  - Drawing at a peak rate of 800 Mpixel/s (at an internal operating frequency of 100 MHz)
  - 2D drawing functions : Point, line, triangle, polygon, BLT and pattern drawing
  - 3D drawing functions : Point, line, triangle drawing and hidden surface removal by Z-buffering
  - Special effects : Anti-aliasing, bold/dashed-line processing, alpha blending, Gouraud shading, texture mapping (bilinear filtering, perspective correct) , and tiling
- Display features :
  - Maximum display resolution supported : 1024 × 768 pixels
  - Color display either with a color palette of 8 Bit/Pixel or directly using 5-bit RGB colors of 16 Bit/Pixel
  - Overlaying four layers of screen, of which two lower layers can be divided into the left and right parts
  - Supporting two 64 Pixel × 64 Pixel hardware cursors
  - Output of analog RGB and digital RGB signals
  - Capable of superimposing using an external synchronization mode
- Power-supply voltage : Two power supplies at  $2.5 \pm 0.2$  V, for internal circuits and  $3.3 \pm 0.2$  V for I/O parts
- Package : PlasticQFP with 256 pins (with a lead pitch of 0.4 mm)
- Process technology : CMOS 0.25  $\mu$ m

## PIN ASSIGNMENT

WE0	1	256 CS
WE1	2	255 BS
WE2	3	254 RD
WE3	4	253 RESET
BCLKI	5	252 VSS
MODE0	6	251 VDDL
MODE1	7	250 VDDH
MODE2	8	249 DTACK/TC
TESTH	9	248 DRACK/DMAAK
TESTH	10	247 A24
VDDH	11	246 A23
VDDL	12	245 A22
VSS	13	244 A21
RDY	14	243 A20
DREQ	15	242 A19
INT	16	241 A18
D0	17	240 A17
D1	18	239 A16
D2	19	238 A15
D3	20	237 A14
D4	21	236 VSS
D5	22	235 VDDL
VDDH	23	234 A13
VSS	24	233 A12
VDDL	25	232 A11
D6	26	231 A10
D7	27	230 A9
D8	28	229 A8
D9	29	228 A7
D10	30	227 A6
D11	31	226 A5
D12	32	225 A4
D13	33	224 A3
D14	34	223 A2
D15	35	222 VSS
D16	36	221 VDDH
D17	37	220 OSCCNT
D18	38	219 PLLVDD
VSS	39	218 S
VDDL	40	217 OSCOUT
D19	41	216 PLLVSS
D20	42	215 CLK
D21	43	214 VSS
D22	44	213 VDDL
D23	45	212 CLKSELO
D24	46	211 CLKSEL1
D25	47	210 CKM
D26	48	209 V17
D27	49	208 V16
D28	50	207 V15
D29	51	206 V14
D30	52	205 V11
D31	53	205 V10
VDDH	54	205 V10
VDDL	55	202 V13
VSS	56	202 V13
MD0	57	204 CCLK
MD1	58	201 V12
MD2	59	200 VSS
MD3	60	199 VDDL
MD4	61	188 VDDH
MD5	62	187 DCLKI
MD6	63	186 TESTH
MD7	64	185 TESTH
65		184 TESTH
VSS	66	183 VDDH
MD8	67	182 R7
MD9	68	181 R6
MD10	69	180 R5
MD11	70	179 R4
MD12	71	178 R3
MD13	72	177 G7
MD14	73	176 G6
MD15	74	175 G5
MD16	75	174 G4
MD17	76	173 G3
MD18	77	172 B7
MD19	78	171 B6
MD20	79	170 B5
MD21	80	169 B4
MD22	81	168 B3
VDDL	82	167 VSS
VSS	83	166 VDDL
VSS	84	165 VDDH
MD23	85	164 MD63
MD24	86	163 MD62
MD25	87	162 MD61
MD26	88	161 MD60
MD27	89	160 MD59
MD28	90	159 MD58
MD29	91	158 MD57
MD30	92	157 MD56
MD31	93	156 MD55
MA0	94	155 MD54
MA1	95	154 MD53
MA2	96	153 MD52
MA3	97	152 MD51
MA4	98	151 MD50
VDDH	99	150 MD49
VSS	100	149 MD48
MCLKO	101	148 VSS
MA5	102	147 VDDL
MA6	103	146 MD47
MA7	104	145 MD46
MA8	105	144 MD45
MA9	106	143 MD44
MA10	107	142 MD43
MA11	108	141 MD42
MA12	109	140 MD41
MA13	110	139 MD40
MVE	111	138 MD39
VDDH	112	137 MD38
VDDL	113	136 MD37
VSS	114	135 MD36
MDQM0	115	134 MD35
MDQM1	116	133 MD34
MDQM2	117	132 MD33
MDQM3	118	131 MD32
MDQM4	119	130 VSS
MDQM5	120	129 VDDH
MDQM6	121	
MDQM7	122	
MCRAS	123	
MCA5	124	
VDDL	125	
VSS	126	
MCLKI	127	
RGBEN	128	

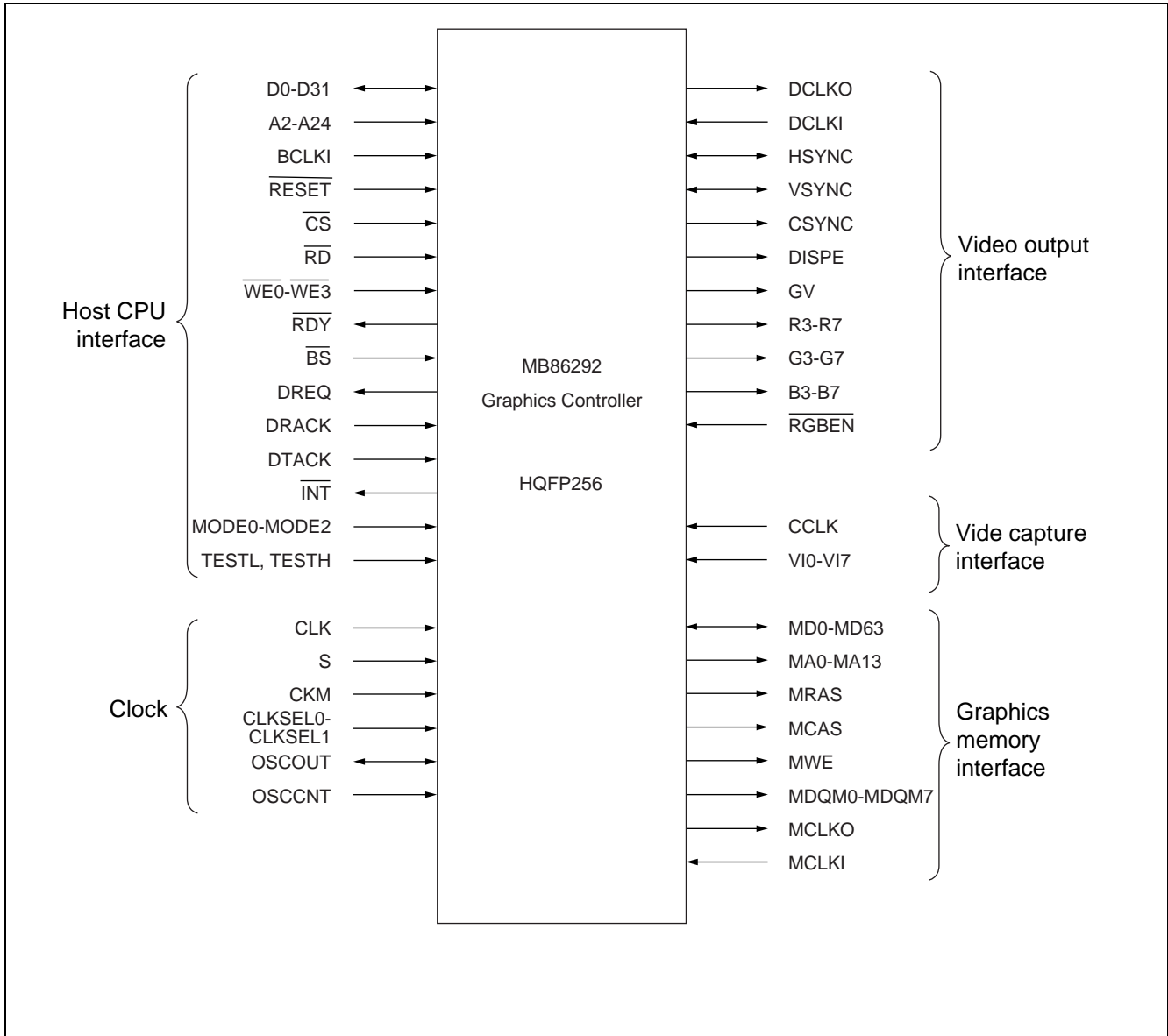
- VSS/PLLVSS : Ground
- VDDH : 3.3 V power supply
- VDDL/PLLVDD : 2.5 V power supply
- PLLVDD : PLL power supply
- OPEN : Do not connect anything.
- TESTH : Input the high level.

Notes :

- The PLLVDD should be separated on the board.
- Insert a bypass capacitor with a superior high-frequency characteristic between the power supply and ground.  
Place the capacitor as near the pins as possible.

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## ■ PIN DESCRIPTION



• Host Interface Pins

Pin Name	Input/output	Function
MODE0-MODE2	Input	Host CPU mode/Ready mode select
$\overline{\text{RESET}}$	Input	Hardware reset
D0-D31	Input/output	Host CPU bus data
A2-A24	Input	Host CPU bus address (Connect A24 to $\overline{\text{MWR}}$ in V832 mode.)
BCLKI	Input	Host CPU bus clock
$\overline{\text{BS}}$	Input	Bus cycle start signal
$\overline{\text{CS}}$	Input	Chip select signal
$\overline{\text{RD}}$	Input	Read strobe signal
$\overline{\text{WE0}}$	Input	D0-D7 write strobe signal
$\overline{\text{WE1}}$	Input	D8-D15 write strobe signal
$\overline{\text{WE2}}$	Input	D16-D23 write strobe signal
$\overline{\text{WE3}}$	Input	D24-D31 write strobe signal
$\overline{\text{RDY}}$	Output Tristate	Wait request signal ("0" for wait state with SH3; "1" for wait state with SH4, V832, or SPARClite)
DREQ	Output	DMA request signal (active low with both SH and V832)
DRACK/ DMAAK	Input	DMA request acknowledge signal (Connect this to DMAAK in V832 mode. Active high with both SH and V832.)
DTACK/ $\overline{\text{TC}}$	Input	DMA transfer strobe signal (Connect this to $\overline{\text{TC}}$ in V832 mode. SH = active high, V832 = active low)
$\overline{\text{INT}}$	Output	Host CPU interrupt signal (SH = active low, V832 = active high)
TESTH	Input	Test signal

Note : The host interface can connect the MB86292 to the SH4 (SH7750) or SH3 (SH7709) from Hitachi Ltd. the V832 from NEC, or to the SPARClite (MB86833) from Fujitsu without any external circuit in between. (Using the SRAM interface allows the MB86292 to use another CPU.) The host CPU is set by the MODE0 and MODE1 pins as shown below.

MODE1 pin	MODE0 pin	CPU Type
L	L	SH3
L	H	SH4
H	L	V832
H	H	SPARClite

Note : The MODE2 pin can be used to set the Ready signal level to be used upon completion of the bus cycle. To use the MODE2 signal at "H" level, set the software setting to two cycles.

MODE2 pin	Ready signal mode
L	Set $\overline{\text{RDY}}$ signal to "Not Ready" level upon completion of bus cycle.
H	Set $\overline{\text{RDY}}$ signal to "Ready" level upon completion of bus cycle.

# MB86292

- Notes :
- The host interface transfers data signals at a fixed width of 32 bits.
  - There are 23 lines for address signals handled in double words (32 bits) and 32 Mbytes of address space.
  - The external bus can be used at an operating frequency of 100 MHz maximum.
  - The  $\overline{\text{RDY}}$  signal at the low level sets the ready state in the SH4 or V832 mode; the signal at the low level sets the wait state in the SH3 mode. Note that the  $\overline{\text{RDY}}$  signal is a tristate output signal synchronized to the rise of BCLKI.
  - The host interface supports DMA transfer using an external DMA controller.
  - The host interface generates a host processor interrupt signal.
  - The  $\overline{\text{RESET}}$  pin requires low level input of at least 300  $\mu\text{s}$  after setting "S" (PLL reset signal) to high level.
  - Fix the TEST signal at high level.
  - In the V832 mode, connect the following pins as specified :

ORCHID Pin Name	V832 Signal Name
A24	$\overline{\text{MWR}}$
DTACK	$\overline{\text{TC}}$
DRACK	DMAAK

• Video Output Interface Pins

Pin Name	Input/output	Function
DCLKO	Output	Display dot clock signal output
DCLKI	Input	Dot clock signal input
HSYNC	Input/output	Horizontal sync signal output Horizontal sync signal input in external synchronization mode
VSYNC	Input/output	Vertical sync signal output Vertical sync signal input in external synchronization mode
CSYNC	Output	Composite sync signal output
DISPE	Output	Display effective period signal
GV	Output	Graphics/video select signal
R3-R7	Output	Digital video (R) signal output
G3-G7	Output	Digital video (G) signal output
B3-B7	Output	Digital video (B) signal output
$\overline{\text{RGBEN}}$	Input	RGB2-0 output/memory bus (MD63-55) select signal

- Notes :
- The video output interface outputs RGB pieces of five-bit display data by default. It can output RGB pieces of eight-bit display data depending on conditions. R0-2, G0-2, and B0-2 can be output to MD61-MD63, MD58-MD60, and MD58-MD60, respectively, by fixing  $\overline{\text{RGBEN}}$  to 0. When eight-bit RGB output is selected, only the 32-bit memory bus width mode can be used.
  - Using an additional external circuit, the video output interface can generate composite video signals.
  - The video output interface can provide display synchronized with external video. The mode for synchronization with the DCLKI signal can be selected as well as the mode for synchronization with a set dot clock as for normal display.
  - The HSYNC and VSYNC signals must be pulled up outside the LSI as they enter the input state upon reset.
  - The GV signal serves to switch between graphics and video for chroma keying. The pin outputs a low level signal to select video.

- Video Capture Interface Pins

Pin Name	Input/output	Function
CCLK	Input	Digital video input clock signal input
VI0-VI7	Input	Digital video data input

Note : The video capture interface inputs digital video signals in the ITU-RBT-656 format.

- Graphics Memory Interface Pins

Pin Name	Input/output	Function
MD0-MD54	Input/output	Graphics memory bus data
MD55-MD63	Input/output	Graphics memory bus data or RGB0-RGB2 output
MA0-MA13	Output	Graphics memory bus data
MRAS	Output	Row address strobe
MCAS	Output	Column address strobe
MWE	Output	Write enable
MDQM0-MDQM7	Output	Data mask
MCLKO	Output	Graphics memory clock output
MCLKI	Input	Graphics memory clock input

Notes : • The graphics memory interface connects the MB86292 to the external memory used for graphical image data. The interface can directly accept 128-Mbit SDRAM or 64-Mbit SDRAM (with a 16-bit or 32-bit data bus) without any external circuit.

- Memory bus data can be selected between 64 bits and 32 bits. To use 32-bit data, leave the MD32-MD63 and MDQM4-7 pins open in the eight-bit RGB output mode ( $\overline{\text{RGBEN}}$  pin = 0) or the MD32-MD54 and MDQM4-7 pins open in the eight-bit RGB output mode ( $\overline{\text{RGBEN}}$  pin = 0).
- Connect the MCLKI pin to the MCLKO pin.
- When  $\overline{\text{RGBEN}}$  is fixed to 1, MD55-MD63 can be used as graphics memory bus data. When  $\overline{\text{RGBEN}}$  is fixed to 0, RGB0-2 is output.

- Clock Input Pins

Pin Name	Input/output	Function
CLK	Input	Clock input signal
S	Input	PLL reset signal
CKM	Input	Clock mode signal
CLKSEL [1 : 0]	Input	Clock rate select signal
OSCOU <sup>*1</sup>	Input/output	For connection of crystal oscillator (Reserved)
OSCCNT <sup>*2</sup>	Input	Crystal oscillator select pin (Reserved)

\*1 : Do not connect anything.

\*2 : Input the "H" level.

Notes : • The clock input block inputs the clock signal that serves as the basis for the reference clock for the internal operating clock and display dot clock. Usually input 4 Fsc (= 14.31818 MHz for NTSC). The internal PLL generates the internal operating clock signal of 100 MHz and the display reference clock signal of 200 MHz.

- The internal operating clock signal to be used can be selected between the clock signal (100 MHz) generated by the internal PLL and the bus clock BCLKI input to the host CPU interface. Select the BCLKI input to use the host CPU bus at 100 MHz.

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CKM	Clock Mode
L	Select internal PLL output.
H	Select host CPU bus clock (BCLKI).

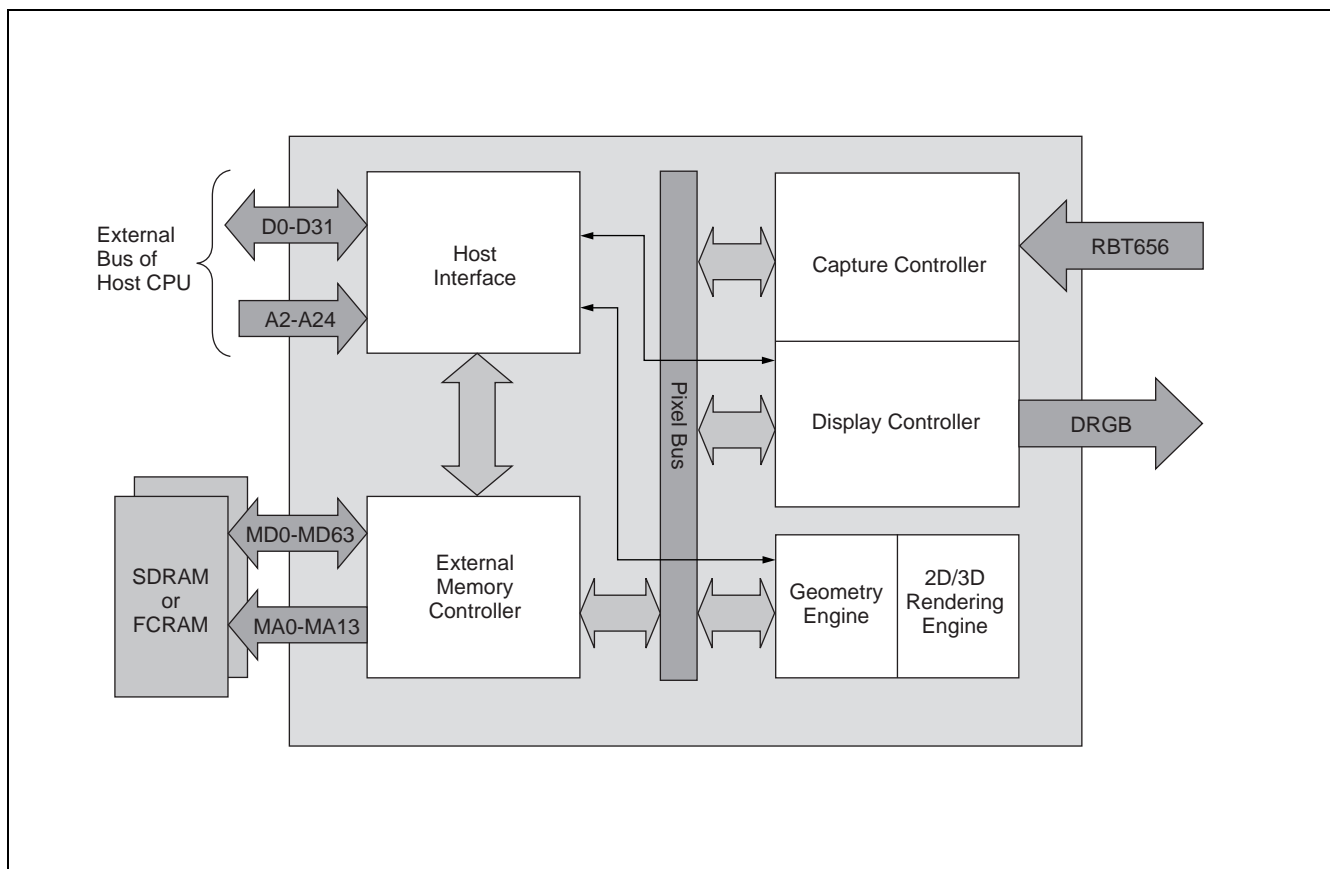
- Use the CLKSEL pin to select the input clock frequency for using the internal PLL with CKM = L.

CLKSEL1	CLKSEL0	Input Clock Frequency	Multiplier	Display reference clock
L	L	Input 13.5 MHz.	× 15	202.5 MHz
L	H	Input 14.32 MHz.	× 14	200.48 MHz
H	L	Input 17.73 MHz.	× 11	195.03 MHz
H	H	Reserved	—	—

Note : Immediately after turning the power supply on, input a pulse whose low level period is 500 ns or more to the S pin before setting it to high level. After the S signal goes high, input the  $\overline{\text{RESET}}$  signal at low level for 300  $\mu\text{s}$  or more.



## ■ BLOCK DIAGRAM



## ■ FUNCTION BLOCKS

### • Host Interface

This block allows the MB86292 to be connected to the SH3 or SH4 microprocessor from Hitachi Ltd., the V83x microprocessor from NEC, or to the SPARCLite from Fujitsu without any external circuit in between. The block provides an interface to transfer display list and texture pattern data directly from main memory to this device's graphics memory or internal register using the external DMA controller.

### • External Memory Controller

This block connects external SDRAM or FCRAM. The data bus can be selected between 64 bits and 32 bits and the maximum operating frequency is 100 MHz.

### • Display Controller

This block contains a three-channel, eight-bit D/A converter to output analog RGB signals. The block has eight-bit RGB digital video outputs, allowing an external digital video encoder to be connected. The block supports resolutions of up to XGA (1024×768 pixels), enabling flexible setting.

### • Set-up Engine

The on-chip geometry engine executes mathematical operations required for graphics processing precisely using the fronting-point format. The geometry engine executes the required geometry processes selected depending on the drawing mode and primitive type settings up to the final drawing process.

### • 2D/3D Rendering Engine

This block draws images in two or three dimensions.

#### 2D drawing

The block provides the anti-aliasing and alpha blending functions to display high-quality images even on a low-resolution LCD.

#### 3D drawing

The block provides true 3D drawing functions such as perspective texture mapping and Gouraud shading.

## ■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min	Max	
Power supply voltage	V <sub>DDL</sub> *	- 0.5	3.0	V
	V <sub>DDH</sub>	- 0.5	4.0	
Input voltage	V <sub>I</sub>	- 0.5	V <sub>DDH</sub> + 0.5 (< 4.0)	V
Output current	I <sub>O</sub>	- 13	+ 13	mA
Power pin current	I <sub>POW</sub>	60	60	mA
Ambient storage temperature	T <sub>stg</sub>	- 55	+ 125	°C

\* : The PLL power supply is included.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

## ■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power supply voltage	V <sub>DDL</sub> *	2.3	2.5	2.7	V
	V <sub>DDH</sub>	3.0	3.3	3.6	
Input voltage ("H" level)	V <sub>IH</sub>	2.0	—	V <sub>DDH</sub> + 0.3	V
Input voltage ("L" level)	V <sub>IL</sub>	- 0.3	—	+ 0.8	V
Ambient operating temperature	T <sub>A</sub>	- 40	—	+ 85	°C

\* : The PLL power supply is included.

Notes : • The VDDL and VDDH power supplies can be turned on or off in either order.

Note, however, that the VDDH voltage must not be applied alone continuously for several seconds.

- Do not input the HSYNC, VSYNC, or EO signal with the power-supply voltage not applied. (See "Input voltage" in "■ ABSOLUTE MAXIMUM RATINGS".)
- After turning the power on, input a pulse remaining at low level for at least 500 ns to the S pin. Then, set the S pin to high level and input the RESET signal held at low level for at least 300 μs.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

## ■ ELECTRICAL CHARACTERISTICS

### 1. DC Characteristics

(VDDL = 2.5 ± 0.2 V, VDDH = 3.3 ± 0.3, VSS = 0.0 V, Ta = 0 °C to + 70 °C)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Output voltage ("H" level) *1	V <sub>OH</sub>	V <sub>DDH</sub> - 0.2	—	V <sub>DDH</sub>	V
Output voltage ("L" level) *2	V <sub>OL</sub>	0.0	—	0.2	V
Output current ("H" level)	I <sub>OH1</sub> *3	- 2.0	—	—	mA
	I <sub>OH2</sub> *4	- 4.0			
	I <sub>OH3</sub> *5	- 8.0			
Output current ("L" level)	I <sub>OL1</sub> *3	2.0	—	—	mA
	I <sub>OL2</sub> *4	4.0			
	I <sub>OL3</sub> *5	8.0			
Input leakage current	I <sub>L</sub>	—	—	± 5	μA
Pin capacitance	C	—	—	16	pF

\*1 : Value when -100 μA current flows into output pins.

\*2 : Value when 100 μA current flows into output pins.

\*3 : Output characteristics of the MD0-63 and MDQM0-7 signal.

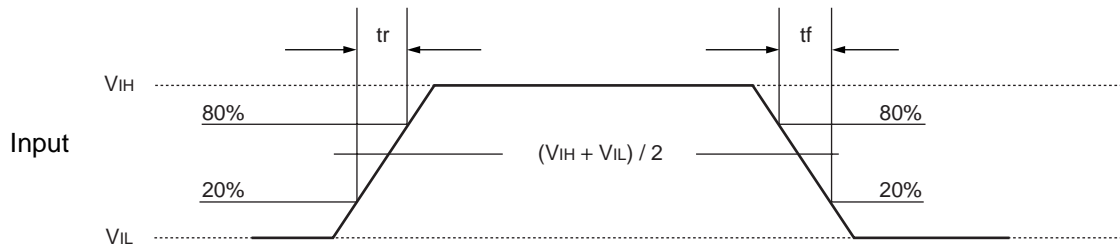
\*4 : Output characteristics of the signals other than those in \*3 and \*5

\*5 : MCLKO signal output characteristics

## 2. AC Characteristics

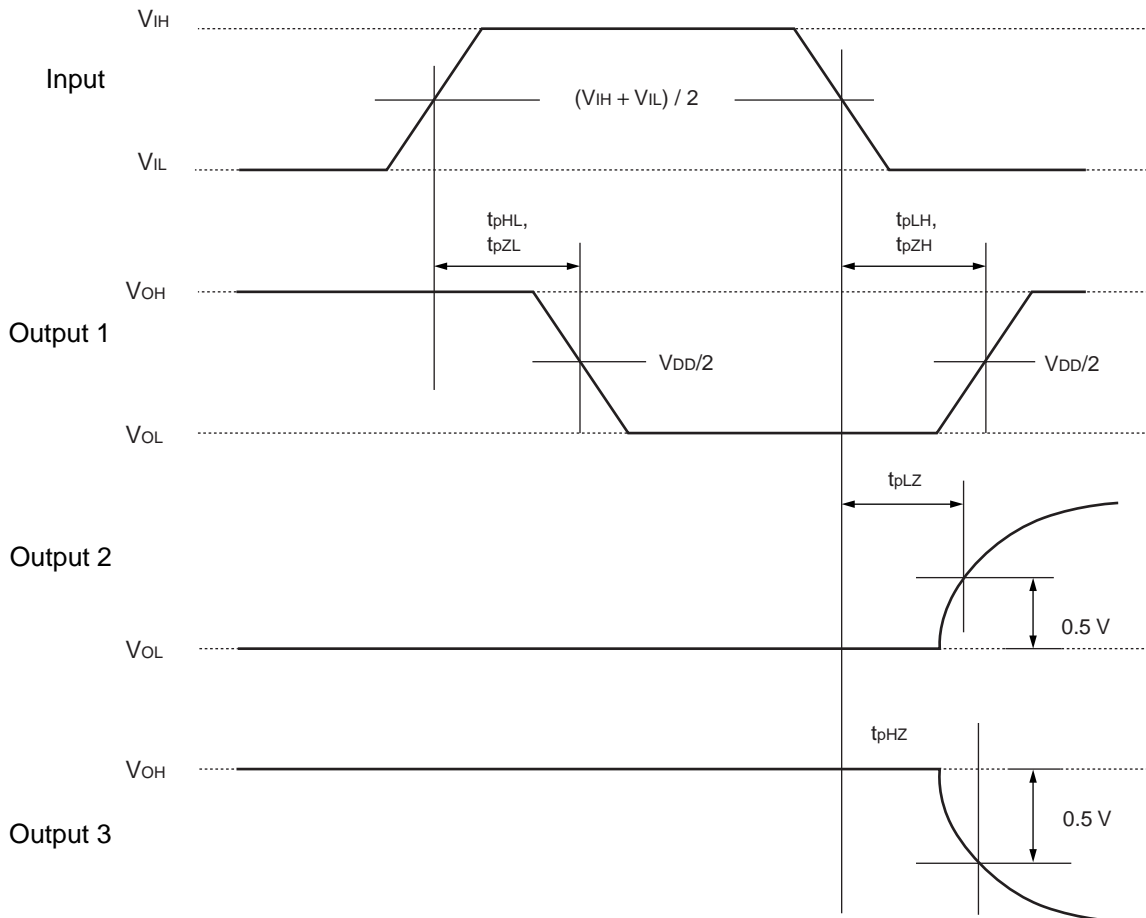
( $V_{IH} = 2.0\text{ V}$ ,  $V_{IL} = 0.8\text{ V}$ )

- Input measurement conditions



- $t_r, t_f \leq 5\text{ ns}$
- Input measurement standard :  $(V_{IH} + V_{IL}) / 2$

- Output measurement conditions



- Output measurement standard :  $t_{pLZ} : V_{OL} + 0.5\text{ V}$   
 $t_{pHZ} : V_{OH} - 0.5\text{ V}$   
Else :  $V_{DD}/2$

# MB86292

## (1) Host Interface

### • Clock

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
BCLKI frequency	$f_{\text{BCLKI}}$	—	—	—	100	MHz
BCLKI H period	$t_{\text{HBCLKI}}$	—	1	—	—	ns
BCLKI L period	$t_{\text{LBCLKI}}$	—	1	—	—	ns

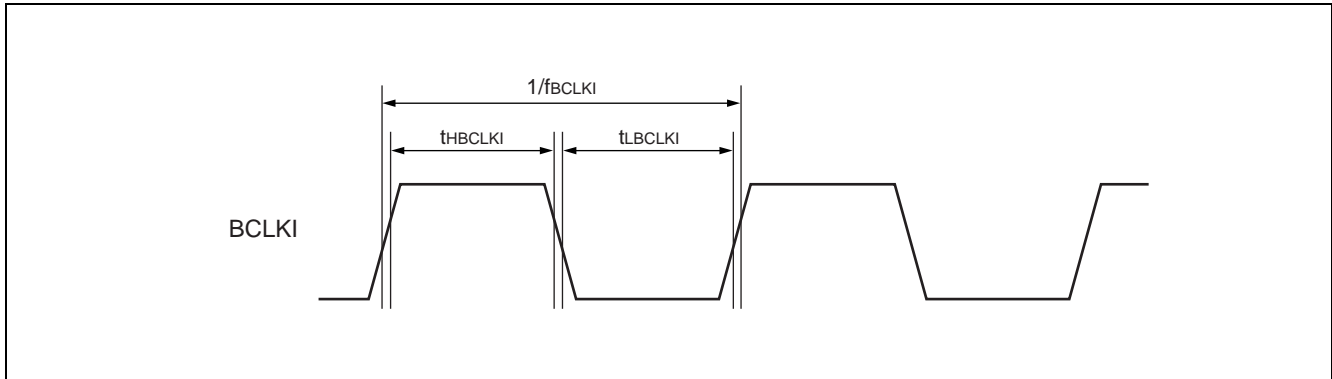
### • Host interface signals

(Operating condition : External load of 20 pF)

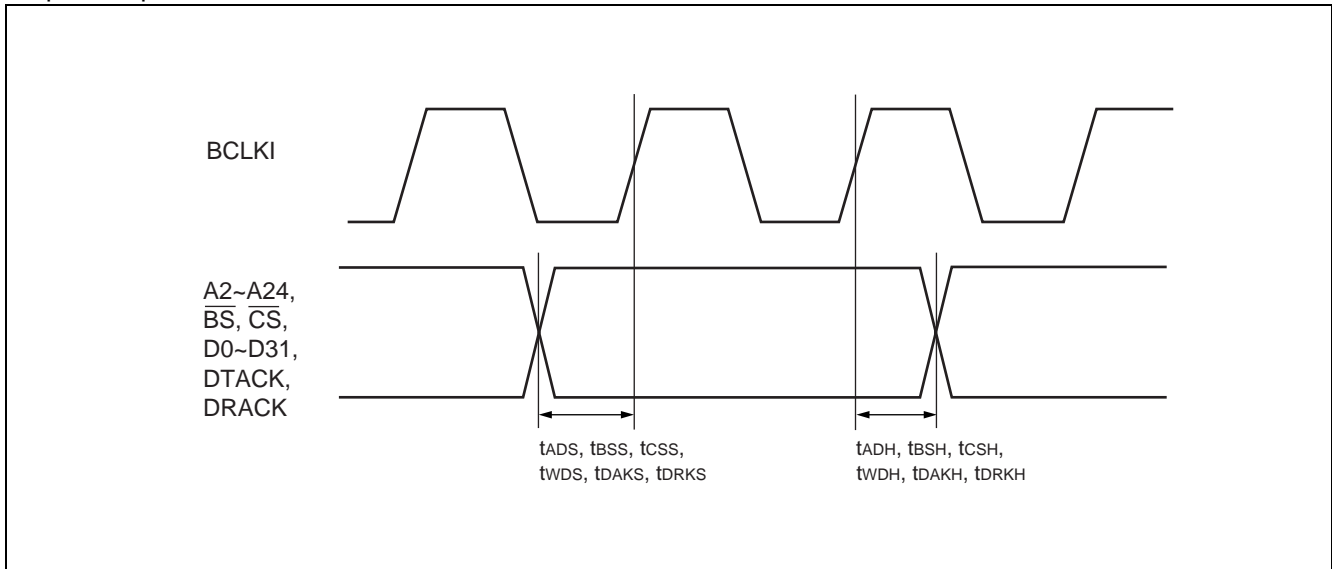
Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Address setup time	$t_{\text{ADS}}$	—	3.0	—	—	ns
Address hold time	$t_{\text{ADH}}$	—	1.0	—	—	ns
$\overline{\text{BS}}$ setup time	$t_{\text{BSS}}$	—	3.5	—	—	ns
$\overline{\text{BS}}$ hold time	$t_{\text{BSH}}$	—	0.0	—	—	ns
$\overline{\text{CS}}$ setup time	$t_{\text{CSS}}$	—	3.5	—	—	ns
$\overline{\text{CS}}$ hold time	$t_{\text{CSH}}$	—	0.0	—	—	ns
$\overline{\text{RD}}$ setup time	$t_{\text{RDS}}$	—	3.0	—	—	ns
$\overline{\text{RD}}$ hold time	$t_{\text{RDH}}$	—	0.0	—	—	ns
$\overline{\text{WE}}$ setup time	$t_{\text{WES}}$	—	5.5	—	—	ns
$\overline{\text{WE}}$ hold time	$t_{\text{WEH}}$	—	0.0	—	—	ns
Write data setup time	$t_{\text{WDS}}$	—	3.5	—	—	ns
Write data hold time	$t_{\text{WDH}}$	—	0.0	—	—	ns
DTACK setup time	$t_{\text{DAKS}}$	—	3.5	—	—	ns
DTACK hold time	$t_{\text{DAKH}}$	—	0.0	—	—	ns
DRACK setup time	$t_{\text{DRKS}}$	—	4.0	—	—	ns
DRACK hold time	$t_{\text{DRKH}}$	—	0.0	—	—	ns
Read data delay time (to $\overline{\text{RD}}$ )	$t_{\text{RDDZ}}$	—	2.5	—	8.5	ns
Read data delay time	$t_{\text{RDD}}$	—	4.0	—	10.5	ns
$\overline{\text{RDY}}$ delay time (to $\overline{\text{CS}}$ )	$t_{\text{RDYDZ}}$	—	2.0	—	6.0	ns
$\overline{\text{RDY}}$ delay time	$t_{\text{RDYD}}$	—	2.5	—	6.5	ns
$\overline{\text{INT}}$ delay time	$t_{\text{INTD}}$	—	2.5	—	7.0	ns
DREQ delay time	$t_{\text{DRQD}}$	—	2.5	—	6.5	ns
MODE hold time	$t_{\text{MODH}}$	*	—	—	20.0	ns

\* : Hold time for reset cancellation

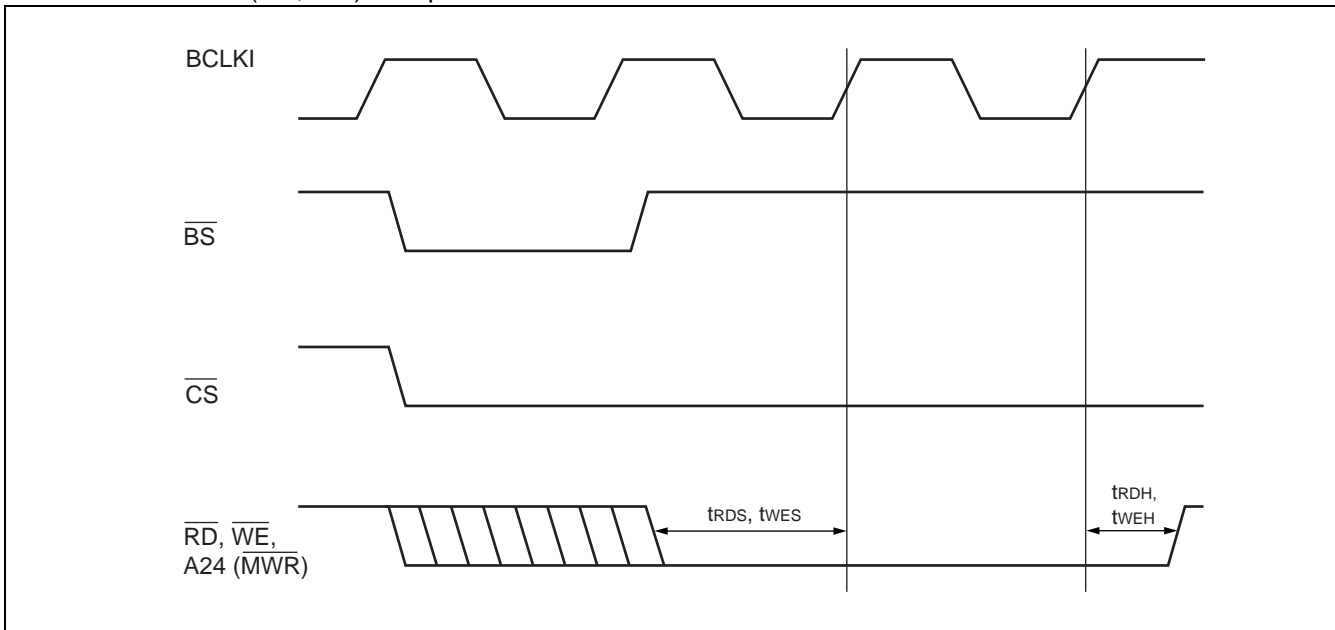
• Clock



• Input setup and hold times

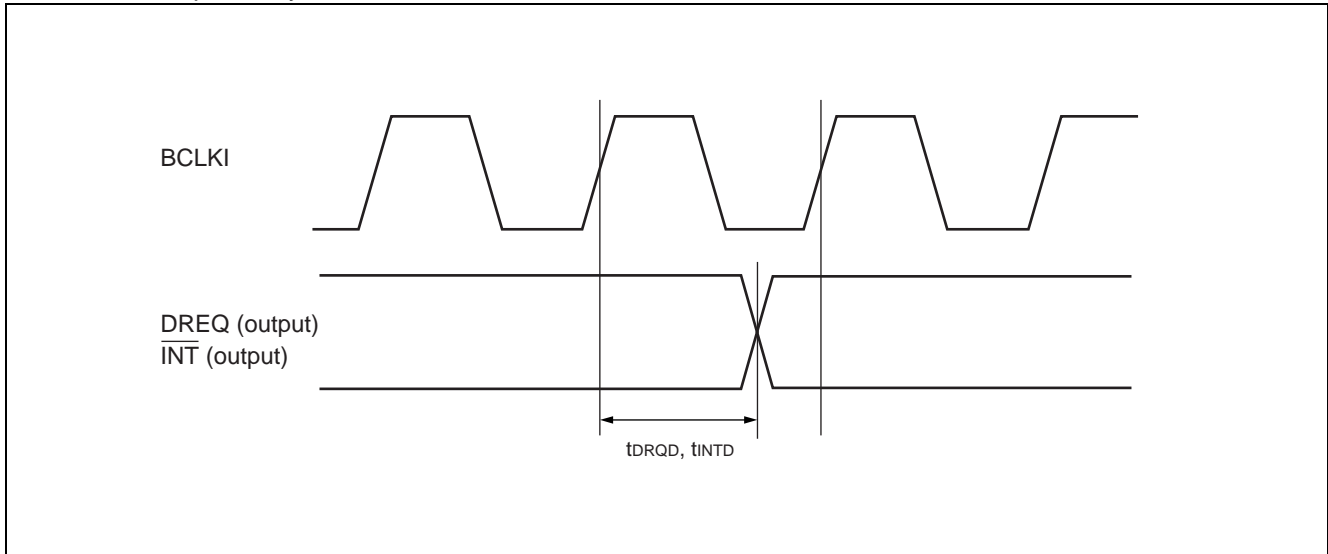


• Read/write enable ( $\overline{RD}$ ,  $\overline{WE}$ ) setup and hold times

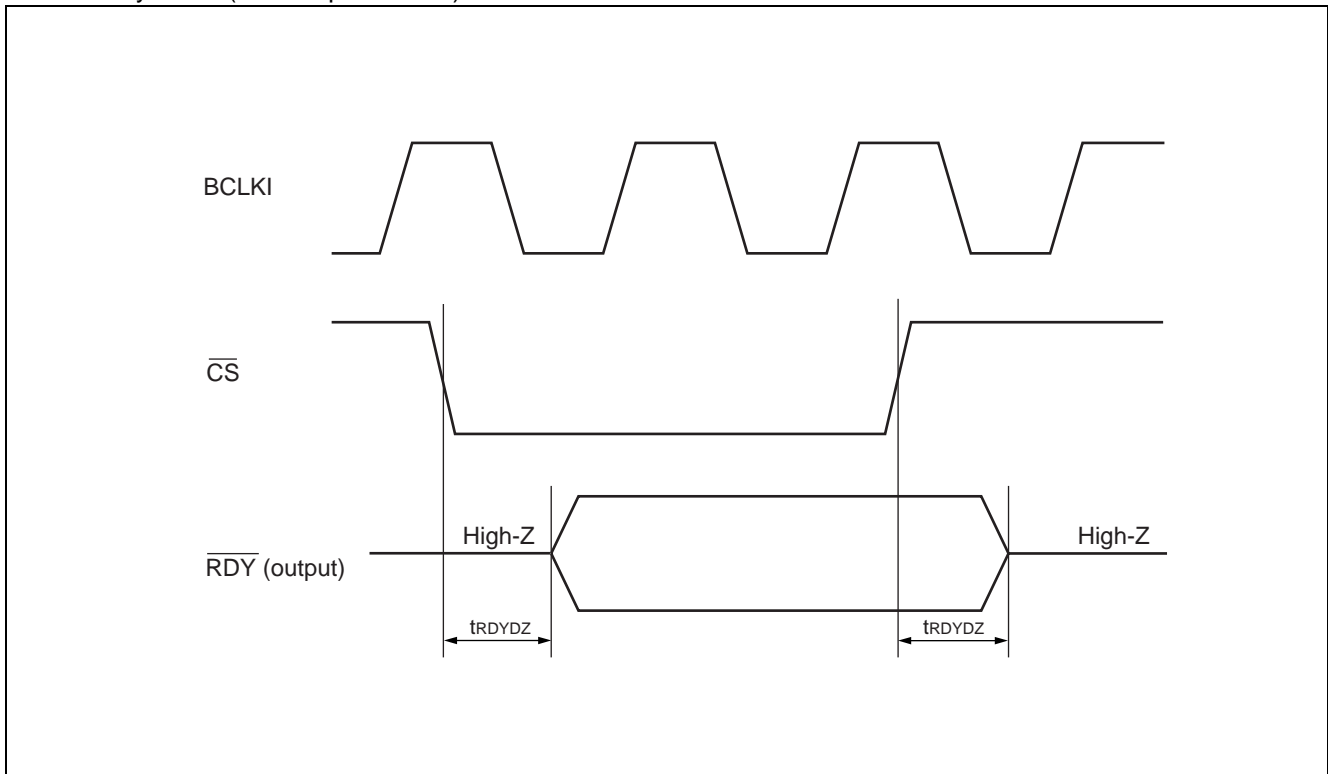


# MB86292

- DREQ/ $\overline{\text{INT}}$  output delay time



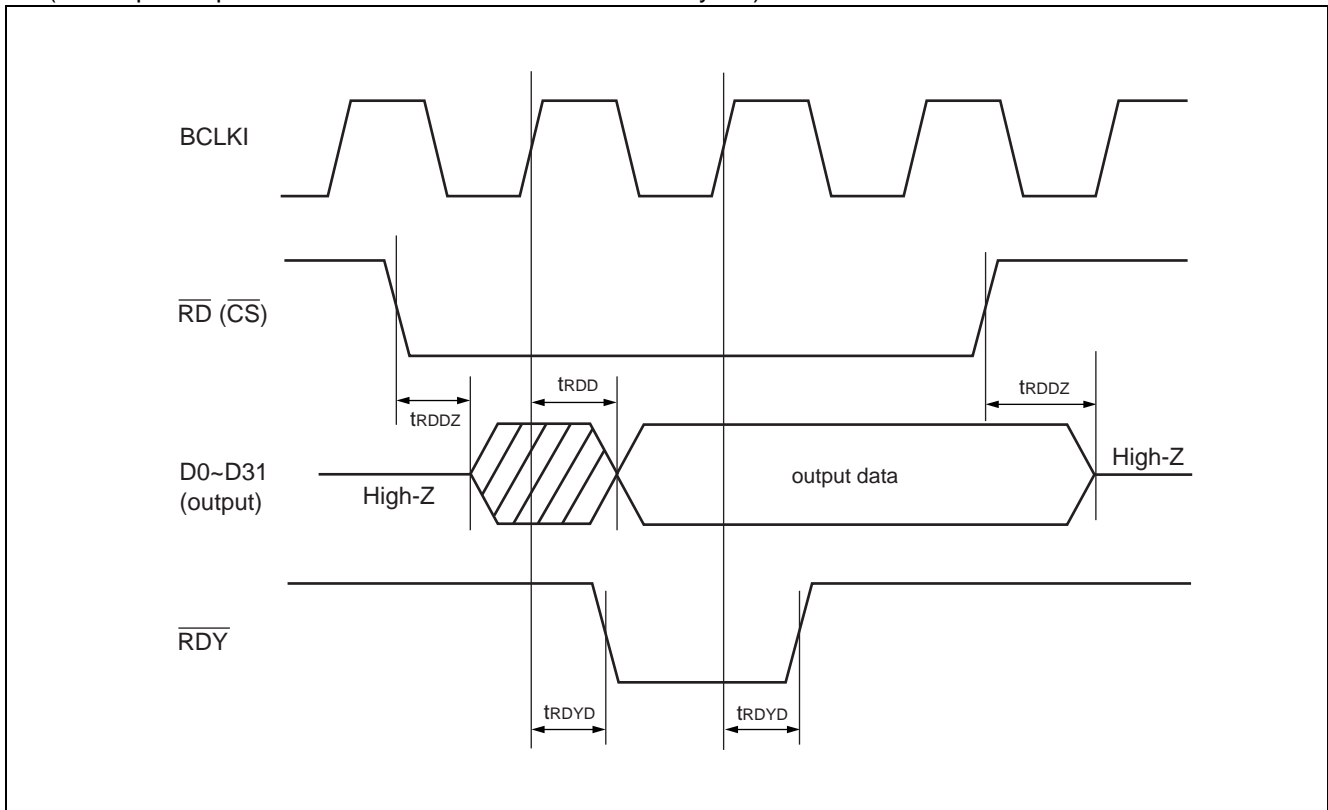
- $\overline{\text{RDY}}$  delay value (with respect to  $\overline{\text{CS}}$ )



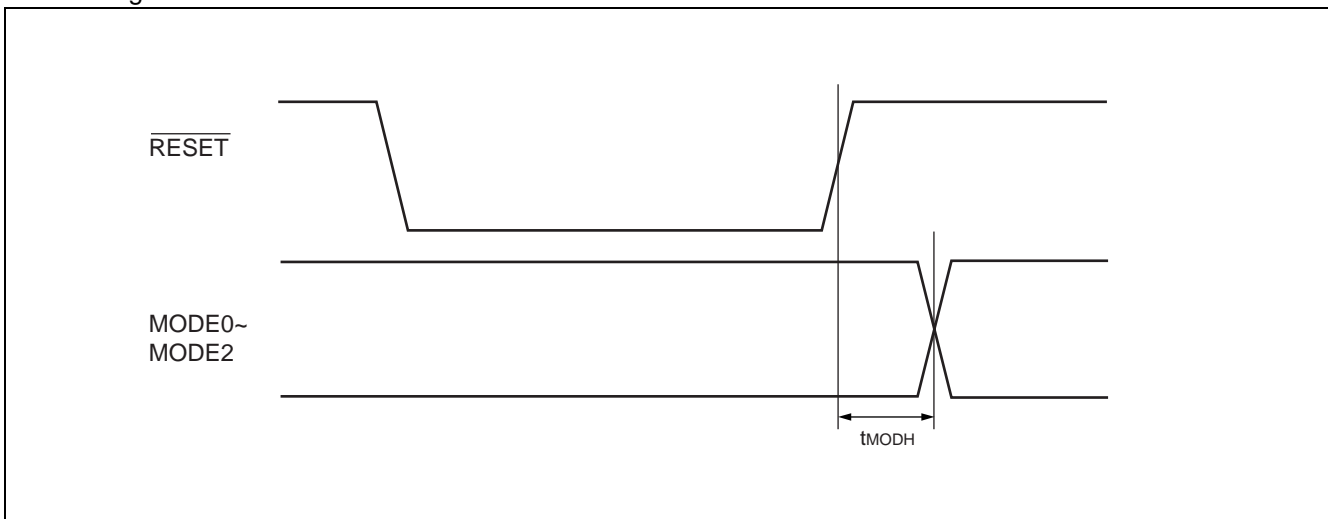


- $\overline{RDY}$ , D output delay values

(The D pin outputs effective data from the  $\overline{RDY}$  assert cycle.)



- MODE signal hold time



# MB86292

## (2) Video Interface

### • Clock

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
CLK frequency	f <sub>CLK</sub>	—	—	14.318	—	MHz
CLK H period	t <sub>HCLK</sub>	—	25	—	—	ns
CLK L period	t <sub>LCLK</sub>	—	25	—	—	ns
DCLKI frequency	f <sub>DCLKI</sub>	—	—	—	67	MHz
DCLKI H period	t <sub>HDCLKI</sub>	—	5	—	—	ns
DCLKI L period	t <sub>LDCLKI</sub>	—	5	—	—	ns
DCLKO frequency	f <sub>DCKO</sub>	—	—	—	67	MHz

### • Input signals

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
HSYNC input pulse width	t <sub>WHSYNC0</sub>	*1	3	—	—	clock
	t <sub>WHSYNC1</sub>	*2	3	—	—	clock
HSYNC input setup time	t <sub>SHSYNC</sub>	*2	10	—	—	ns
HSYNC input hold time	t <sub>HHSYNC</sub>	*2	10	—	—	ns
VSYNC input pulse width	t <sub>WHSYNC1</sub>	—	1	—	—	HSYNC cycle

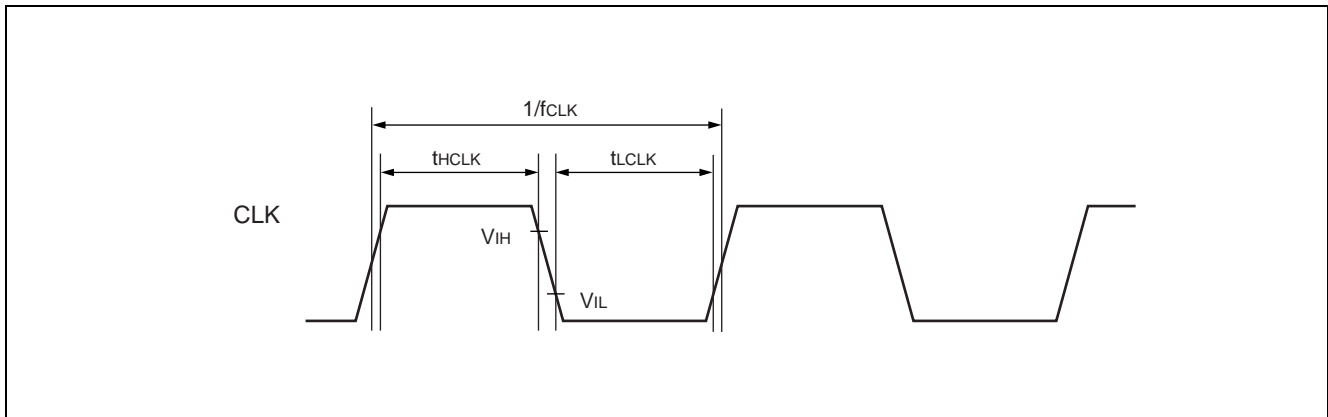
\*1 : Applied only in PLL synchronization mode (CKS = 0) . The reference clock is the internal PLL's output with Cycle = 1/ (14 f<sub>CLK</sub>) .

\*2 : Applied only in DCLKI synchronization mode (CKS = 1) . The reference clock is DCLKI.

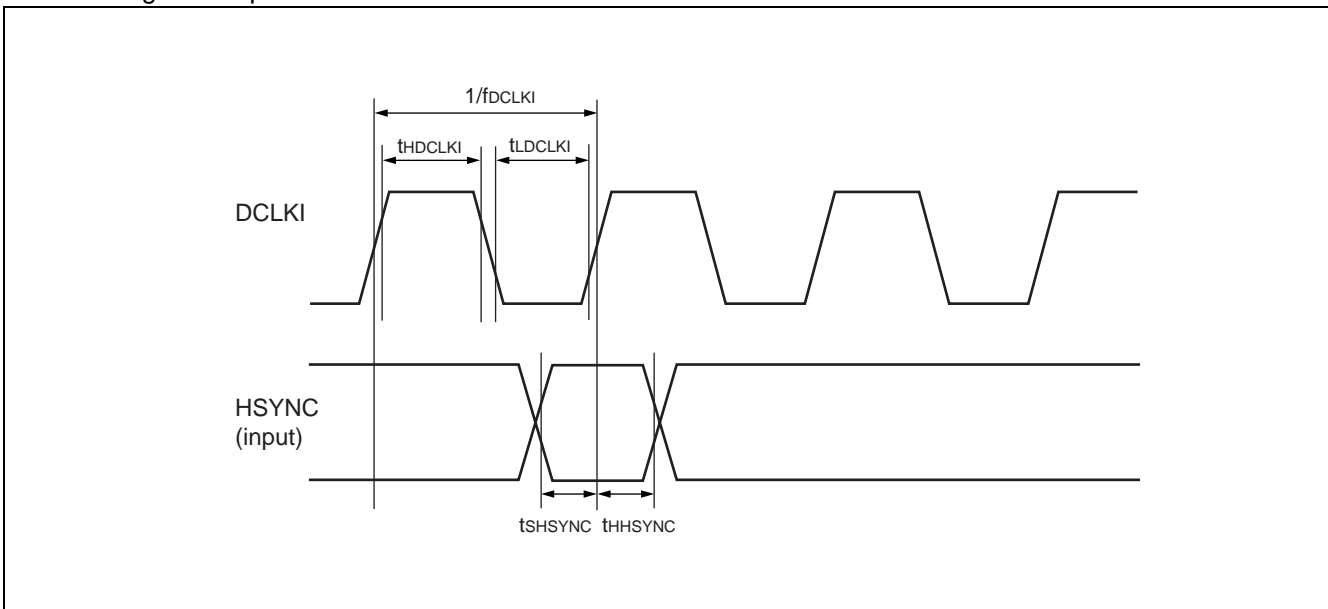
### • Output signals

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
RGB output delay time	t <sub>RGB</sub>	—	2	—	10	ns
DISPE output delay time	t <sub>DEO</sub>	—	2	—	10	ns
HSYNC output delay time	t <sub>DHSYNC</sub>	—	2	—	10	ns
VSYNC output delay time	t <sub>DVSYNC</sub>	—	2	—	10	ns
CSYNC output delay time	t <sub>DCSYNC</sub>	—	2	—	10	ns
GV output delay time	t <sub>DGV</sub>	—	2	—	10	ns

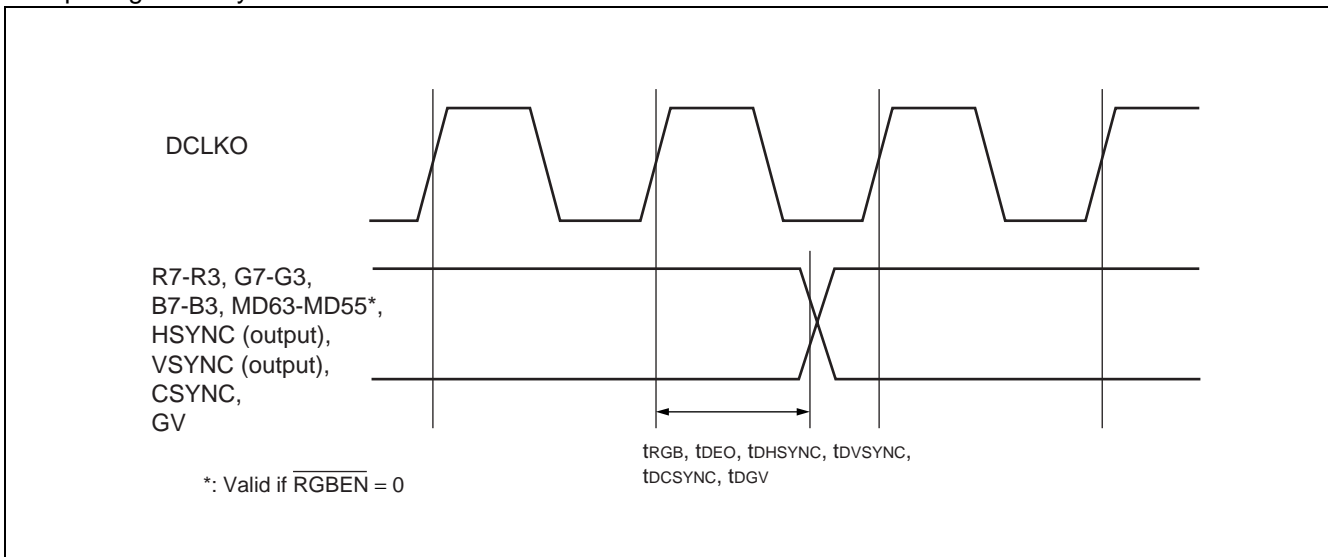
• Clock



• HSYNC signal setup and hold



• Output signal delay



## (3) Graphics Memory Interface

### • Clock

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
MCLKO frequency	f <sub>MCLKO</sub>	—	—	—	*	MHz
MCLKO H period	t <sub>HMCLKO</sub>	—	1.0	—	—	ns
MCLKO L period	t <sub>LMCLKO</sub>	—	1.0	—	—	ns
MCLKI frequency	f <sub>MCLKI</sub>	—	—	—	*	MHz
MCLKI H period	t <sub>HMCLKI</sub>	—	1.0	—	—	ns
MCLKI L period	t <sub>LMCLKI</sub>	—	1.0	—	—	ns
MCLKI delay to MCLKO	t <sub>OID</sub>	—	0.0	—	3.5	ns

\* : In BUS asynchronous mode, the frequency is half the internal PLL oscillation frequency. In Bus synchronous mode, the frequency is the same as BCLKI.

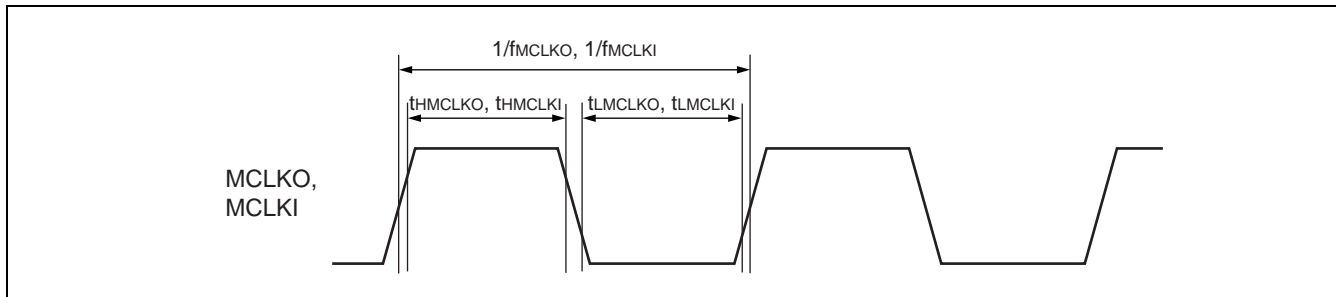
### • Input/output signals

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
MA, MRAS, MCAS, MWE setup time	t <sub>MADS</sub>	*1	3.2	—	—	ns
MA, MRAS, MCAS, MWE hold time	t <sub>MADH</sub>	*1	1.3	—	—	ns
MDQM data setup time	t <sub>MDQMDS</sub>	*1	3.2	—	—	ns
MDQM data hold time	t <sub>MDQMDH</sub>	*1	1.3	—	—	ns
MD output data setup time	t <sub>MDODS</sub>	*1	3.2	—	—	ns
MD output data hold time	t <sub>MDODH</sub>	*1	1.3	—	—	ns
MD input data setup time	t <sub>MDIDS</sub>	*2	3.0	—	—	ns
MD input data hold time	t <sub>MDIDH</sub>	*2	1.0	—	—	ns

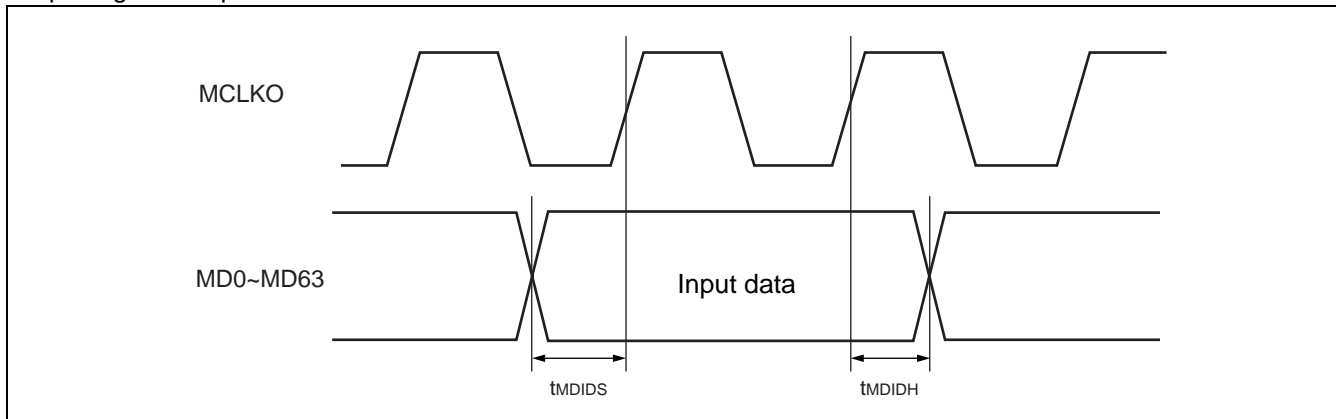
\*1 : Setup/hold time with respect to MCLKO

\*2 : Setup/hold time with respect to MCLKI

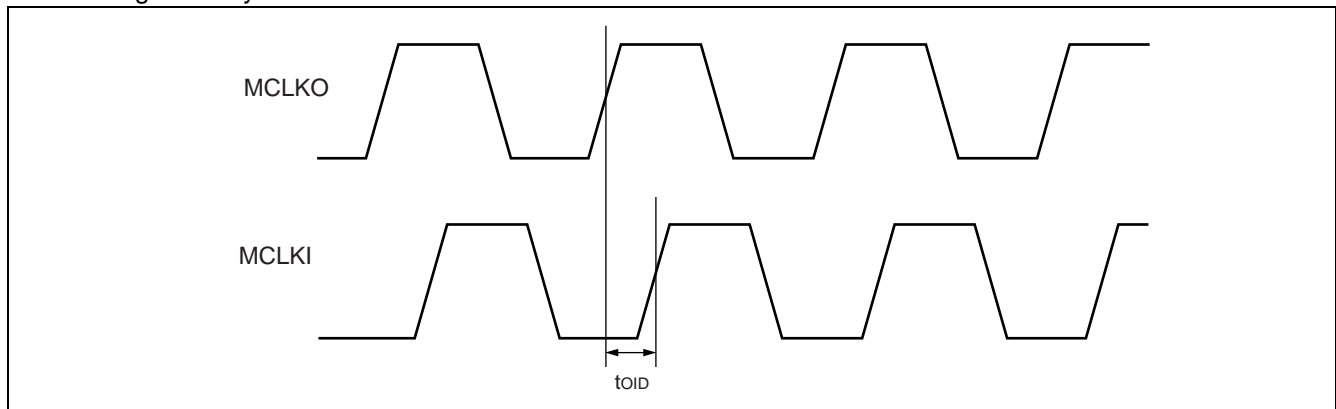
• Clock



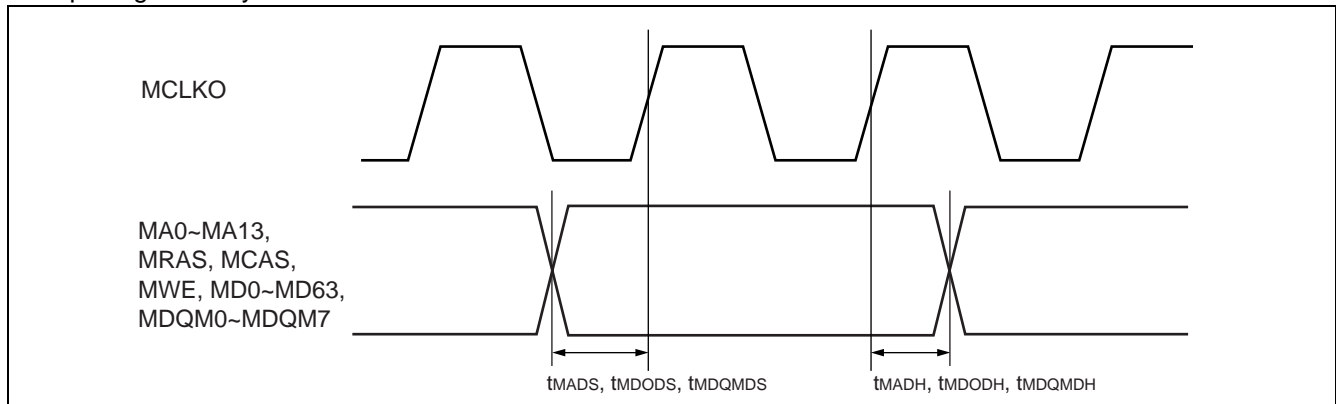
• Input signal setup and hold times



• MCLKI signal delay



• Output signal delay



## (4) PLL Standards

Parameter	Value			Remarks
	Min	Typ	Max	
Input frequency	—	14.31818 MHz	—	
Output frequency	—	—	200.45452 MHz	Multiplied by 14
Duty ratio	101.3 %	—	93.1 %	PLL output clock H/L pulse width ratio
Jitter	180 ps	—	– 150 ps	Cycle difference between two consecutive cycles

## ■ ORDERING INFORMATION

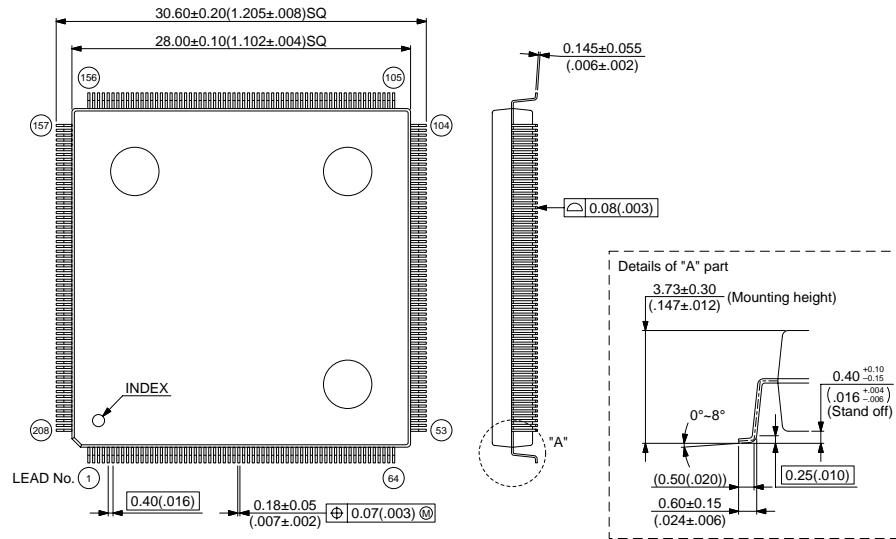
Part Number	Package	Remarks
MB86292PFFS-G-BND	256-pin plastic QFP (FPT-256P-M09)	

# MB86292

## ■ PACKAGE DIMENSION

256-pin plastic QFP  
(FPT-256P-M09)

\*Pins width and pins thickness include plating thickness.



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Dimensions in mm (inches)



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