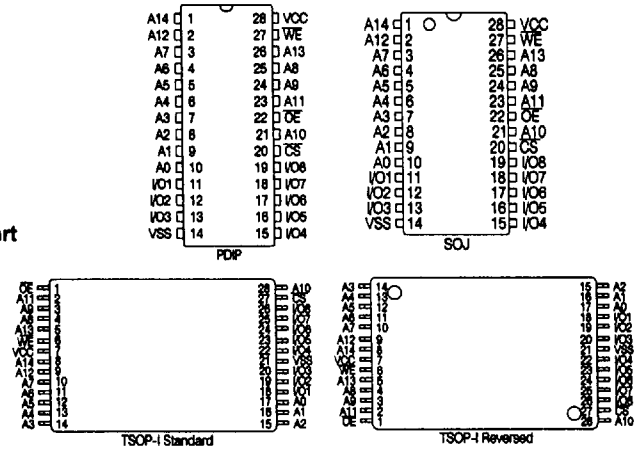
DESCRIPTION

The HY638256 is a high-speed 32,768 x 8-bits CMOS static RAM fabricated using Hyundai's high performance twin tub CMOS process technology. This high reliability process coupled with high-speed circuit design techniques, yields maximum access time of 15ns. The HY638256 has a data retention mode that guarantees data to remain valid at a minimum power supply voltage of 2.0 volt. It is suitable for use in high-density high-speed system applications.

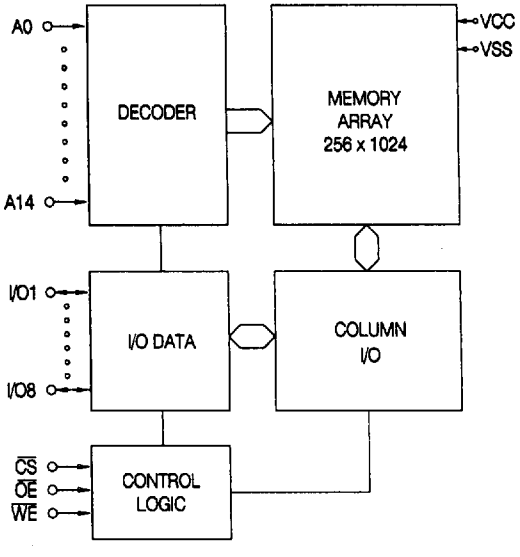
FEATURES

- **High speed - 15/17/20/25ns (max.)**
- **Low power consumption**
  - **Operating 15ns : 100mA (max.)**
    17ns : 100mA (max.)
    20ns : 90mA (max.)
    25ns : 90mA (max.)
  - **Standby (TTL) : 30mA (max.)**
    (CMOS) : 2mA (max.)
    : 100μA (max.) - L-part
- **Single 5V±10% power supply**
- **Battery backup (L-part)**
  - **2.0V (min.) data retention**
- **Fully static operation**
  - **No clock or refresh requird**
- **TTL compatible inputs and outputs**
- **Tri-state output**
- **Standard pin configuration**
  - **28 pin 300 mil PDIP**
  - **28 pin 300 mil SOJ**
  - **28 pin 8 x 13.4 mm TSOP-I**

PIN CONNECTION



BLOCK DIAGRAM



PIN DESCRIPTION

Pin Name	Pin Function
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
A0-A14	Address Inputs
I/O1-I/O8	Data Input/Output
Vcc	Power(+5V)
Vss	Ground

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}, V_{IN}, V_{OUT}	Power Supply, Input/Output Voltage	-0.5 to 7.0	V
T_A	Operating Temperature	0 to 70	°C
T_{BIAS}	Temperature Under Bias	-10 to 125	°C
T_{STG}	Storage Temperature	-65 to 150	°C
P_D	Power Dissipation	1.0	W
I_{OUT}	Data Output Current	50	mA
T_{SOLDER}	Lead Soldering Temperature & Time	260 • 10	°C • sec

Note:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliablity.

RECOMMENDED DC OPERATING CONDITIONS

(T_A= 0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	-	V_{CC} + 0.5	V
V_{IL}	Input Low Voltage	-0.5[1]	-	0.8	V

Note:
1. V_{IL} = -3.0V for pulse width less than 10ns

TRUTH TABLE

MODE	I/O OPERATION	$\overline{CS}$	$\overline{WE}$	$\overline{OE}$
Standby	High-Z	H	X	X
Output Disabled	High-Z	L	H	H
Read	Data out	L	H	L
Write	Data in	L	L	X

Note:
1. X= Don't Care
   H= V_{IH}
   L= V_{IL}

DC CHARACTERISTICS

(T_A = 0°C to 70°C, V_{CC} = 5V± 10%, unless otherwise specified.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Leakage Current	$V_{SS} \le V_{IN} \le V_{CC}$		-2	-	2	μA
I_{LO}	Output Leakage Current	$V_{SS} \le V_{OUT} \le V_{CC}$ $\overline{CS}$ = V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$ = V_{IL}		-2	-	2	μA
I_{CC1}	Average Operating Current	$\overline{CS}$ = V_{IL}, I_{VO} = 0mA Min. Duty Cycle = 100%	15ns	-	-	100	mA
			17ns	-	-	100	mA
			20ns	-	-	90	mA
			25ns	-	-	90	mA
I_{SB}	TTL Standby Current (TTL Inputs)	$\overline{CS}$=V_{IH}, V_{IN}=V_{IH} or V_{IL}, Min. Cycle		-	-	30	mA
I_{SB1}	CMOS Standby Current(CMOS Inputs)	$\overline{CS} \ge V_{CC}$ -0.2V, $V_{IN} \ge$ V_{CC}-0.2V or $V_{IN} \le$ 0.2V		-	-	2	mA
			L	-	20	100	μA
V_{OL}	Output Low Voltage	I_{OL}= 8.0mA		-	-	0.4	V
V_{OH}	Output High Voltage	I_{OH}= - 4.0mA		2.4	-	-	V

Note:
1. Typical values are at Vcc=5.0V, T=25°C

AC CHARACTERISTICS

(TA=0°C to 70°C, Vcc=5V ±10%, unless otherwise noted.)

#	SYMBOL	PARAMETER	15		17		20		25		UNIT
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
	READ CYCLE										
1	tRC	Read Cycle Time	15	-	17	-	20	-	25	-	ns
2	tAA	Address Access Time	-	15	-	17	-	20	-	25	ns
3	tACS	Chip Select Access Time	-	15	-	17	-	20	-	25	ns
4	tOE	Output Enable to Output Valid	-	8	-	9	-	10	-	12	ns
5	tCLZ	Chip Select to Low -Z Output	3	-	3	-	3	-	3	-	ns
6	tOLZ	Output Enable to Low-Z Output	3	-	3	-	3	-	3	-	ns
7	tCHZ	Chip Disable to High -Z Output	0	8	0	8	0	10	0	10	ns
8	tOHZ	Output Disable to High -Z Output	0	8	0	8	0	8	0	8	ns
9	tOH	Output Hold from Address Change	3	-	3	-	3	-	3	-	ns
	WRITE CYCLE										
10	tWC	Write Cycle Time	15	-	17	-	20	-	25	-	ns
11	tCW	Chip Select to End of Write	12	-	13	-	13	-	15	-	ns
12	tAW	Address Valid to End of Write	12	-	13	-	13	-	15	-	ns
13	tAS	Address Set-up Time	0	-	0	-	0	-	0	-	ns
14	tWP	Write Pulse Width	12	-	13	-	13	-	15	-	ns
15	tWR	Write Recovery Time	0	-	0	-	0	-	0	-	ns
16	tWHZ	Write to High-Z Output	0	7	0	8	0	9	0	10	ns
17	tDW	Data to Write Time Overlap	8	-	8	-	9	-	10	-	ns
18	tDH	Data Hold from Write Time	0	-	0	-	0	-	0	-	ns
19	tOW	Output Active from End of Write	3	-	3	-	3	-	3	-	ns

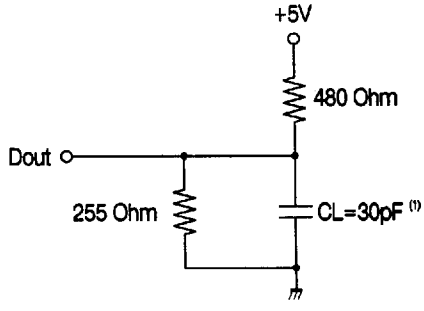
AC TEST CONDITIONS

(T_A=0°C to 70°C, V_{CC}=5V ±10%, unless otherwise specified.)

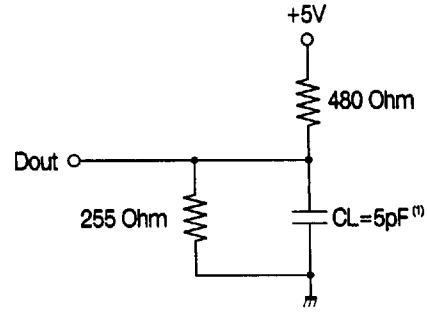
PARAMETER	VALUE
Input Pulse Level	0V to 3V
Input Rise and Fall Time	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	See below

AC TEST LOADS

Output Load (A)



Output Load (B)
(for t_{CHZ},t_{CLZ},t_{OHZ},t_{WHZ} & t_{OW})



Note:
1. Including jig and scope capacitance.

CAPACITANCE

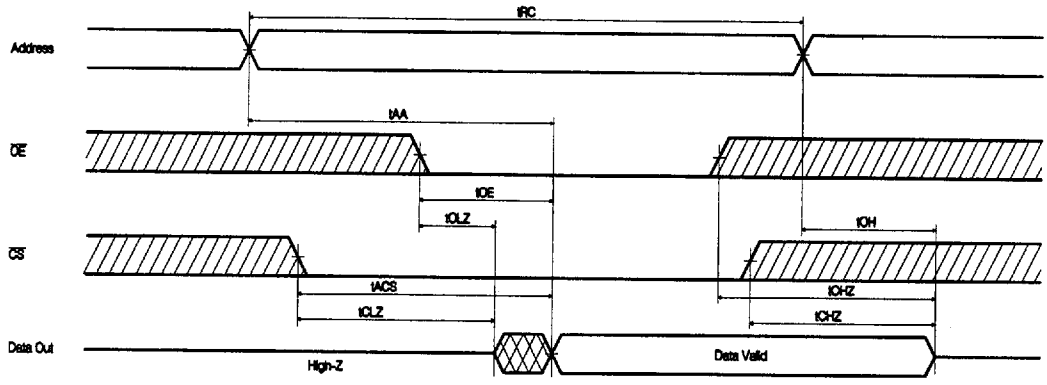
(T_A=25°C, f= 1MHz)

SYMBOL	PARAMETER	CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=0V	6	pF
$C_{I/O}$	Input/Output Capacitance	$V_{I/O}$=0V	8	pF

Note:
1. This parameter is sampled and not 100% tested.

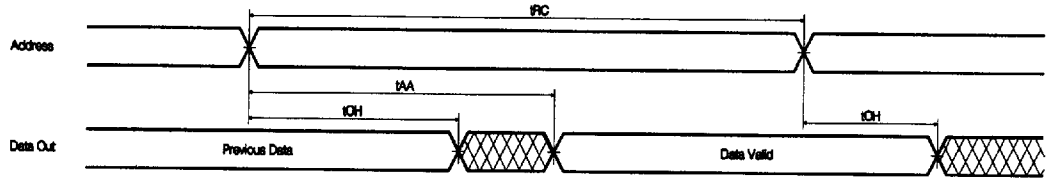
TIMING DIAGRAM

READ CYCLE1



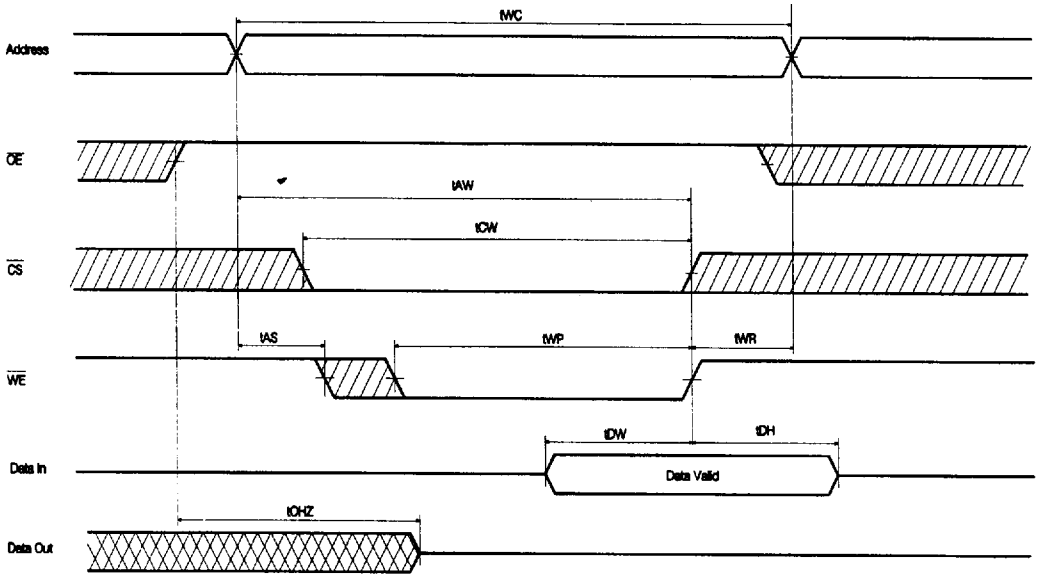
Note (READ CYCLE):
1. t_{CHZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, t_{CHZ} max. is less than t_{CLZ} min. both for a given device and from device to device.
3. $\overline{WE}$ is high for read cycle.

READ CYCLE2

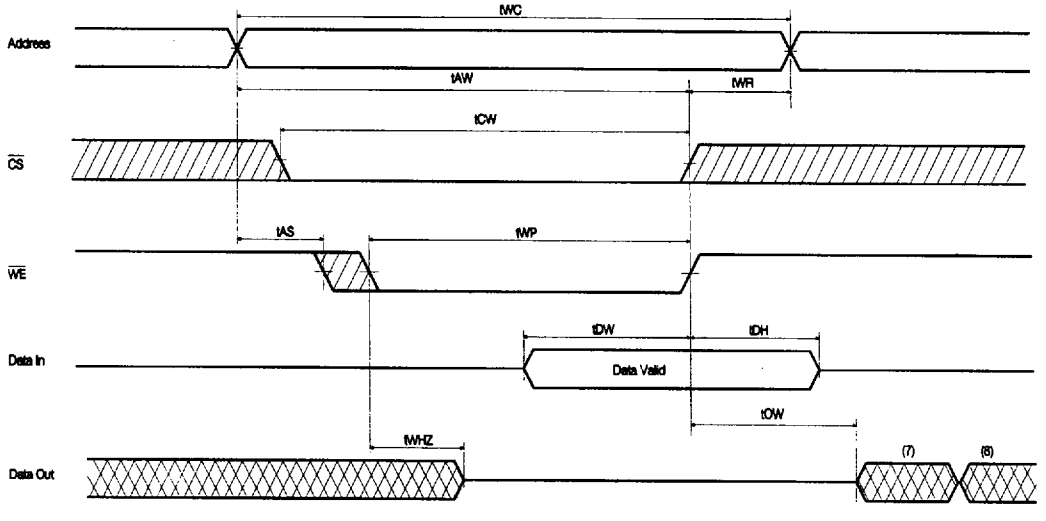


Note (READ CYCLE):
1. $\overline{WE}$ is high for read cycle.
2. Device is continuously selected $\overline{CS}$=V_{IL}.
3. $\overline{OE}$=V_{IL}.

WRITE CYCLE 1($\overline{OE}$ Clocked)



WRITE CYCLE 2($\overline{OE}$ Low Fixed)



Note (WRITE CYCLE):

1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS}$ going low, and $\overline{WE}$ going low: A write ends at the earlist transition among $\overline{CS}$ going high and $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the later of $\overline{CS}$ going low to end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as $\overline{CS}$ or $\overline{WE}$ going high.
5. If $\overline{OE}$ and $\overline{WE}$ are in the read mode during this period, the I/O pins are in the output low-Z state, inputs of opposite phase of the output must not be applied because bus contention can occur.
6. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high impedance state.
7. D_{OUT} is the same phase of lastest written data in this write cycle.
8. D_{OUT} is the read data of the new address.

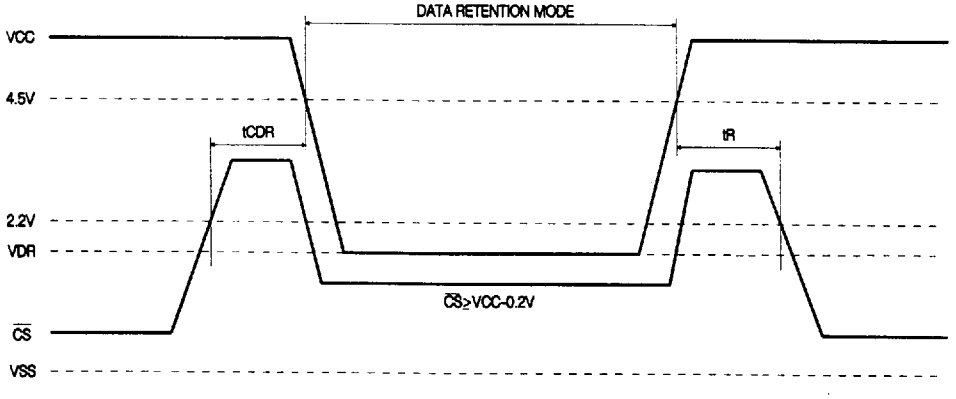
DATA RETENTION CHARACTERISTICS (L Version)

(T_A=0°C to 70°C)

SYMBOL	PARAMETER	TEST CONDITION	POWER	MIN.	TYP.	MAX.	UNIT
V_{DR}	Vcc for Data Retention	$\overline{CS} \geq V_{CC}-0.2V$ $V_{SS} \leq V_{IN} \leq V_{CC}$		2.0	–	–	V
I_{CCDR}	Data Retention Current	Vcc=3.0V $\overline{CS} \geq V_{CC}-0.2V$ $V_{SS} \leq V_{IN} \leq V_{CC}$	L	–	2	50	μA
t_{CDR}	Chip Disable to Data Retention Time	See Data Retention Timing Diagram		0	–	–	ns
t_R	Operating Recovery Time			t_{RC}(2)	–	–	ns

Notes:
1. Typical values are at the condition of T_A=25°C.
2. t_{RC} is read cycle time.

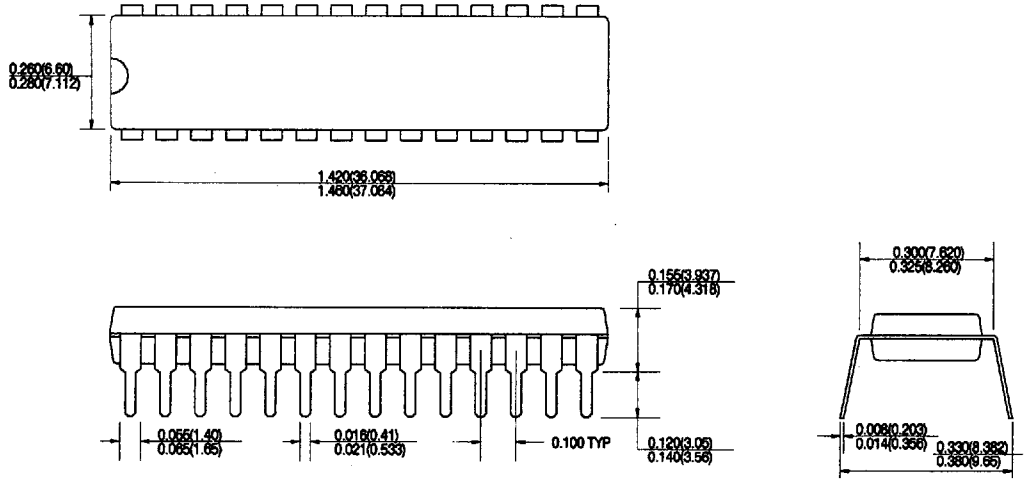
DATA RETENTION TIMING DIAGRAM



PACKAGE INFORMATION

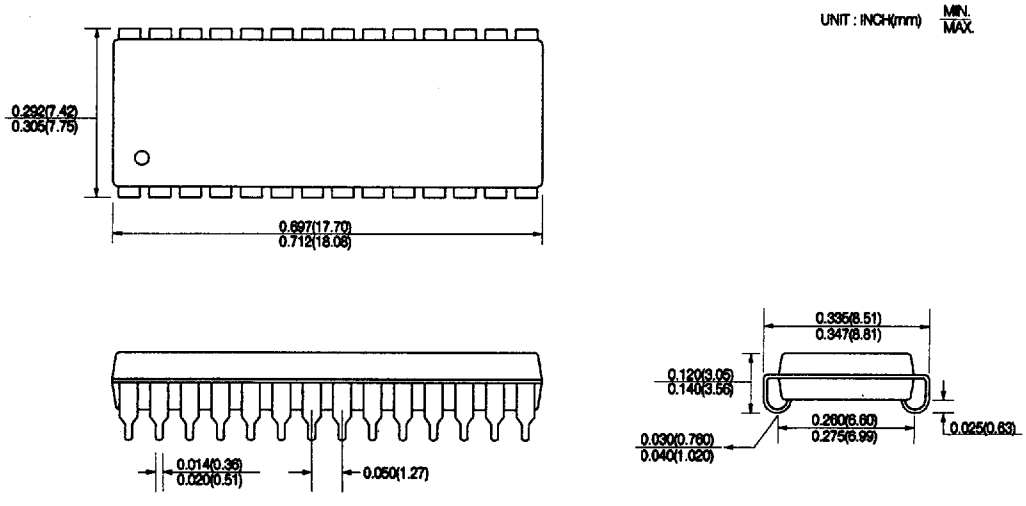
300mil 28 pin Plastic Dual In-line Package (P)

UNIT : INCH(mm) MIN. MAX.

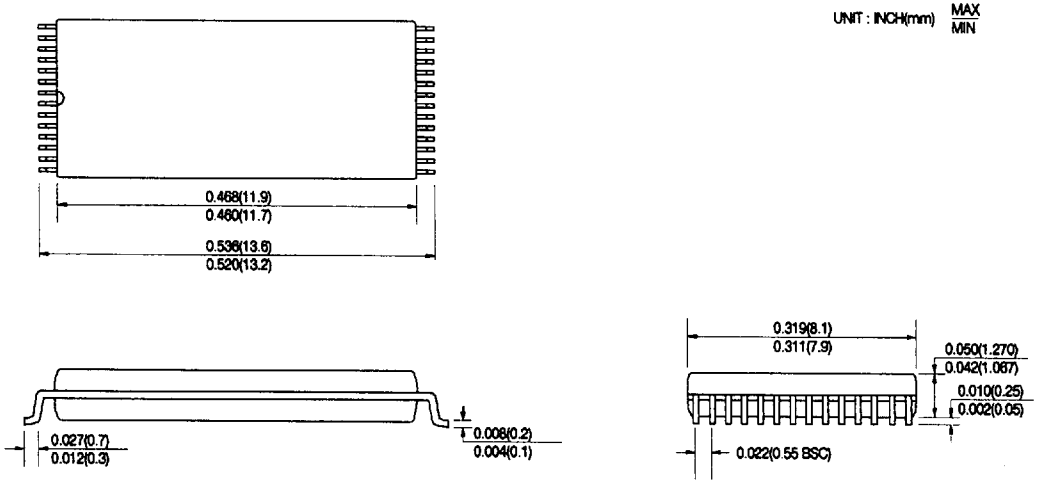


300mil 28 pin Small Outline J-Form Package (J)

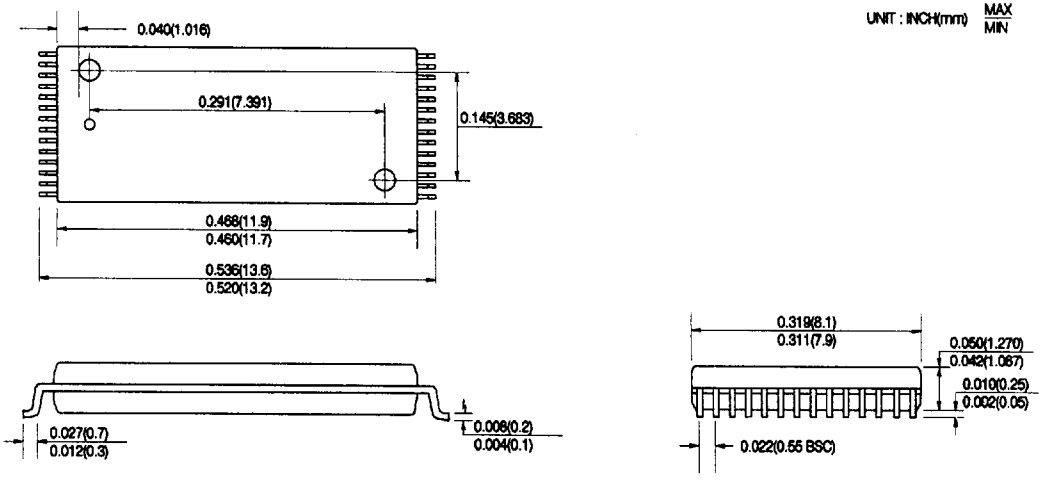
UNIT : INCH(mm) MIN. MAX.



28 pin Plastic Thin Small Out Line Package (T1)



28 pin Thin Small Out Line Package (R1)



ORDERING INFORMATION

PART NO.	SPEED	POWER	PACKAGE
HY638256P	15/17/20/25		PDIP
HY638256LP	15/17/20/25	L-part	PDIP
HY638256J	15/17/20/25		SOJ
HY638256LJ	15/17/20/25	L-part	SOJ
HY638256T1	15/17/20/25		TSOP-I
HY638256LT1	15/17/20/25	L-part	TSOP-I
HY638256R1	15/17/20/25		TSOP-I (R)
HY638256LR1	15/17/20/25	L-part	TSOP-I (R)