

SERIES EL552 ECL (100K COMPATIBLE) DUAL LOGIC DELAY MODULES

- 12 Pin DIP Package • Two Independent Equal Delays
- ECL 100K Input and Output Levels • 70 ECL DC Fan-out Capacity

Specifications:

- Supply Voltage : $-4.5\text{VDC} \pm 5\%$ to Vee
- Logic 1 Input Voltage : -1.165v Min
- Logic 0 Input Voltage : -1.475v Max
- Logic 1 Output Voltage : -1.025v Min
- Logic 0 Output Voltage : -1.63v Max
- Output Rise Time (2) : 2NSEC Typ.
- Operating Temperature : -30°C to $+85^\circ\text{C}$
- Storage Temperature : -55°C to $+125^\circ\text{C}$

Test Conditions:

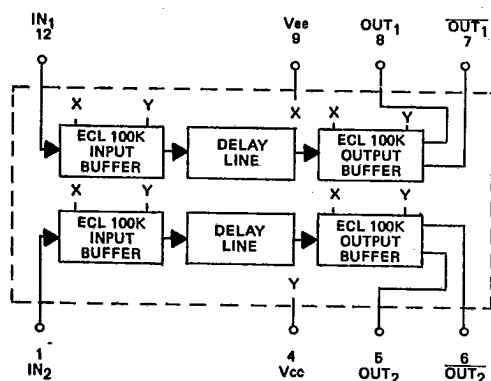
- Input Pulse-Width : Min 150% of Total Delay
- Input Pulse Rise Time : 2NSEC Max
- Input Pulse Voltage : 0.8v P.P (-0.9vH to -1.7vL)
- Vee Supply Voltage : -4.5VDC

Electrical Specifications at 25°C

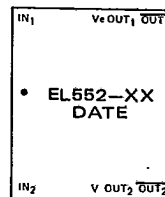
Part Number	Delay Per Line (NS) (1)	Part Number	Delay Per Line (NS) (1)
EL552-2	$2 \pm .2$	EL552-11	11 ± 1
EL552-2.5	$2.5 \pm .2$	EL552-12	12 ± 1
EL552-3	$3 \pm .2$	EL552-12.5	12.5 ± 1
EL552-3.5	$3.5 \pm .3$	EL552-13	13 ± 1
EL552-4	$4 \pm .4$	EL552-14	14 ± 1
EL552-4.5	$4.5 \pm .4$	EL552-15	15 ± 1
EL552-5	$5 \pm .5$	EL552-16	16 ± 1
EL552-5.5	$5.5 \pm .5$	EL552-17	17 ± 1
EL552-6	$6 \pm .6$	EL552-18	18 ± 1
EL552-7	$7 \pm .7$	EL552-19	19 ± 1
EL552-8	$8 \pm .8$	EL552-20	20 ± 1
EL552-9	$9 \pm .9$	EL552-25	25 ± 1.5
EL552-10	10 ± 1	EL552-30	30 ± 1.5

Note: (1) Measured at -1.3v level leading edge.

(2) Output Rise Time measured from 20% to 80% Pulse Amplitude.



SCHEMATIC



Solderable Leads (8)
Dia. .020
.51

