PA01 • PA73

POWER OPERATIONAL AMPLIFIERS

T-79-23

FEATURES

- LOW COST, ECONOMY MODEL—PA01
- SECOND SOURCEABLE—PA73
- HIGH OUTPUT CURRENT—Up to ±5A PEAK
- EXCELLENT LINEARITY—PA01
- HIGH SUPPLY VOLTAGE—Up to ±34V
- ISOLATED CASE—300V

APPLICATIONS

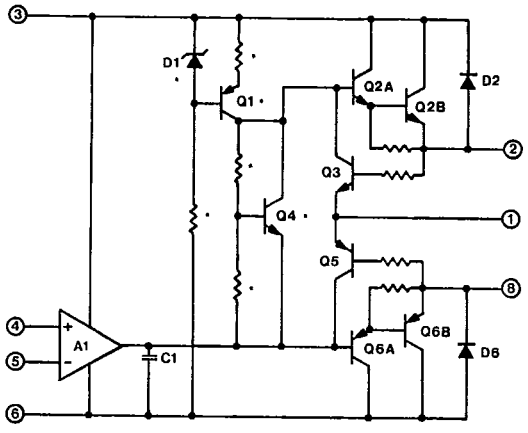
- MOTOR, VALVE AND ACTUATOR CONTROL
- MAGNETIC DEFLECTION CIRCUITS UP TO 4A
- POWER TRANSDUCERS UP TO 20KHz
- TEMPERATURE CONTROL UP TO 180W
- PROGRAMMABLE POWER SUPPLIES UP TO 56V
- AUDIO AMPLIFIERS UP TO 50W RMS

DESCRIPTION

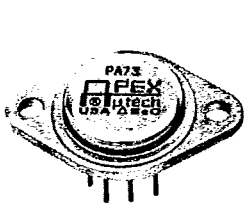
The PA01 and PA73 are high voltage, high output current operational amplifiers designed to drive resistive, inductive and capacitive loads. All three have a complementary darlington emitter follower output stage protected against transient inductive kickback or back EMF. For optimum linearity, the PA01 has a class A/B output stage. The PA73 has a simple class C output stage (see Note 1) to reduce cost for motor control and other applications where crossover distortion is not critical and to provide interchangeability with type 3573 amplifiers. The safe operating area (SOA) can be observed for all operating conditions by selection of user programmable current limit resistors. These amplifiers are internally compensated for all gain settings. For continuous operation under load, a heatsink of proper rating is recommended.

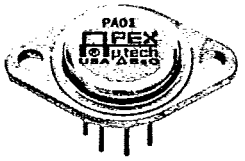
This hybrid integrated circuit utilizes thick film (cermet) resistors, ceramic capacitors and semiconductor chips to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 8 pin TO-3 package is hermetically sealed and electrically isolated. The use of compressible isolation washers may void the warranty.

EQUIVALENT SCHEMATIC

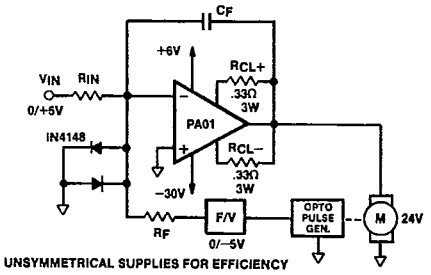


NOTE 1 *Indicates not used in PA73. Open base of Q2A connected to output of A1.





TYPICAL APPLICATION

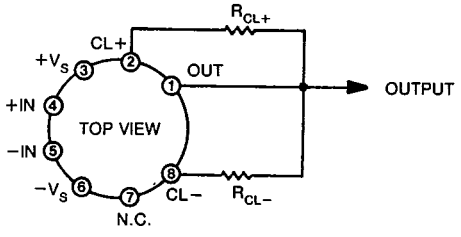


UNSYMMETRICAL SUPPLIES FOR EFFICIENCY

Unidirectional Optical Speed Control

The pulse output of a non-contact optical sensor drives a voltage to frequency converter which generates feedback for the op amp. With the loop closed in this manner the op amp corrects for any variations in the speed due to changing load. Because of operation in only one direction, an unsymmetrical supply is used to maximize efficiency of both power op amp and power supply. High speed diodes at the input protect the op amp from commutator noise which may be generated by the motor.

EXTERNAL CONNECTIONS



PA01, 73 ABSOLUTE MAXIMUM RATINGS

T-79-23

	PA01	PA73
SUPPLY VOLTAGE, +Vs to -Vs	60V	68V
OUTPUT CURRENT, within SOA	5A	5A
POWER DISSIPATION, internal[1]	67W	67W
INPUT VOLTAGE, differential	±Vs -3V	±Vs -3V
INPUT VOLTAGE, common-mode	±Vs	±Vs
TEMPERATURE, junction[1]	200°C	200°C
TEMPERATURE, pin solder -10s	300°C	300°C
TEMPERATURE RANGE, storage	-65 to +150°C	-65 to +150°C
OPERATING TEMPERATURE RANGE, case	-25 to +85°C	-25 to +85°C

SPECIFICATIONS

		PA01			PA73			
PARAMETER	**TEST CONDITIONS[2]**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT								
OFFSET VOLTAGE, initial	$T_C = 25°C$		±5	±12		*	±10	mV
OFFSET VOLTAGE, vs. temperature	Full temperature range		±10	±65		*	*	µV/°C
OFFSET VOLTAGE, vs. supply	$T_C = 25°C$		±35			*	±200	µV/V
OFFSET VOLTAGE, vs. power	$T_C = 25°C$		±20			*		µV/W
BIAS CURRENT, initial	$T_C = 25°C$		±15	±50		*	±40	nA
BIAS CURRENT, vs. temperature	Full temperature range		±.05	±.4		*	*	nA/°C
BIAS CURRENT, vs. supply	$T_C = 25°C$		±.02			*		nA/V
OFFSET CURRENT, initial	$T_C = 25°C$		±5	±15		*	±10	nA
OFFSET CURRENT, vs. temperature	Full temperature range		±.01			*		nA/°C
INPUT IMPEDANCE, common-mode	$T_C = 25°C$		200			*		MΩ
INPUT IMPEDANCE, differential	$T_C = 25°C$		10			*		MΩ
INPUT CAPACITANCE	$T_C = 25°C$		3			*		pF
COMMON-MODE VOLTAGE RANGE[3]	Full temperature range	$\pm V_S - 6$	$\pm V_S - 3$		*	*		V
COMMON-MODE REJECTION, dc[3]	$T_C = 25°C$, $V_{CM} = V_S - 6V$	70	110		*	*		db
GAIN								
OPEN LOOP GAIN at 10Hz	Full temp. range, full load	91	113		*	*		db
GAIN BANDWIDTH PRODUCT at 1MHz	$T_C = 25°C$, full load		1			*		MHz
POWER BANDWIDTH	$T_C = 25°C$, $I_O = 4A$, $V_O = 40V_{PP}$	15	23		*	*		kHz
PHASE MARGIN	Full temperature range		45			*		°
OUTPUT								
VOLTAGE SWING[3]	$T_C = 25°C$, $I_O = 5A$	$\pm V_S - 10$	$\pm V_S - 5$		$\pm V_S - 8$	*		V
VOLTAGE SWING[3]	Full temp. range, $I_O = 2A$	$\pm V_S - 6$	$\pm V_S - 5$		*	*		V
VOLTAGE SWING[3]	Full temp. range, $I_O = 46mA$	$\pm V_S - 5$			*			V
CURRENT, peak	$T_C = 25°C$	±5			*			A
SETTLING TIME to .1%	$T_C = 25°C$, 2V step		2			*		µs
SLEW RATE	$T_C = 25°C$, $R_L = 2.5Ω$	±1.0	2.6		*	*		V/µs
CAPACITIVE LOAD, unity gain	Full temperature range			3.3			*	nF
CAPACITIVE LOAD, gain>4	Full temperature range			SOA			*	
POWER SUPPLY								
VOLTAGE	Full temperature range	±10	±28	±28	*	*	±30	V
CURRENT, quiescent	$T_C = 25°C$		20	50		20/2.6	30/5	mA
THERMAL								
RESISTANCE, ac[4] junction to case	F>60Hz		1.9	2.1		*	*	°C/W
RESISTANCE, dc junction to case	F<60Hz		2.4	2.6		*	*	°C/W
RESISTANCE, junction to air			30			*	*	°C/W
TEMPERATURE RANGE, case	Meet full range specification	−25	25	+85	*	*	*	°C

NOTES: * The specification of PA73 is identical to the specification for PA01 in applicable column to the left.

1. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.
2. The power supply voltage specified under the TYP rating applies unless otherwise noted as a test condition.
3. +Vs and -Vs denote the positive and negative supply rail respectively. Total Vs is measured from +Vs to -Vs.
4. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.

CAUTION: The internal substrate contains berylia (BeO). Do not break the seal. If broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

PA01, 73 TYPICAL PERFORMANCE GRAPHS

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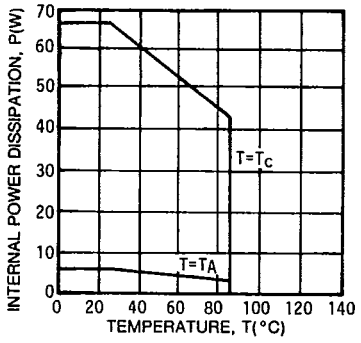
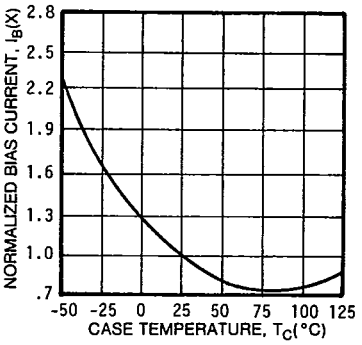
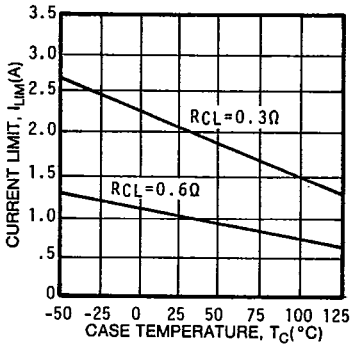
POWER DERATING



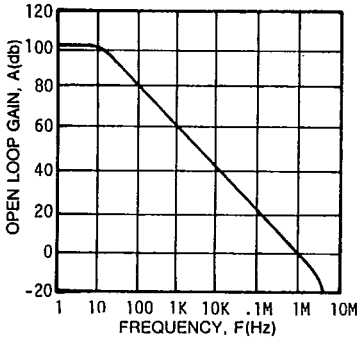
BIAS CURRENT



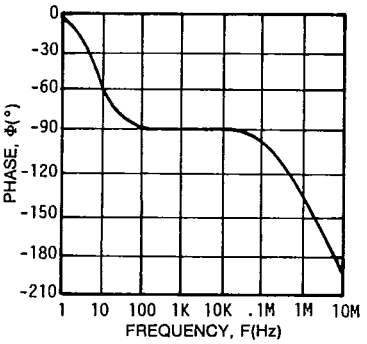
CURRENT LIMIT



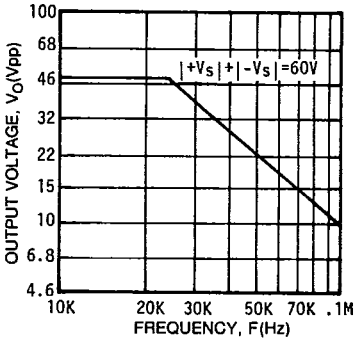
SMALL SIGNAL RESPONSE



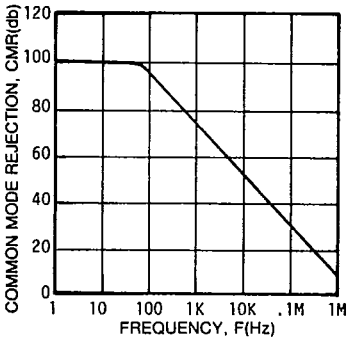
PHASE RESPONSE



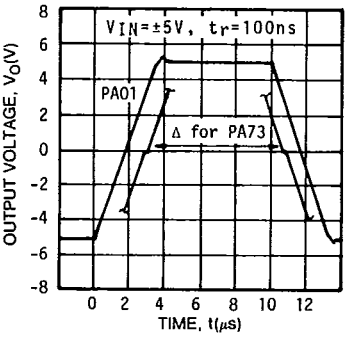
POWER RESPONSE



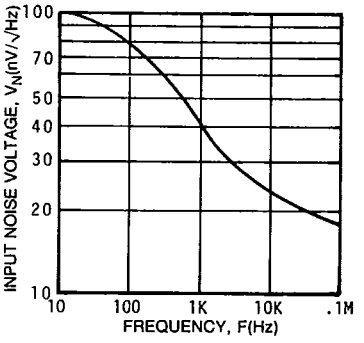
COMMON MODE REJECTION



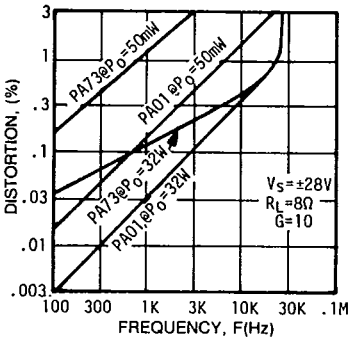
PULSE RESPONSE



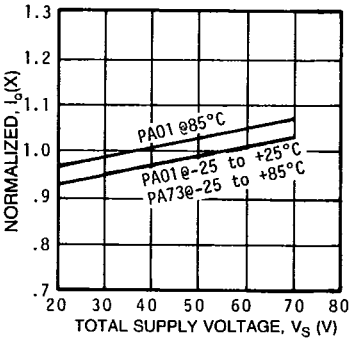
INPUT NOISE



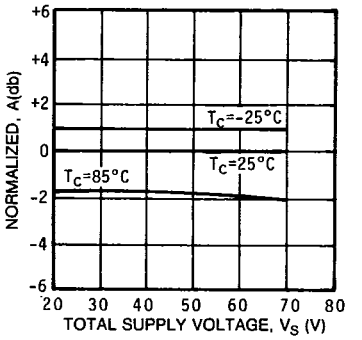
HARMONIC DISTORTION



QUIESCENT CURRENT



OPEN LOOP GAIN



PA01, 73 OPERATING CONSIDERATIONS

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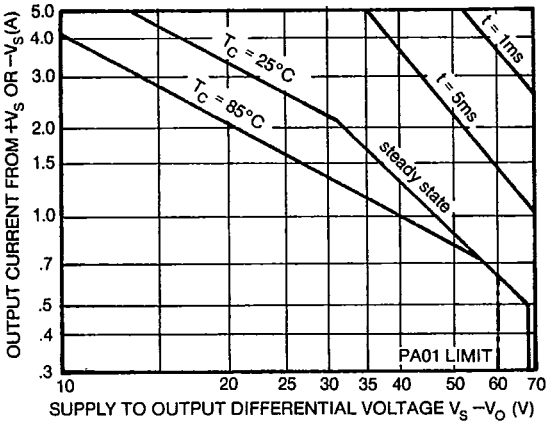
GENERAL

Please read the "General Operating Considerations" section, which covers stability, supplies, heatsinking, mounting, current limit, SOA interpretation, and specification interpretation. Additional information can be found in the applications notes. For information on the package outline, heatsinks, and mounting hardware, consult the "Accessory and Package Mechanical Data" section of the handbook.

SAFE OPERATING AREA

The output stage of most power amplifiers has 3 distinct limitations:

1. The current handling capability of the transistor geometry and the wire bonds.
2. The secondary breakdown effect which occurs whenever the simultaneous collector current and collector-emitter voltage exceeds specified limits.
3. The junction temperature of the output transistors.



The SOA curves combine the effect of these limits. For a given application, the direction and magnitude of the output current should be calculated or measures and checked against the SOA curves. This is simple for resistive loads but more complex for reactive and EMF generating loads. However, the following guidelines may save extensive analytical efforts:

1. Capacitive and dynamic* inductive loads up to the following maximums are safe with the current limits set as specified:

	CAPACITIVE LOAD		INDUCTIVE LOAD	
$\pm V_S$	I_{LIM} = 2A	I_{LIM} = 5A	I_{LIM} = 2A	I_{LIM} = 5A
30V	1,200µF	500µF	250mH	24mH
25V	4,000µF	1,600µF	400mH	38mH
20V	20,000µF	5,000µF	1,500mH	75mH
15V	**	25,000µF	**	100mH

* If the inductive load is driven near steady state conditions, allowing the output voltage to drop more than 8V below the supply rail with I_{LIM} = 5A or 20V below the supply rail with I_{LIM} = 2A while the amplifier is current limiting, the inductor should be capacitively coupled or the current limit must be lowered to meet SOA criteria.

** Secondary breakdown effect imposes no limitation but thermal limitations must still be observed.

2. EMF generating or reactive load and short circuits to the supply rails or shorts to common are safe if the current limits are set as follows at T_C = 85°C:

$\pm V_S$	SHORT TO $\pm V_S$, C,L or EMF LOAD	SHORT TO COMMON
34V	.50A	1.2A
30V	.60A	1.3A
25V	.75A	1.6A
20V	1.0A	2.1A
15V	1.3A	2.8A

These simplified limits may be exceeded with further analysis using the operating conditions for a specific application.

3. The output stage is protected against transient flyback. However, for protection against sustained, high energy flyback, external fast-recovery diodes should be used.

CURRENT LIMIT

Proper operation requires the use of two current limit resistors, connected as shown in the external connection diagram. The minimum value for Rcl is 0.12 ohm, however for optimum reliability it should be set as high as possible. Refer to the "General Operating Considerations" section of the handbook for current limit adjust details.

APEX μtech

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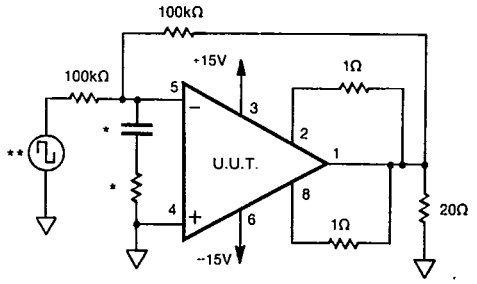
PA73M

TABLE 4 — GROUP A INSPECTION

SG	PARAMETER	SYMBOL	TEMP	PWR	TEST CONDITIONS	MIN	MAX	UNITS
1	Quiescent Current	I_Q	25°C	±28V	V_{IN} = 0, G = 100		5	mA
1	Input Offset Voltage	V_{OS}	25°C	±28V	V_{IN} = 0, G = 100		±10	mV
1	Input Offset Voltage	V_{OS}	25°C	±10V	V_{IN} = 0, G = 100		±17.2	mV
1	Input Offset Voltage	V_{OS}	25°C	±30V	V_{IN} = 0, G = 100		±10.8	mV
1	Input Bias Current, +IN	$+I_B$	25°C	±28V	V_{IN} = 0, G = 100		±40	nA
1	Input Bias Current, −IN	$-I_B$	25°C	±28V	V_{IN} = 0, G = 100		±40	nA
1	Input Offset Current	I_{OS}	25°C	±28V	V_{IN} = 0, G = 100		±10	nA
3	Quiescent Current	I_Q	−55°C	±28V	V_{IN} = 0, G = 100		5	mA
3	Input Offset Voltage	V_{OS}	−55°C	±28V	V_{IN} = 0, G = 100		±15.2	mV
3	Input Offset Voltage	V_{OS}	−55°C	±10V	V_{IN} = 0, G = 100		±22.4	mV
3	Input Offset Voltage	V_{OS}	−55°C	±30V	V_{IN} = 0, G = 100		±16	mV
3	Input Bias Current, +IN	$+I_B$	−55°C	±28V	V_{IN} = 0, G = 100		±72	nA
3	Input Bias Current, −IN	$-I_B$	−55°C	±28V	V_{IN} = 0, G = 100		±72	nA
3	Input Offset Current	I_{OS}	−55°C	±28V	V_{IN} = 0, G = 100		±26	nA
2	Quiescent Current	I_Q	125°C	±28V	V_{IN} = 0, G = 100		7	mA
2	Input Offset Voltage	V_{OS}	125°C	±28V	V_{IN} = 0, G = 100		±16.5	mV
2	Input Offset Voltage	V_{OS}	125°C	±10V	V_{IN} = 0, G = 100		±23.7	mV
2	Input Offset Voltage	V_{OS}	125°C	±30V	V_{IN} = 0, G = 100		±17.3	mV
2	Input Bias Current, +IN	$+I_B$	125°C	±28V	V_{IN} = 0, G = 100		±80	nA
2	Input Bias Current, −IN	$-I_B$	125°C	±28V	V_{IN} = 0, G = 100		±80	nA
2	Input Offset Current	I_{OS}	125°C	±28V	V_{IN} = 0, G = 100		±30	nA
4	Output Voltage, I_O = 5A	V_O	25°C	±18.3V	R_L = 2.07Ω	10.3		V
4	Output Voltage, I_O = 50mA	V_O	25°C	±30V	R_L = 500Ω	25		V
4	Output Voltage, I_O = 2A	V_O	25°C	±30V	R_L = 12Ω	24		V
4	Current Limits	I_{CL}	25°C	±16V	R_L = 2.07Ω, R_{CL} = .2Ω	2.6	3.9	A
4	Stability/Noise	E_N	25°C	±28V	R_L = 500Ω, G = 1, C_L = 10nF		1	mV
4	Slew Rate	SR	25°C	±28V	R_L = 500Ω	1	10	V/μs
4	Open Loop Gain	A_{OL}	25°C	±28V	R_L = 500Ω, f = 10Hz	91		db
4	Common-mode Rejection	CMR	25°C	±15V	R_L = 500Ω, f = DC, V_{CM} = ±9V	70		db
6	Output Voltage, I_O = 5A	V_O	−55°C	±18.3V	R_L = 2.07Ω	10.3		V
6	Output Voltage, I_O = 50mA	V_O	−55°C	±30V	R_L = 500Ω	25		V
6	Output Voltage, I_O = 2A	V_O	−55°C	±30V	R_L = 12Ω	24		V
6	Stability/Noise	E_N	−55°C	±28V	R_L = 500Ω, G = 1, C_L = 10nF		1	mV
6	Slew Rate	SR	−55°C	±28V	R_L = 500Ω	1	10	V/μs
6	Open Loop Gain	A_{OL}	−55°C	±28V	R_L = 500Ω, f = 10Hz	91		db
6	Common-mode Rejection	CMR	−55°C	±15V	R_L = 500Ω, f = DC, V_{CM} = ±9V	70		db
5	Output Voltage, I_O = 3A	V_O	125°C	±11.3V	R_L = 2.07Ω	6.3		V
5	Output Voltage, I_O = 50mA	V_O	125°C	±30V	R_L = 500Ω	25		V
5	Output Voltage, I_O = 2A	V_O	125°C	±30V	R_L = 12Ω	24		V
5	Stability/Noise	E_N	125°C	±28V	R_L = 500Ω, G = 1, C_L = 10nF		1	mV
5	Slew Rate	SR	125°C	±28V	R_L = 500Ω	1	10	V/μs
5	Open Loop Gain	A_{OL}	125°C	±28V	R_L = 500Ω, f = 10Hz	91		db
5	Common-mode Rejection	CMR	125°C	±15V	R_L = 500Ω, f = DC, V_{CM} = ±9V	70		db

BURN IN CIRCUIT:



*These components are used to stabilize device due to poor high frequency characteristics of burn in board.

**Input signals are calculated to result in internal power dissipation of approximately 2.1W at case temperature = 125°C.

APEX µtech

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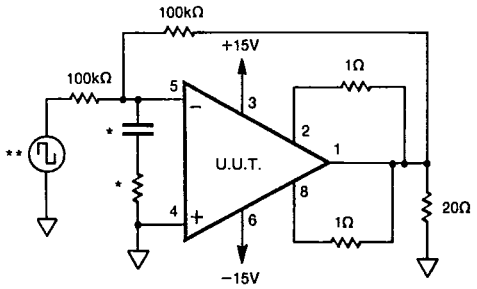
PA73Q

100% TEST TABLE

SG	PARAMETER	SYMBOL	TEMP	PWR	TEST CONDITIONS	MIN	MAX	UNITS
1	Quiescent Current	I_Q	25°C	±28V	V_{IN} = 0, G = 100		5	mA
1	Input Offset Voltage	V_{OS}	25°C	±28V	V_{IN} = 0, G = 100		±10	mV
1	Input Offset Voltage	V_{OS}	25°C	±10V	V_{IN} = 0, G = 100		±17.2	mV
1	Input Offset Voltage	V_{OS}	25°C	±30V	V_{IN} = 0, G = 100		±10.8	mV
1	Input Bias Current, +IN	$+I_B$	25°C	±28V	V_{IN} = 0, G = 100		±40	nA
1	Input Bias Current, −IN	$-I_B$	25°C	±28V	V_{IN} = 0, G = 100		±40	nA
1	Input Offset Current	I_{OS}	25°C	±28V	V_{IN} = 0, G = 100		±10	nA
3	Quiescent Current	I_Q	−25°C	±28V	V_{IN} = 0, G = 100		5	mA
3	Input Offset Voltage	V_{OS}	−25°C	±28V	V_{IN} = 0, G = 100		±13.2	mV
3	Input Offset Voltage	V_{OS}	−25°C	±10V	V_{IN} = 0, G = 100		±20.4	mV
3	Input Offset Voltage	V_{OS}	−25°C	±30V	V_{IN} = 0, G = 100		±14	mV
3	Input Bias Current, +IN	$+I_B$	−25°C	±28V	V_{IN} = 0, G = 100		±60	nA
3	Input Bias Current, −IN	$-I_B$	−25°C	±28V	V_{IN} = 0, G = 100		±60	nA
3	Input Offset Current	I_{OS}	−25°C	±28V	V_{IN} = 0, G = 100		±20	nA
2	Quiescent Current	I_Q	85°C	±28V	V_{IN} = 0, G = 100		7	mA
2	Input Offset Voltage	V_{OS}	85°C	±28V	V_{IN} = 0, G = 100		±13.9	mV
2	Input Offset Voltage	V_{OS}	85°C	±10V	V_{IN} = 0, G = 100		±21.1	mV
2	Input Offset Voltage	V_{OS}	85°C	±30V	V_{IN} = 0, G = 100		±14.7	mV
2	Input Bias Current, +IN	$+I_B$	85°C	±28V	V_{IN} = 0, G = 100		±64	nA
2	Input Bias Current, −IN	$-I_B$	85°C	±28V	V_{IN} = 0, G = 100		±64	nA
2	Input Offset Current	I_{OS}	85°C	±28V	V_{IN} = 0, G = 100		±22	nA
4	Output Voltage, I_O = 5A	V_O	25°C	±18.3V	R_L = 2.07Ω	10.3		V
4	Output Voltage, I_O = 50mA	V_O	25°C	±30V	R_L = 500Ω	25		V
4	Output Voltage, I_O = 2A	V_O	25°C	±30V	R_L = 12Ω	24		V
4	Current Limits	I_{CL}	25°C	±16V	R_L = 2.07Ω, R_{CL} = .2Ω	2.6	3.9	A
4	Stability/Noise	E_N	25°C	±28V	R_L = 500Ω, G = 1, C_L = 10nF		1	mV
4	Slew Rate	SR	25°C	±28V	R_L = 500Ω	1	10	V/µs
4	Open Loop Gain	A_{OL}	25°C	±28V	R_L = 500Ω, f = 10Hz	91		db
4	Common-mode Rejection	CMR	25°C	±15V	R_L = 500Ω, f = DC, V_{CM} = ±9V	70		db
6	Output Voltage, I_O = 5A	V_O	−25°C	±18.3V	R_L = 2.07Ω	10.3		V
6	Output Voltage, I_O = 50mA	V_O	−25°C	±30V	R_L = 500Ω	25		V
6	Output Voltage, I_O = 2A	V_O	−25°C	±30V	R_L = 12Ω	24		V
6	Stability/Noise	E_N	−25°C	±28V	R_L = 500Ω, G = 1, C_L = 10nF		1	mV
6	Slew Rate	SR	−25°C	±28V	R_L = 500Ω	1	10	V/µs
6	Open Loop Gain	A_{OL}	−25°C	±28V	R_L = 500Ω, f = 10Hz	91		db
6	Common-mode Rejection	CMR	−25°C	±15V	R_L = 500Ω, f = DC, V_{CM} = ±9V	70		db
5	Output Voltage, I_O = 3A	V_O	85°C	±11.3V	R_L = 2.07Ω	6.3		V
5	Output Voltage, I_O = 50mA	V_O	85°C	±30V	R_L = 500Ω	25		V
5	Output Voltage, I_O = 2A	V_O	85°C	±30V	R_L = 12Ω	24		V
5	Stability/Noise	E_N	85°C	±28V	R_L = 500Ω, G = 1, C_L = 10nF		1	mV
5	Slew Rate	SR	85°C	±28V	R_L = 500Ω	1	10	V/µs
5	Open Loop Gain	A_{OL}	85°C	±28V	R_L = 500Ω, f = 10Hz	91		db
5	Common-mode Rejection	CMR	85°C	±15V	R_L = 500Ω, f = DC, V_{CM} = ±9V	70		db

BURN IN CIRCUIT:



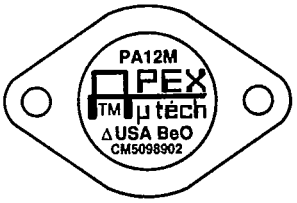
*These components are used to stabilize device due to poor high frequency characteristics of burn in board.

**Input signals are calculated to result in internal power dissipation of approximately 2.1W at case temperature = 125°C.

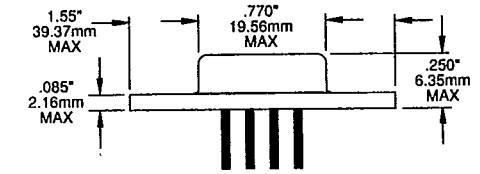
PACKAGE OUTLINE DIMENSIONS

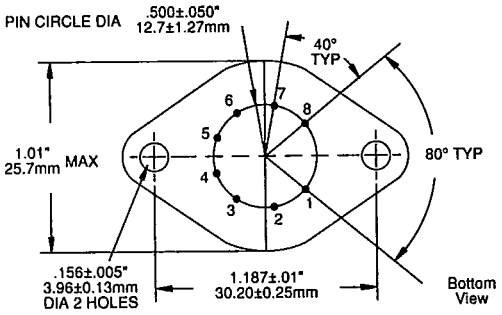
T-90-20

STANDARD 8 PIN TO-3



NOTE: ESD triangle (Δ) on top of package denotes pin 1 location.

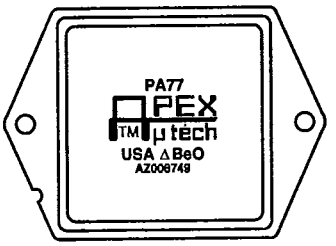




PIN DIAMETER:	.967/1.07mm or .038/.042"
PIN LENGTH:	11.4/12.7mm or .450/.500"
PIN MATERIAL, STD:	Nickel plated alloy 52, solderable
PIN MATERIAL, MIL:	Gold plated alloy 52, solderable
PACKAGE:	Hermetic, nickel plated steel
WEIGHT:	15 grams or .53 ounces
ISOLATION:	500VDC any pin to case
SOCKETS:	APEX PN: MS03
CAGE JACKS:	APEX PN: MS02 (Set of 8)
HEATSINKS:	APEX PN: HS01 thru HS05

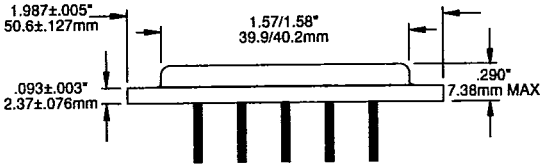
CAUTION
Recommended mounting torque is 4 – 7 in•lbs (.45 – .79 N•m)

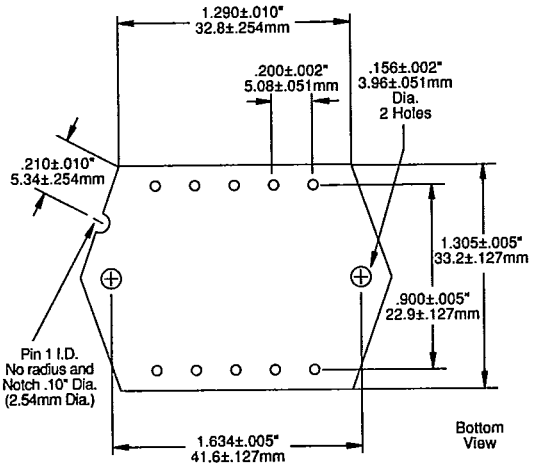
POWER PD10



NOTE: Notch on package base denotes pin 1 location.

PD10/60S





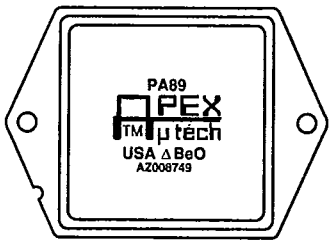
PIN DIAMETER:	1.47/1.58mm or .058/.062"
PIN LENGTH:	11.4/12.7mm or .450/.500"
PIN MATERIAL, STD:	Nickel plated steel
PACKAGE:	Hermetic, nickel plated steel
WEIGHT:	36 grams or 1.27 ounces
ISOLATION:	500VDC any pin to case
CAGE JACKS:	MS04 (Set of 12)

CAUTION
Recommended mounting torque is 8 – 10 in•lbs (.90 – 1.13 N•m)

PACKAGE OUTLINE DIMENSIONS

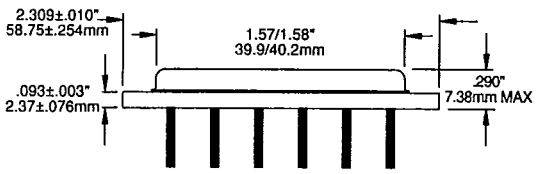
T-90-20

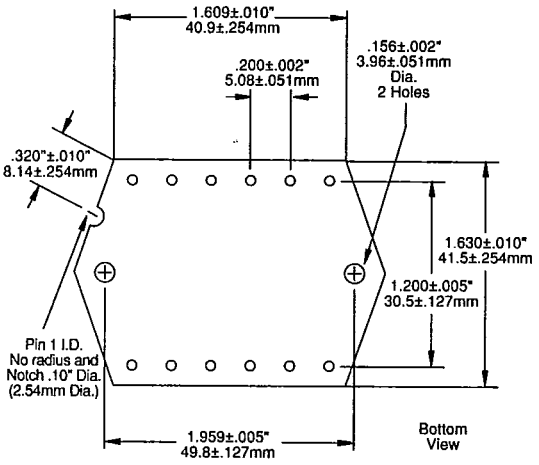
HIGH VOLTAGE PD12



NOTE: Notch on package base denotes pin 1 location.

PD12/25S

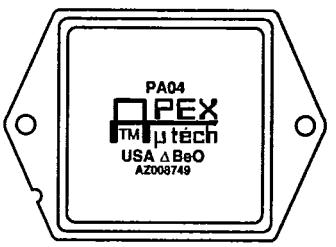




PIN DIAMETER:	.585/.687mm or .023/.027"
PIN LENGTH:	11.4/12.7mm or .450/.500"
PIN MATERIAL, STD:	Nickel plated steel
PACKAGE:	Hermetic, nickel plated steel
WEIGHT:	53 grams or 1.87 ounces
ISOLATION:	1200VDC any pin to case

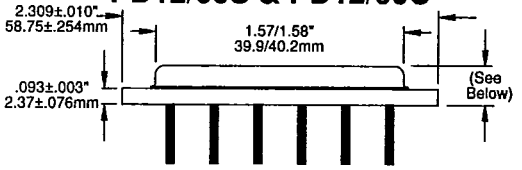
CAUTION
Recommended mounting torque is 8 – 10 in•lbs (.90 – 1.13 N•m)

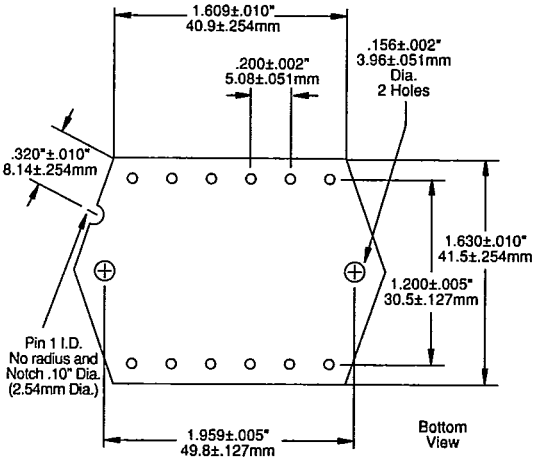
HIGH POWER PD12



NOTE: Notch on package base denotes pin 1 location.

PD12/60S & PD12/60C





PIN DIAMETER:		1.47/1.58mm or .058/.062"
PIN LENGTH:		11.4/12.7mm or .450/.500"
PIN MATERIAL, STD:		Nickel plated steel
ISOLATION:	PD12/60S:	500VDC any pin to case
	PD12/60C:	300VDC any pin to case
HEIGHT:	PD12/60S:	7.38mm or .290" MAX
	PD12/60C:	8.90mm or .350" MAX
PACKAGE:	PD12/60S:	Hermetic, nickel plated steel
	PD12/60C:	Base: Nickel plated copper
	PD12/60C:	Cap: Hermetic, nickel plated steel
WEIGHT:	PD12/60S:	53 grams or 1.87 ounces
	PD12/60C:	58 grams or 2.05 ounces
CAGE JACKS:	Apex PN:	MS04 (Set of 12)
HEAT SINKS:	Apex PN:	HS06
MATING SOCKET:	Apex PN:	MS05

CAUTION Recommended mounting torque is 8–10 in•lbs (.90–1.13 N•m)