100-Pin TQFP
Commercial Temp
Industrial Temp

512K x 18, 256K x 36 8Mb Sync Burst SRAMs

11 ns–18 ns
3.3 V V_{DD}
3.3 V and 2.5 V I/O

Features

- Flow Through mode operation
- 3.3 V +10%/–5% core power supply
- 2.5 V or 3.3 V I/O supply
- LBO pin for Linear or Interleaved Burst mode
- Internal input resistors on mode pins allow floating mode pins
- Default to Interleaved Pipeline mode
- Byte Write (BW) and/or Global Write (GW) operation
- Common data inputs and data outputs
- Clock Control, registered, address, data, and control
- Internal self-timed write cycle
- Automatic power-down for portable applications
- 100-lead TQFP package

		-11	-11.5	-12	-14	-18
Flow Through 2-1-1-1	t_{KQ}	11 ns	11.5 ns	12 ns	14 ns	18 ns
	tCycle	15 ns	15 ns	15 ns	15 ns	20 ns
	I_{DD}	180 mA	180 mA	180 mA	175 mA	165 mA

Functional Description

Applications

The GS880F18/36T is a 9,437,184-bit high performance synchronous SRAM with a 2-bit burst address counter. Although of a type originally developed for Level 2 Cache applications supporting high performance CPUs, the device now finds application in synchronous SRAM applications, ranging from DSP main store to networking chip set support.

Controls

Addresses, data I/Os, chip enables (E1, E2, E3), address burst control inputs (ADSP, ADSC, ADV) and write control inputs (Bx, BW, GW) are synchronous and are controlled by a positive-edge-triggered clock input (CK). Output enable (G) and power down control (ZZ) are asynchronous inputs. Burst cycles can be initiated with either ADSP or ADSC inputs. In Burst mode, subsequent burst addresses are generated internally and are controlled by ADV. The burst address counter may be configured to count in either linear or interleave order with the Linear Burst Order (LBO) input. The Burst function need not be used. New addresses can be loaded on every cycle with no degradation of chip performance.

Designing For Compatibility

The JEDEC Standard for Burst RAMS calls for a FT mode pin option (pin 14 on TQFP). Board sites for flow through Burst RAMS should be designed with V_{SS} connected to the FT pin location to ensure the broadest access to multiple vendor sources. Boards designed with FT pin pads tied low may be stuffed with GSI's Pipeline/Flow Through-configurable Burst RAMS or any vendor's Flow Through or configurable Burst SRAM. Bumps designed with the FT pin location tied high or floating must employ a non-configurable Flow Through Burst RAM, like this RAM, to achieve flow through functionality.

Byte Write and Global Write

Byte write operation is performed by using Byte Write enable (BW) input combined with one or more individual byte write signals (Bx). In addition, Global Write (GW) is available for writing all bytes at one time, regardless of the byte write control inputs.

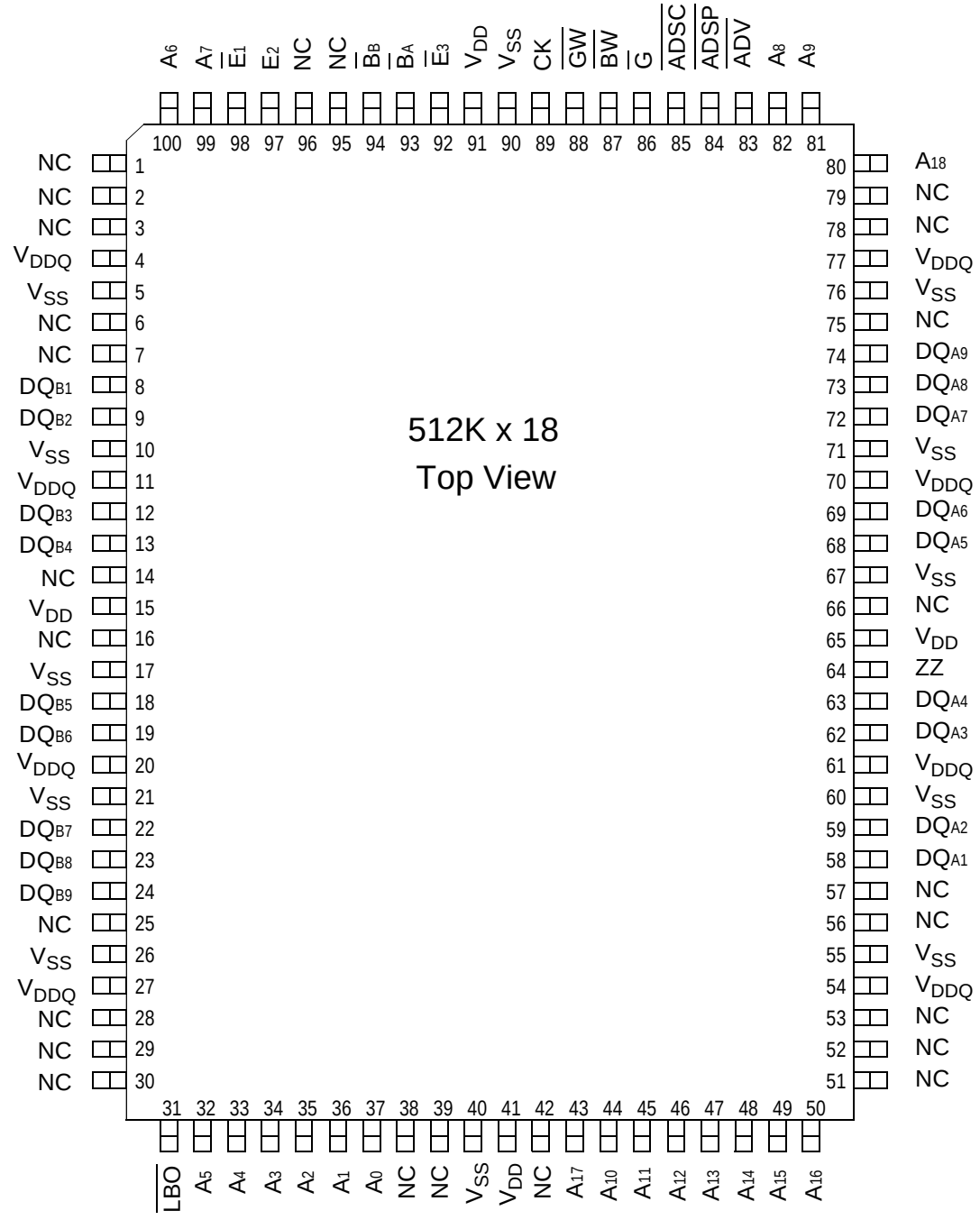
Sleep Mode

Low power (Sleep mode) is attained through the assertion (high) of the ZZ signal, or by stopping the clock (CK). Memory data is retained during Sleep mode.

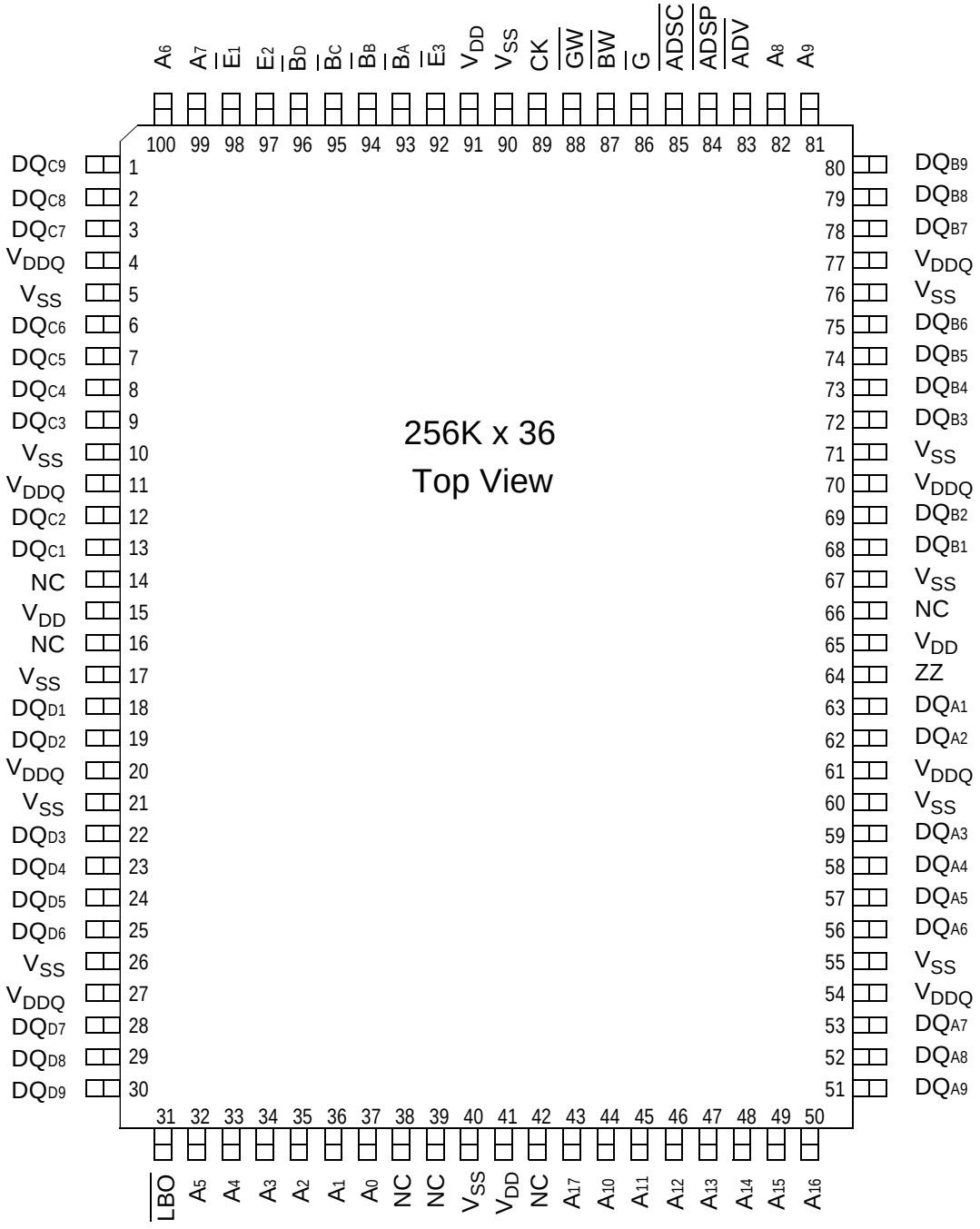
Core and Interface Voltages

The GS880F18/36T operates on a 3.3 V power supply, and all inputs/outputs are 3.3 V- and 2.5 V-compatible. Separate output power (V_{DDQ}) pins are used to decouple output noise from the internal circuit.

GS880F18 100-Pin TQFP Pinout



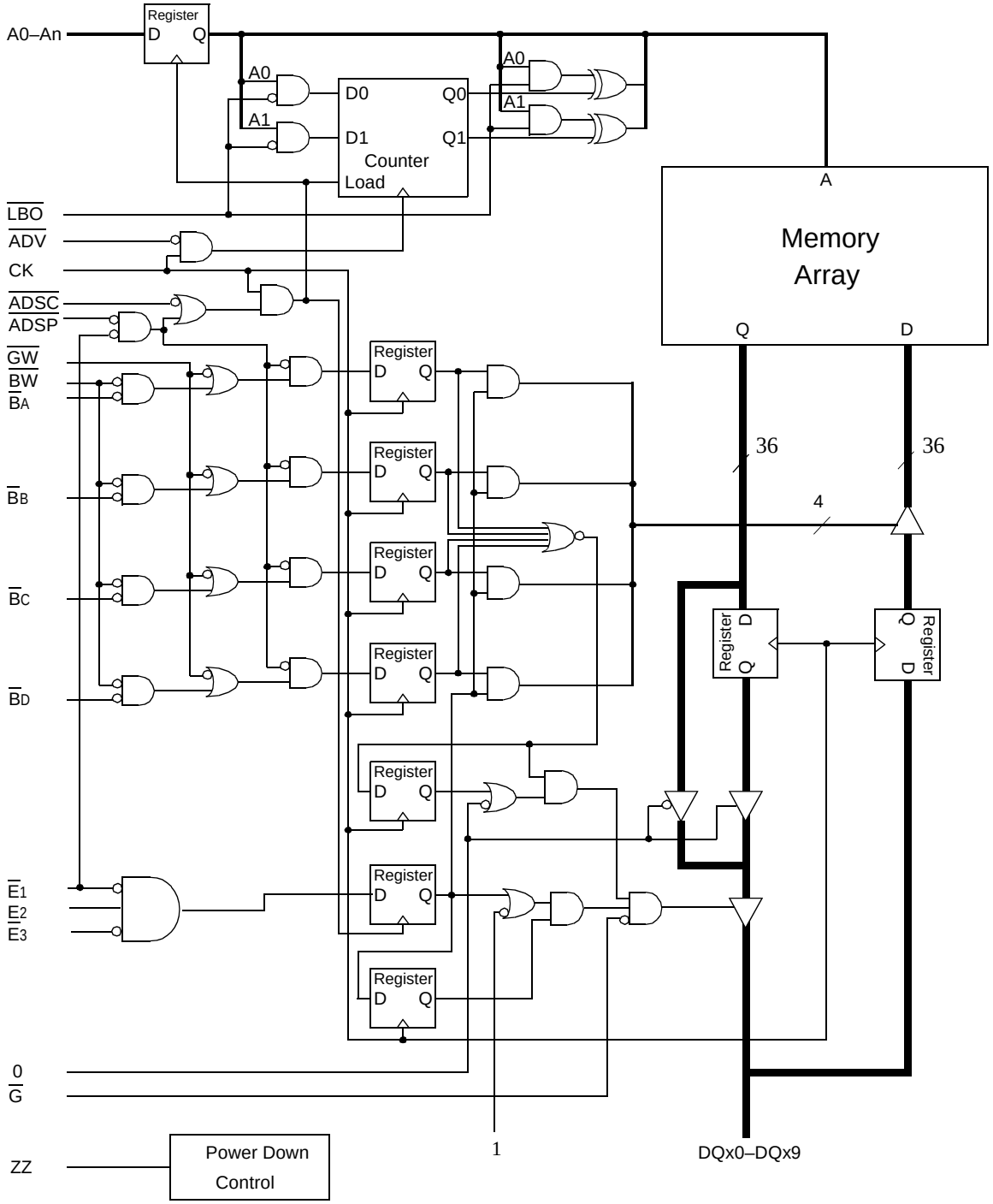
GS880F36 100-Pin TQFP Pinout



TQFP Pin Description

Pin Location	Symbol	Type	Description
37, 36	A_0, A_1	I	Address field LSBs and Address Counter preset Inputs
35, 34, 33, 32, 100, 99, 82, 81, 44, 45, 46, 47, 48, 49, 50, 43	A_2–A_{17}	I	Address Inputs
80	A_{18}	I	Address Inputs
63, 62, 59, 58, 57, 56, 53, 52 68, 69, 72, 73, 74, 75, 78, 79 13, 12, 9, 8, 7, 6, 3, 2 18, 19, 22, 23, 24, 25, 28, 29	DQ_{A1}–DQ_{A8} DQ_{B1}–DQ_{B8} DQ_{C1}–DQ_{C8} DQ_{D1}–DQ_{D8}	I/O	Data Input and Output pins (x36 Version)
51, 80, 1, 30	DQ_{A9}, DQ_{B9}, DQ_{C9}, DQ_{D9}	I/O	Data Input and Output pins
58, 59, 62, 63, 68, 69, 72, 73, 74 8, 9, 12, 13, 18, 19, 22, 23, 24	DQ_{A1}–DQ_{A9} DQ_{B1}–DQ_{B9}	I/O	Data Input and Output pins
51, 52, 53, 56, 57 75, 78, 79, 1, 2, 3, 6, 7 25, 28, 29, 30	NC	—	No Connect
87	$\overline{BW}$	I	Byte Write—Writes all enabled bytes; active low
93, 94	$\overline{B}_A$, $\overline{B}_B$	I	Byte Write Enable for DQ_A, DQ_B Data I/Os; active low
95, 96	$\overline{B}_C$, $\overline{B}_D$	I	Byte Write Enable for DQ_C, DQ_D Data I/Os; active low (x36 Version)
95, 96	NC	—	No Connect (x18 Version)
89	CK	I	Clock Input Signal; active high
88	$\overline{GW}$	I	Global Write Enable—Writes all bytes; active low
98, 92	$\overline{E}_1$, $\overline{E}_3$	I	Chip Enable; active low
97	E_2	I	Chip Enable; active high
86	$\overline{G}$	I	Output Enable; active low
83	$\overline{ADV}$	I	Burst address counter advance enable; active low
84, 85	$\overline{ADSP}$, $\overline{ADSC}$	I	Address Strobe (Processor, Cache Controller); active low
64	ZZ	I	Sleep mode control; active high
31	$\overline{LBO}$	I	Linear Burst Order mode; active low
15, 41, 65, 91	V_{DD}	I	Core power supply
5,10,17, 21, 26, 40, 55, 60, 67, 71, 76, 90	V_{SS}	I	I/O and Core Ground
4, 11, 20, 27, 54, 61, 70, 77	V_{DDQ}	I	Output driver power supply
14, 16, 38, 39, 42, 66	NC	—	No Connect.

GS880F18/36 Block Diagram



Note: Only x36 version shown for simplicity.

Mode Pin Functions

Mode Name	Pin Name	State	Function
Burst Order Control	$\overline{LBO}$	L	Linear Burst
		H or NC	Interleaved Burst
Power Down Control	ZZ	L or NC	Active
		H	Standby, $I_{DD} = I_{SB}$

Note:
There is a pull-up device on the $\overline{LBO}$ pin and a pull down device on the ZZ pin, so those input pins can be unconnected and the chip will operate in the default states as specified in the above table.

Burst Counter Sequences

Linear Burst Sequence

	A[1:0]	A[1:0]	A[1:0]	A[1:0]
1st address	00	01	10	11
2nd address	01	10	11	00
3rd address	10	11	00	01
4th address	11	00	01	10

Note: The burst counter wraps to initial state on the 5th clock.

Interleaved Burst Sequence

	A[1:0]	A[1:0]	A[1:0]	A[1:0]
1st address	00	01	10	11
2nd address	01	00	11	10
3rd address	10	11	00	01
4th address	11	10	01	00

Note: The burst counter wraps to initial state on the 5th clock.

BPR 1999.05.18

Byte Write Truth Table

Function	$\overline{GW}$	$\overline{BW}$	$\overline{B}_A$	$\overline{B}_B$	$\overline{B}_C$	$\overline{B}_D$	Notes
Read	H	H	X	X	X	X	1
Read	H	L	H	H	H	H	1
Write byte a	H	L	L	H	H	H	2, 3
Write byte b	H	L	H	L	H	H	2, 3
Write byte c	H	L	H	H	L	H	2, 3, 4
Write byte d	H	L	H	H	H	L	2, 3, 4
Write all bytes	H	L	L	L	L	L	2, 3, 4
Write all bytes	L	X	X	X	X	X	

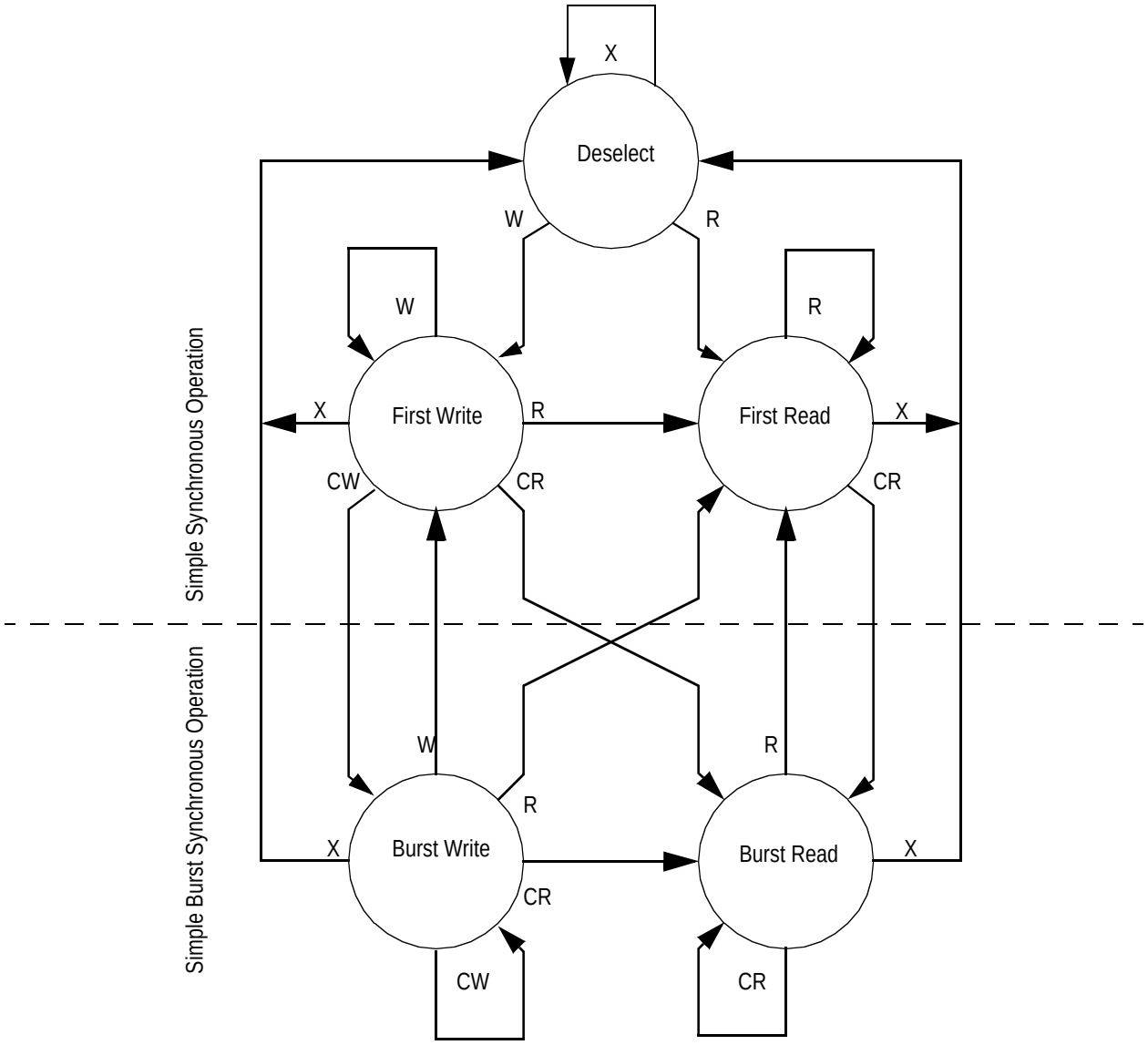
Notes:
1. All byte outputs are active in read cycles regardless of the state of Byte Write Enable inputs.
2. Byte Write Enable inputs $\overline{B}_A$, $\overline{B}_B$, $\overline{B}_C$, and/or $\overline{B}_D$ may be used in any combination with $\overline{BW}$ to write single or multiple bytes.
3. All byte I/Os remain High-Z during all write operations regardless of the state of Byte Write Enable inputs.
4. Bytes "C" and "D" are only available on the and x36 version.

Synchronous Truth Table

Operation	Address Used	State Diagram Key[5]	$\overline{E1}$	E2[2] (x36only)	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	W[3]	DQ[4]
Deselect Cycle, Power Down	**None**	**X**	**H**	**X**	**X**	**L**	**X**	**X**	**High-Z**
Deselect Cycle, Power Down	None	X	L	F	L	X	X	X	High-Z
Deselect Cycle, Power Down	**None**	**X**	**L**	**F**	**H**	**L**	**X**	**X**	**High-Z**
Read Cycle, Begin Burst	External	R	L	T	L	X	X	X	Q
Read Cycle, Begin Burst	**External**	**R**	**L**	**T**	**H**	**L**	**X**	**F**	**Q**
Write Cycle, Begin Burst	**External**	**W**	**L**	**T**	**H**	**L**	**X**	**T**	**D**
Read Cycle, Continue Burst	*Next*	*CR*	*X*	*X*	*H*	*H*	*L*	*F*	*Q*
Read Cycle, Continue Burst	Next	CR	H	X	X	H	L	F	Q
Write Cycle, Continue Burst	*Next*	*CW*	*X*	*X*	*H*	*H*	*L*	*T*	*D*
Write Cycle, Continue Burst	Next	CW	H	X	X	H	L	T	D
Read Cycle, Suspend Burst	Current		X	X	H	H	H	F	Q
Read Cycle, Suspend Burst	Current		H	X	X	H	H	F	Q
Write Cycle, Suspend Burst	Current		X	X	H	H	H	T	D
Write Cycle, Suspend Burst	Current		H	X	X	H	H	T	D

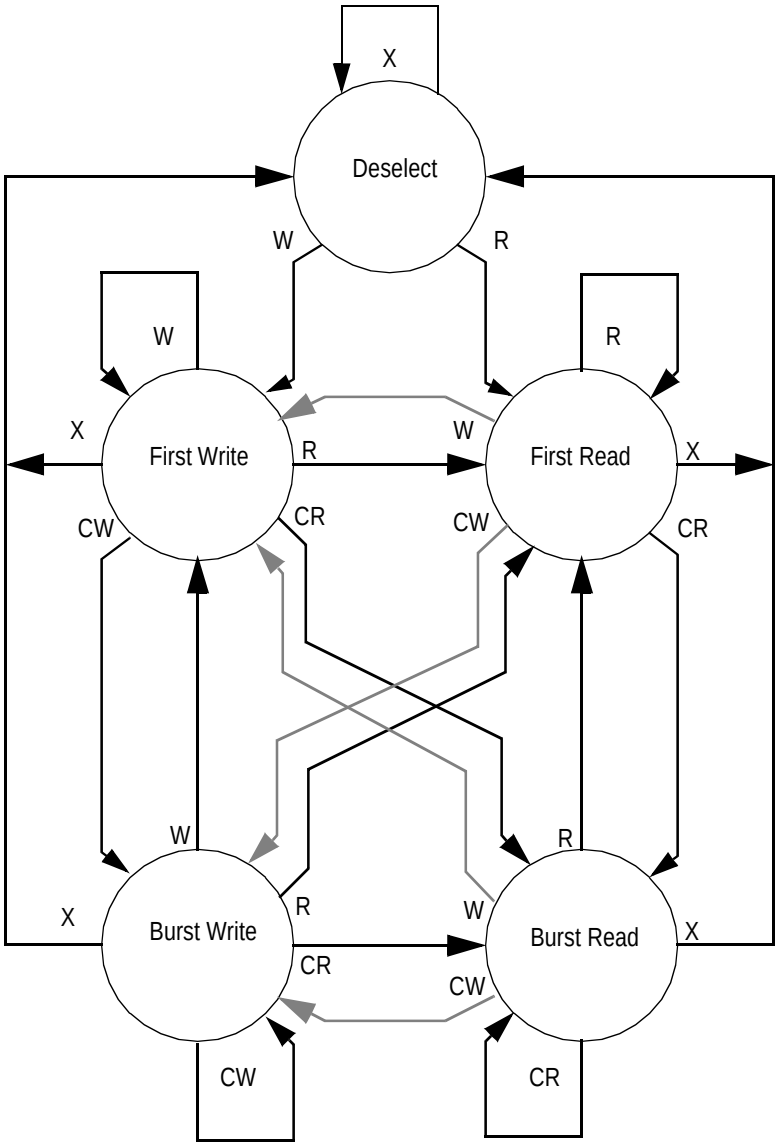
Notes:
1. X = Don't Care, H = High, L = Low.
2. For x36 Version, E = T (True) if E2 = 1 and $\overline{E3}$ = 0; E = F (False) if E2 = 0 or $\overline{E3}$ = 1.
3. $\overline{W}$ = T (True) and F (False) is defined in the Byte Write Truth Table preceding.
4. $\overline{G}$ is an asynchronous input. $\overline{G}$ can be driven high at any time to disable active output drivers. $\overline{G}$ low can only enable active drivers (shown as "Q" in the Truth Table above).
5. All input combinations shown above are tested and supported. Input combinations shown in gray boxes need not be used to accomplish basic synchronous or synchronous burst operations and may be avoided for simplicity.
6. Tying $\overline{ADSP}$ high and $\overline{ADSC}$ low allows simple non-burst synchronous operations. See **BOLD** items above.
7. Tying $\overline{ADSP}$ high and $\overline{ADV}$ low while using $\overline{ADSC}$ to load new addresses allows simple burst operations. See *ITALIC* items above.

Simplified State Diagram



Notes:
1. The diagram shows only supported (tested) synchronous state transitions. The diagram presumes $\overline{G}$ is tied low.
2. The upper portion of the diagram assumes active use of only the Enable ($\overline{E1E2}$) and Write ($\overline{B_A}$, $\overline{B_B}$, $\overline{B_C}$, $\overline{B_D}$, $\overline{BW}$, and $\overline{GW}$) control inputs, and that $\overline{ADSP}$ is tied high and $\overline{ADSC}$ is tied low.
3. The upper and lower portions of the diagram together assume active use of only the Enable, Write, and $\overline{ADSC}$ control inputs, and assumes $\overline{ADSP}$ is tied high and $\overline{ADV}$ is tied low.

Simplified State Diagram with $\overline{G}$



Notes:
1. The diagram shows supported (tested) synchronous state transitions plus supported transitions that depend upon the use of $\overline{G}$.
2. Use of "Dummy Reads" (Read Cycles with $\overline{G}$ High) may be used to make the transition from Read cycles to Write cycles without passing through a Deselect cycle. Dummy Read cycles increment the address counter just like normal Read cycles.
3. Transitions shown in grey tone assume $\overline{G}$ has been pulsed high long enough to turn the RAM's drivers off and for incoming data to meet Data Input Set Up Time.

Absolute Maximum Ratings

(All voltages reference to V_{SS})

Symbol	Description	Value	Unit
V_{DD}	Voltage on V_{DD} Pins	–0.5 to 4.6	V
V_{DDQ}	Voltage in V_{DDQ} Pins	–0.5 to V_{DD}	V
V_{CK}	Voltage on Clock Input Pin	–0.5 to 6	V
$V_{I/O}$	Voltage on I/O Pins	–0.5 to V_{DDQ} +0.5 (≤ 4.6 V max.)	V
V_{IN}	Voltage on Other Input Pins	–0.5 to V_{DD} +0.5 (≤ 4.6 V max.)	V
I_{IN}	Input Current on Any Pin	+/–20	mA
I_{OUT}	Output Current on Any I/O Pin	+/–20	mA
P_D	Package Power Dissipation	1.5	W
T_{STG}	Storage Temperature	–55 to 125	°C
T_{BIAS}	Temperature Under Bias	–55 to 125	°C

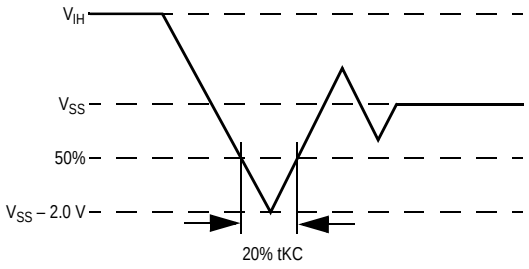
Note:
Permanent damage to the device may occur if the Absolute Maximum Ratings are exceeded. Operation should be restricted to Recommended Operating Conditions. Exposure to conditions exceeding the Absolute Maximum Ratings, for an extended period of time, may affect reliability of this component.

Recommended Operating Conditions

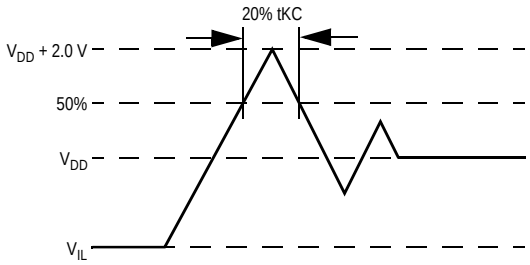
Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Supply Voltage	V_{DD}	3.135	3.3	3.6	V	
I/O Supply Voltage	V_{DDQ}	2.375	2.5	V_{DD}	V	1
Input High Voltage	V_{IH}	1.7	—	V_{DD} +0.3	V	2
Input Low Voltage	V_{IL}	–0.3	—	0.8	V	2
Ambient Temperature (Commercial Range Versions)	T_A	0	25	70	°C	3
Ambient Temperature (Industrial Range Versions)	T_A	–40	25	85	°C	3

Notes:
1. Unless otherwise noted, all performance specifications quoted are evaluated for worst case at both 2.75 V ≤ V_{DDQ} ≤ 2.375 V (i.e., 2.5 V I/O) and 3.6 V ≤ V_{DDQ} ≤ 3.135 V (i.e., 3.3 V I/O), and quoted at whichever condition is worst case.
2. This device features input buffers compatible with both 3.3 V and 2.5 V I/O drivers.
3. Most speed grades and configurations of this device are offered in both Commercial and Industrial Temperature ranges. The part number of Industrial Temperature Range versions end the character "I". Unless otherwise noted, all performance specifications quoted are evaluated for worst case in the temperature range marked on the device.
4. Input Under/overshoot voltage must be –2 V > Vi < V_{DD} +2 V with a pulse width not to exceed 20% tKC.

Undershoot Measurement and Timing



Overshoot Measurement and Timing



Capacitance

(T_A = 25°C, f = 1 MHz, V_{DD} = 3.3 V)

Parameter	Symbol	Test conditions	Typ.	Max.	Unit
Input Capacitance	C_{IN}	V_{IN} = 0 V	4	5	pF
Input/Output Capacitance	$C_{I/O}$	V_{OUT} = 0 V	6	7	pF

Note: These parameters are sample tested.

Package Thermal Characteristics

Rating	Layer Board	Symbol	Max	Unit	Notes
Junction to Ambient (at 200 lfm)	single	$R_{\Theta JA}$	40	°C/W	1,2
Junction to Ambient (at 200 lfm)	four	$R_{\Theta JA}$	24	°C/W	1,2
Junction to Case (TOP)	—	$R_{\Theta JC}$	9	°C/W	3

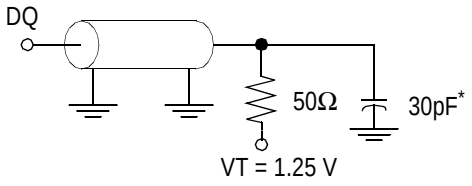
Notes:
1. Junction temperature is a function of SRAM power dissipation, package thermal resistance, mounting board temperature, ambient. Temperature air flow, board density, and PCB thermal resistance.
2. SCMI G-38-87
3. Average thermal resistance between die and top surface, MIL SPEC-883, Method 1012.1

AC Test Conditions

Parameter	Conditions
Input high level	2.3 V
Input low level	0.2 V
Input slew rate	1 V/ns
Input reference level	1.25 V
Output reference level	1.25 V
Output load	**Fig. 1& 2**

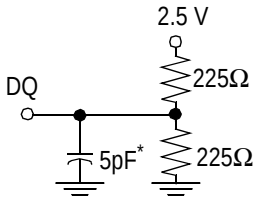
Notes:
1. Include scope and jig capacitance.
2. Test conditions as specified with output loading as shown in **Fig. 1** unless otherwise noted.
3. Output Load 2 for t_{LZ}, t_{HZ}, t_{OLZ} and t_{OHZ}
4. Device is deselected as defined by the Truth Table.

Output Load 1



* Distributed Test Jig Capacitance

Output Load 2



DC Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Max
Input Leakage Current (except mode pins)	I_{IL}	V_{IN} = 0 to V_{DD}	–1 uA	1 uA
ZZ Input Current	I_{INZZ}	$V_{DD} \geq V_{IN} \geq V_{IH}$ $0\ V \leq V_{IN} \leq V_{IH}$	–1 uA –1 uA	1 uA 300 uA
Mode Pin Input Current	I_{INM}	$V_{DD} \geq V_{IN} \geq V_{IL}$ $0\ V \leq V_{IN} \leq V_{IL}$	–300 uA –1 uA	1 uA 1 uA
Output Leakage Current	I_{OL}	Output Disable, V_{OUT} = 0 to V_{DD}	–1 uA	1 uA
Output High Voltage	V_{OH}	I_{OH} = – mA, V_{DDQ} = 2.375 V	1.7 V	—
Output High Voltage	V_{OH}	I_{OH} = – mA, V_{DDQ} = 3.135 V	2.4 V	—
Output Low Voltage	V_{OL}	I_{OL} = mA	—	0.4 V

Operating Currents

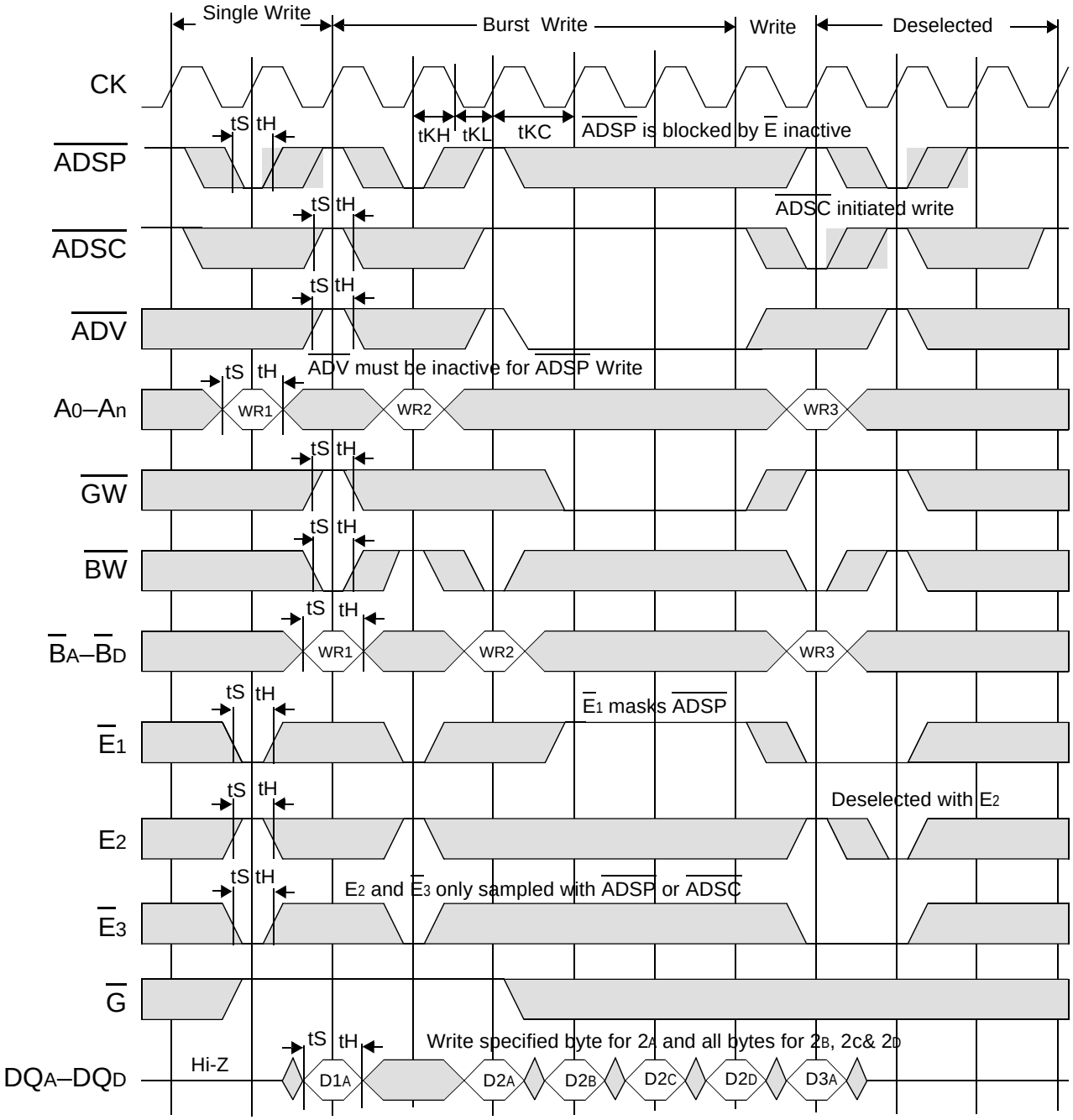
Parameter	Test Conditions	Symbol	-11		-11.5		-12		-14		-18		Unit
			0 to 70°C	-40 to 85°C	0 to 70°C	-40 to 85°C	0 to 70°C	-40 to 85°C	0 to 70°C	-40 to 85°C	0 to 70°C	-40 to 85°C	
Operating Current	Device Selected; All other inputs ≥V_{IH} or ≤ V_{IL} Output open	I_{DD} Flow-Thru	180	190	180	190	180	190	175	185	165	175	mA
Standby Current	ZZ ≥ V_{DD} °– 0.2 V	I_{SB} Flow-Thru	30	40	30	40	30	40	30	40	30	40	mA
Deselect Current	Device Deselected; All other inputs ≥ V_{IH} or ≤ V_{IL}	I_{DD} Flow-Thru	65	75	65	75	65	75	55	65	50	60	mA

AC Electrical Characteristics

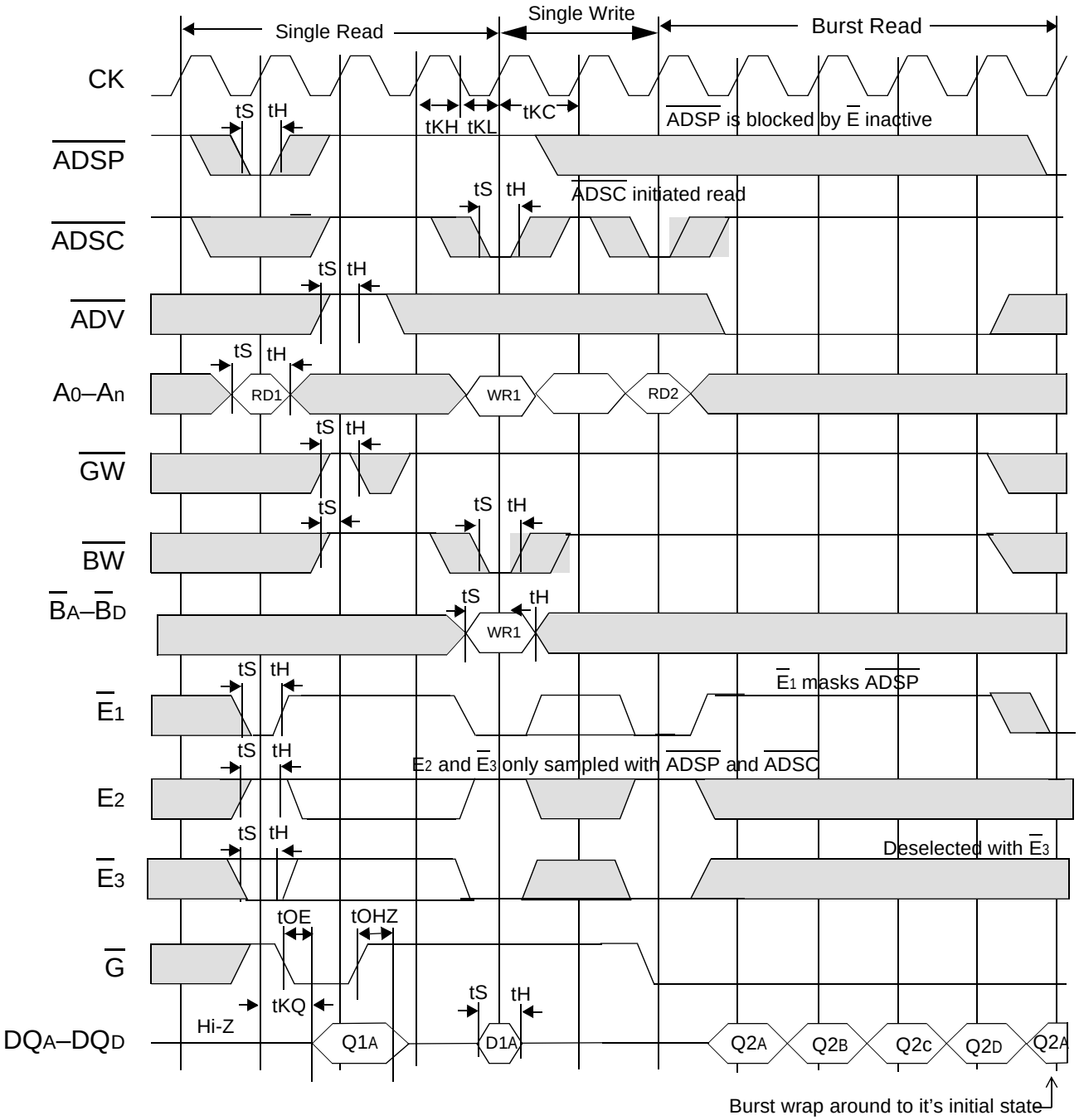
	Parameter	Symbol	-11		-11.5		-12		-14		-18		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Flow-Thru	Clock Cycle Time	tKC	15.0	—	15.0	—	15.0	—	15.0	—	20	—	ns
	Clock to Output Valid	tKQ	—	11.0	—	11.5	—	12.0	—	14.0	—	18	ns
	Clock to Output Invalid	tKQX	3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	ns
	Clock to Output in Low-Z	tLZ[1]	3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	ns
	Clock HIGH Time	tKH	1.7	—	1.7	—	2	—	2	—	2.3	—	ns
	Clock LOW Time	tKL	2	—	2	—	2.2	—	2.2	—	2.5	—	ns
	Clock to Output in High-Z	tHZ[1]	1.5	4.0	1.5	4.2	1.5	4.5	1.5	4.5	1.5	4.8	ns
	$\overline{G}$ to Output Valid	tOE	—	4.0	—	4.2	—	4.5	—	4.5	—	4.8	ns
	$\overline{G}$ to output in Low-Z	tOLZ[1]	0	—	0	—	0	—	0	—	0	—	ns
	$\overline{G}$ to output in High-Z	tOHZ[1]	—	4.0	—	4.2	—	4.5	—	4.5	—	4.8	ns
	Setup time	tS	1.5	—	2.0	—	2.0	—	2.0	—	2.0	—	ns
	Hold time	tH	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	ns
	ZZ setup time	tZZS[2]	5	—	5	—	5	—	5	—	5	—	ns
	ZZ hold time	tZZH[2]	1	—	1	—	1	—	1	—	1	—	ns
	ZZ recovery	tZZR	20	—	20	—	20	—	20	—	20	—	ns

Notes:
1. These parameters are sampled and are not 100% tested.
2. ZZ is an asynchronous signal. However, in order to be recognized on any given clock cycle, ZZ must meet the specified setup and hold times as specified above.

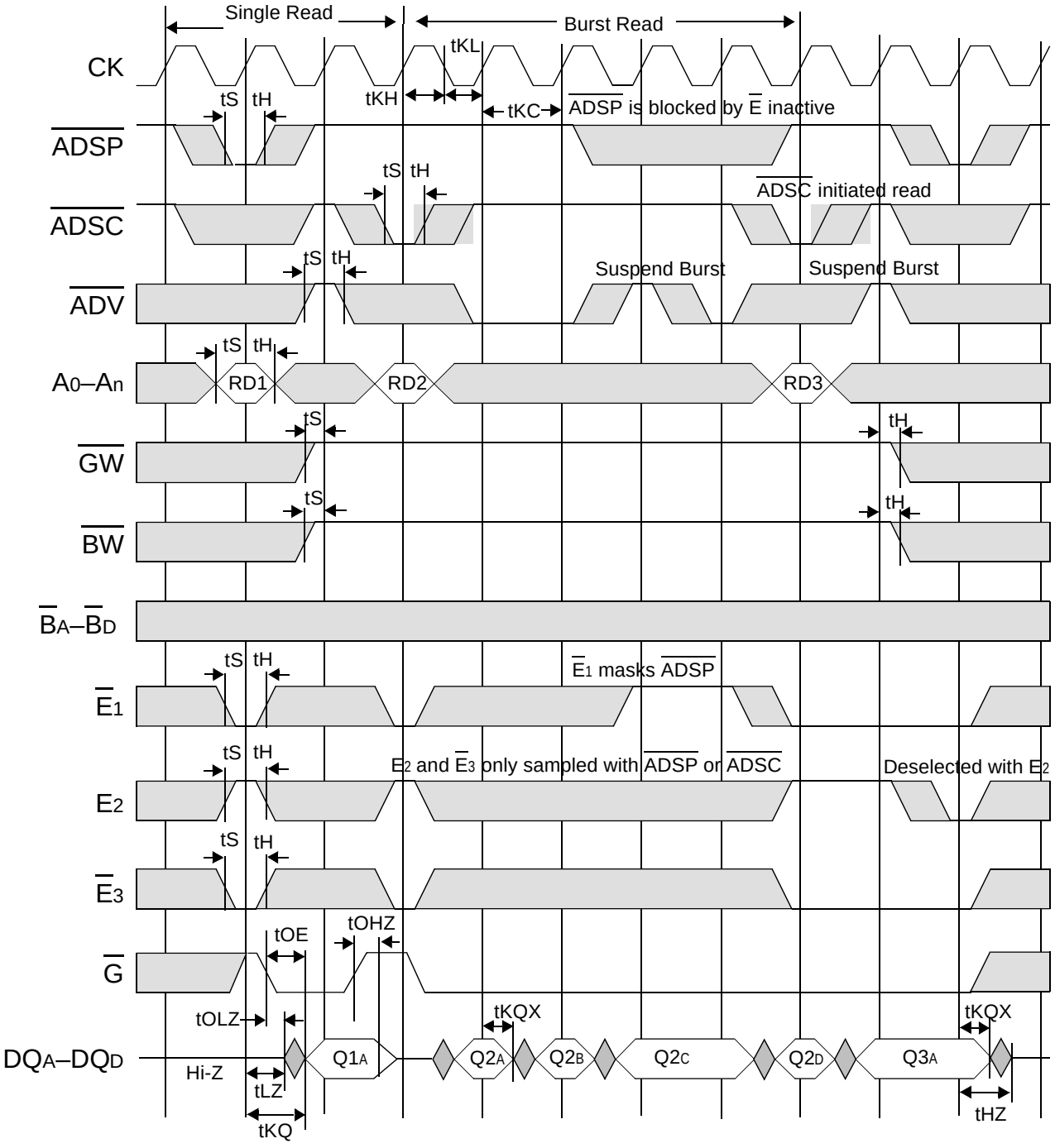
Write Cycle Timing



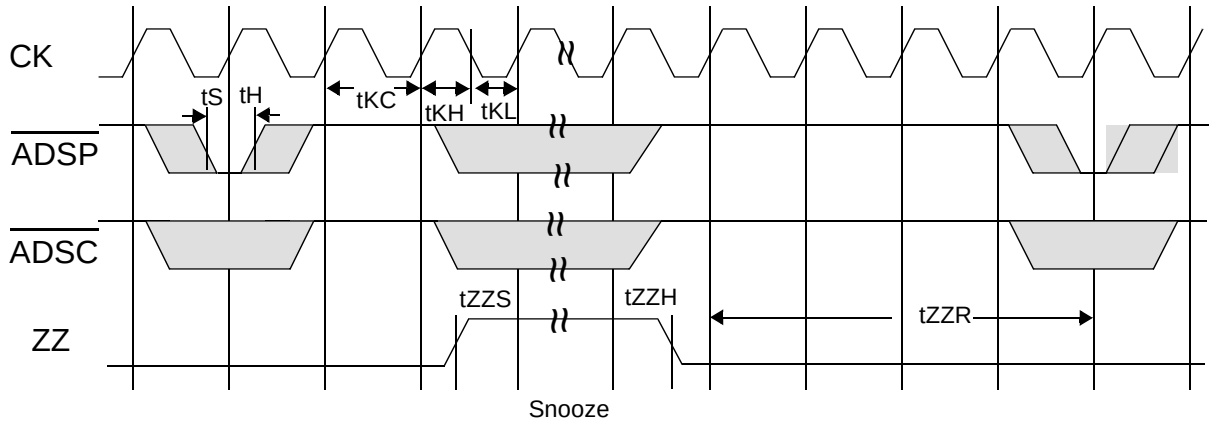
Flow Through Read-Write Cycle Timing



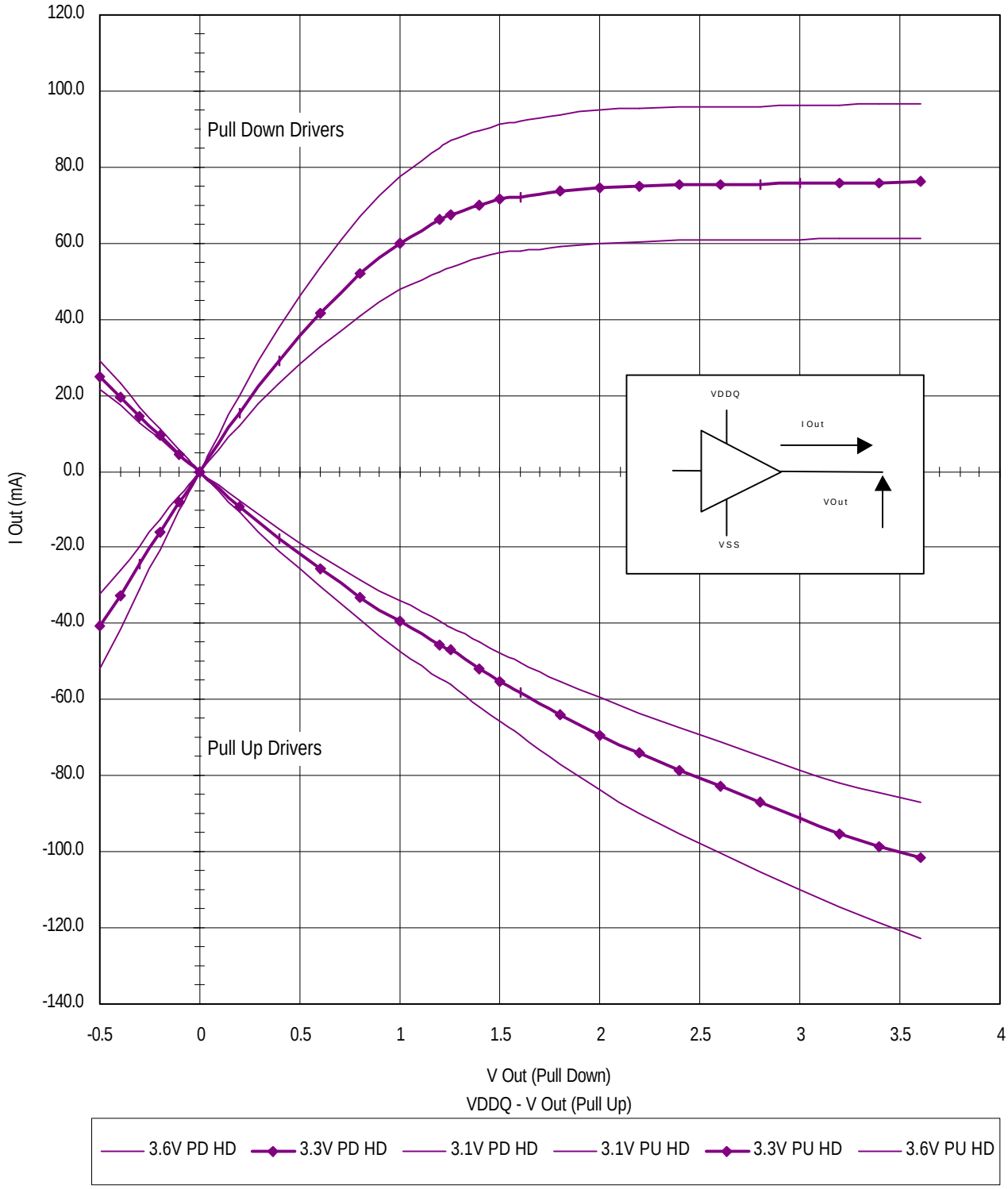
Flow Through Read Cycle Timing



Sleep Mode Timing Diagram

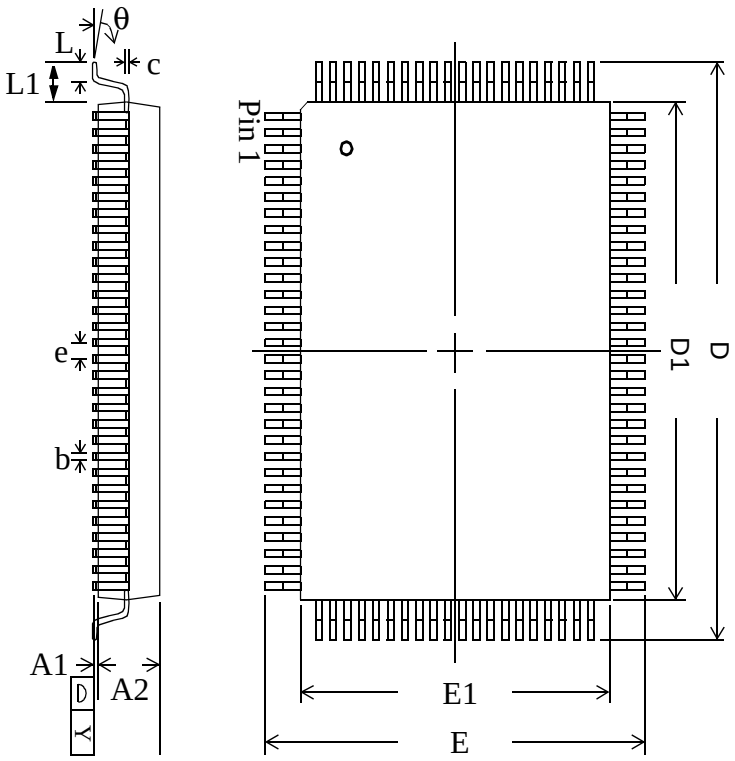


Output Driver Characteristics



TQFP Package Drawing

Symbol	Description	Min.	Nom.	Max
A1	Standoff	0.05	0.10	0.15
A2	Body Thickness	1.35	1.40	1.45
b	Lead Width	0.20	0.30	0.40
c	Lead Thickness	0.09	—	0.20
D	Terminal Dimension	21.9	22.0	22.1
D1	Package Body	19.9	20.0	20.1
E	Terminal Dimension	15.9	16.0	16.1
E1	Package Body	13.9	14.0	14.1
e	Lead Pitch	—	0.65	—
L	Foot Length	0.45	0.60	0.75
L1	Lead Length	—	1.00	—
Y	Coplanarity	—	—	0.10
θ	Lead Angle	0°	—	7°



Notes:
1. All dimensions are in millimeters (mm).
2. Package width and length do not include mold protrusion.

BPR 1999.05.18

Ordering Information for GSI Synchronous Burst RAMs

Org	Part Number[1]	Type	Package	Speed[2] (MHz/ns)	T_A[3]	Status
512K x 18	GS880F18T-11	Flow Through	TQFP	11	C	
512K x 18	GS880F18T-11.5	Flow Through	TQFP	11.5	C	
512K x 18	GS880F18T-12	Flow Through	TQFP	12	C	
512K x 18	GS880F18T-14	Flow Through	TQFP	14	C	
512K x 18	GS880F18T-18	Flow Through	TQFP	18	C	
256K x 36	GS880F36T-11	Flow Through	TQFP	11	C	
256K x 36	GS880F36T--11.5	Flow Through	TQFP	11.5	C	
256K x 36	GS880F36T-12	Flow Through	TQFP	12	C	
256K x 36	GS880F36T-14	Flow Through	TQFP	14	C	
256K x 36	GS880F36T-18	Flow Through	TQFP	18	C	
512K x 18	GS880F18T-11I	Flow Through	TQFP	11	I	
512K x 18	GS880F18T--11.5I	Flow Through	TQFP	11.5	I	
512K x 18	GS880F18T-12I	Flow Through	TQFP	12	I	
512K x 18	GS880F18T-14I	Flow Through	TQFP	14	I	
512K x 18	GS880F18T-18I	Flow Through	TQFP	18	I	
256K x 36	GS880F36T-11I	Flow Through	TQFP	11	I	
256K x 36	GS880F36T--11.5I	Flow Through	TQFP	11.5	I	
256K x 36	GS880F36T-12I	Flow Through	TQFP	12	I	
256K x 36	GS880F36T-14I	Flow Through	TQFP	14	I	
256K x 36	GS880F36T-18I	Flow Through	TQFP	18	I	

Notes:

1. Customers requiring delivery in Tape and Reel should add the character "T" to the end of the part number. Example: GS880LF18TT.
2. The speed column indicates the cycle frequency (MHz) of the device in Pipeline mode and the latency (ns) in Flow Through mode. Each device is Pipeline/Flow Through mode-selectable by the user.
3. T_A = C = Commercial Temperature Range. T_A = I = Industrial Temperature Range.
4. GSI offers other versions this type of device in many different configurations and with a variety of different features, only some of which are covered in this data sheet. See the GSI Technology web site (www.gsitechnology.com) for a complete listing of current offerings.

Revision History

DS/DateRev. Code: Old; New	Types of Changes Format or Content	Page;Revisions;Reason
GS880F18/361.00 11/1999J	Content	• First Release of 880 F.
GS880F18/36T1.00 K**880F18/36T**1.02 1/2000L	Content	• Changed Flow Through Read-Write Cycle Timing Diagram for accuracy. • Changed order of TQFP Address Inputs to match pinout. • Changed order of TQFP DATA Input and Output pins to match pinout. • New GSI Logo.
GS880F1836T Rev. 1.02 1/ 2000L; GS880F1836T Rev. 1.03 3/ 2000N	Content	• Changed all speed bin information (headings, references, tables, ordering info..) to reflect 14 -10Mhz
GS880F1836T Rev. 1.03 1/ 2000N; GS880F1836T Rev. 1.04 3/ 2000O	Content	• Corrections to AC Electrical Characteristics Table -
GS880F1836T Rev. 1.04 3/ 2000O; 880F1836_r1_05	Content/Format	• Removed 150 MHz speed bin • Added 18 ns speed bin • Updated format to comply with Technical Publications standards
880F18_r1_05; 880F18_r1_06	Content	• Updated Capitance table—removed Input row and changed Output row to I/O

